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**NI-7932**

**Manufacturer:** National Instruments

**Board Assembly Part Numbers** (Refer to Procedure 1 for identification procedure):

Part Number and Revision	Description
157752A-0xL or later	NI-7931R, NI-7932R, and NI-7935R

## Volatile Memory

<i>Target Data</i>	<i>Type</i>	<i>Size</i>	<i>Battery Backup</i>	<i>User<sup>1</sup> Accessible</i>	<i>System Accessible</i>	<i>Sanitization Procedure</i>
System Memory	CPU DRAM	512 MB	No	Yes	Yes	Cycle Power
System Processing	Zynq Block RAM	560 Kb	No	No	No	Cycle Power
Field Programmable Gate Array	Kintex-7 Block RAM	16,020Kb or 28,620Kb	No	Yes	Yes	Cycle Power
Data storage during VI Execution	FPGA DRAM	2 GB	No	Yes	Yes	Cycle Power
CPLD Memory	CPLD	32 B	No	No	Yes	Cycle Power
Time Keeping	RTC	20 B	Yes	No	Yes	Procedure 2

## Non-Volatile Memory (*incl. Media Storage*)

<i>Target Data</i>	<i>Type</i>	<i>Size</i>	<i>Battery Backup</i>	<i>User Accessible</i>	<i>System Accessible</i>	<i>Sanitization Procedure</i>
Operating System constants	EEPROM	2Kb	No	No	Yes	None
Board revision, clocking and voltage constants	EEPROM	2Kb	No	No	Yes	None
CPLD configuration	CPLD	0.17 MB	No	No	No	None
Operating System Storage	Flash	512 MB	No			Procedure 3
• Device Firmware				No	Yes	
• Operating System				Yes	Yes	
• User Data				Yes	Yes	
User FPGA Bitfile	Flash	512 MB	No	Yes	Yes	Procedure 3

<sup>1</sup> Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

## Procedures

### **Procedure 1 – Board Assembly Part Number identification:**

To determine the Board Assembly Part Number and Revision, refer to the label applied to the bottom surface of your product. The Assembly Part Number should be formatted as “P/N: #####a-##L.

### **Procedure 2 – Time-Keeping RTC:**

To clear the battery-backed Time-Keeping RTC, complete the following steps:

1. Remove the battery
2. Unplug master power for at least 5 minutes

### **Procedure 3 – Operating System Storage Flash & User FPGA Bitfile:**

To clear the Operating System Storage Flash and the User FPGA Bitfile, complete the following steps:

1. Connect to your NI-793XR as outlined in the NI-793XR Getting Started Guide
2. Open NI MAX
3. Find and select your NI-793XR device under “Remote Systems”
4. Click on the “Update Firmware” button and choose a default firmware image to re-flash the entire Operating System Storage Flash and User FPGA Bitfile memory to a default, factory state.

## Terms and Definitions

### **Cycle Power:**

The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

### **Volatile Memory:**

Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

### **Non-Volatile Memory:**

Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

### **User Accessible:**

The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

### **System Accessible:**

The component is read and/or write addressable from the host without the need to physically alter the product.

### **Clearing:**

Per *NIST Special Publication 800-88 Revision 1*, “clearing” is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

### **Sanitization:**

Per *NIST Special Publication 800-88 Revision 1*, “sanitization” is a process to render access to “Target Data” on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.