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NI PXIe-6556 Specifications

200 MHz Digital Waveform Generator/Analyzer with PPMU

このドキュメントには、日本語ページも含まれています。

This document provides the specifications for the NI PXIe-6556 (NI 6556). Specifications are subject to change without notice. For the most recent NI 6556 specifications, visit `ni.com/manuals`. To access the NI 6556 documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 6556 signals and the connector pinouts, navigate to **Start»Programs» National Instruments»NI-HSDIO»Documentation**.

Caution The NI 6556 has a maximum operating temperature range of 0 ºC to +45 ºC in all NI PXI Express and hybrid NI PXI Express chassis.

Hot Surface If the NI 6556 has been in use, it may exceed safe handling temperatures and cause burns. Allow time to cool before removing the NI 6556 from the chassis.

Caution Refer to the *Read Me First: Safety and Electromagnetic Compatibility* document for important safety and electromagnetic compatibility information. To obtain a copy of this document online, visit `ni.com/manuals`, and search for the document title.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure specified EMC performance, you must install PXI EMC Filler Panels, National Instruments part number 778700-01, in all open chassis slots.

Caution To ensure the specified EMC performance, all I/O cables must be no longer than 3 m (10 ft).

Note All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

NATIONAL INSTRUMENTS

Terminology

Maximum and *minimum* specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

All specifications are *Typical* unless otherwise noted. These specifications are valid within the operating temperature range. Accuracy specifications are valid within ±5 ºC of self-calibration unless otherwise noted.

Contents

Channel Specifications

Specification	Value	Comments
Number of data channels	24, per pin parametric measurement unit (PPMU) enabled	All data channels have pattern memory.
Direction control of data channels	Per channel	—
Number of programmable function interface (PFI) channels	4 PPMU-enabled PFI channels: PFI 1, PFI 2, PFI 4/DDC CLK OUT, and PFI 5/STROBE 10 general PFI channels: PFI 0, PFI 3, and PFI <24..31>	Refer to the *Waveform Specifications* section for more details.
Direction control of PFI channels	Per channel	—
Number of clock terminals	4 input 2 output	Refer to the *Timing Specifications* section for more details.
Number of remote sense channels	28	All PPMU-enabled channels have remote sense capability.

Digital Generation Channels (DIO <0..23>, PFI 1, PFI 2, PFI 4, and PFI 5)

Note These features are controlled independently per channel.

Specification	Value		Comments
Generation signal type	Single-ended, ground referenced.		—
Programmable generation voltage levels	Drive Voltage High Level (V_{OH}) Drive Voltage Low Level (V_{OL}) Drive Tristate (V_{TT})		—
Generation voltage range	–2 V to 6 V (default) or –1 V to 7 V		Software-selectable.
Generation voltage resolution	122 µV		—
DC generation voltage accuracy	**±5 ºC of Self-Calibration**	**±15 ºC of Self-Calibration**	Maximum accuracy when operating within the specified self-calibration temperature range.
	±11 mV	±16 mV	
Generation voltage swing	400 mV to 8.0 V		Into a 1 MΩ load. Power limitations may restrict the number of channels toggling at full voltage swing.
Output impedance	50 Ω		Nominal.

Specification	Value	Comments
Maximum allowed DC drive strength per channel	±35 mA	Nominal. Do *not* exceed the maximum power limit of the device.
Data channel tristate control	Per channel, per cycle	Software-selectable and hardware-timed.
Channel power-on state	Drivers disabled, high impedance	—
Output protection	The device can indefinitely sustain a short to any voltage between –3 V and 8.5 V provided that you observe the maximum drive strength limitations.	—

Digital Acquisition Channels (DIO <0..23>, PFI 1, PFI 2, PFI 4, and PFI 5)

Note These features are controlled independently per channel.

Specification	Value	Comments
Acquisition signal type	Single-ended, ground referenced	—
Programmable acquisition voltages	Compare Voltage High Threshold (V_{IH}) Compare Voltage Low Threshold (V_{IL}) Termination Voltage (V_{TT})	—
Acquisition voltage threshold range	–2 V to 7 V	—
Acquisition and termination voltage resolution	122 µV	—

Specification	Value		Comments
Termination voltage range	–2 V to 6 V (default) or –1 V to 7 V		—
DC acquisition voltage threshold accuracy	**±5 ºC of Self-Calibration**	**±15 ºC of Self-Calibration**	Maximum accuracy when operating within the specified self-calibration temperature range below 6.8 V.
	(V_{IL}) = ±25 mV (V_{IH}) = ±25 mV (V_{TT}) = ±11 mV	(V_{IL}) = ±28 mV (V_{IH}) = ±28 mV (V_{TT}) = ±16 mV	
Minimum detectable voltage swing	50 mV		—
Input impedance	High-impedance or 50 Ω terminated into V_{TT}		Software-selectable.
High impedance leakage	±10 nA		Maximum.
Input protection	The device can indefinitely sustain a short to any voltage between –3 V and 8.5 V, provided that you observe the maximum drive strength limitations.		—

PPMU Channels (DIO <0..23>, PFI 1, PFI 2, PFI 4, and PFI 5)

Note These features are controlled independently per channel.

Specification	Value	Comments
PPMU signal type	Single-ended, ground referenced	Referenced to the ground pins on the VHDCI connector.
Programmable states	Force voltage (FV) Force current (FI) Voltage clamp high (V_{CHI}) Voltage clamp low (V_{CLO})	Clamp voltages are only active when forcing current.

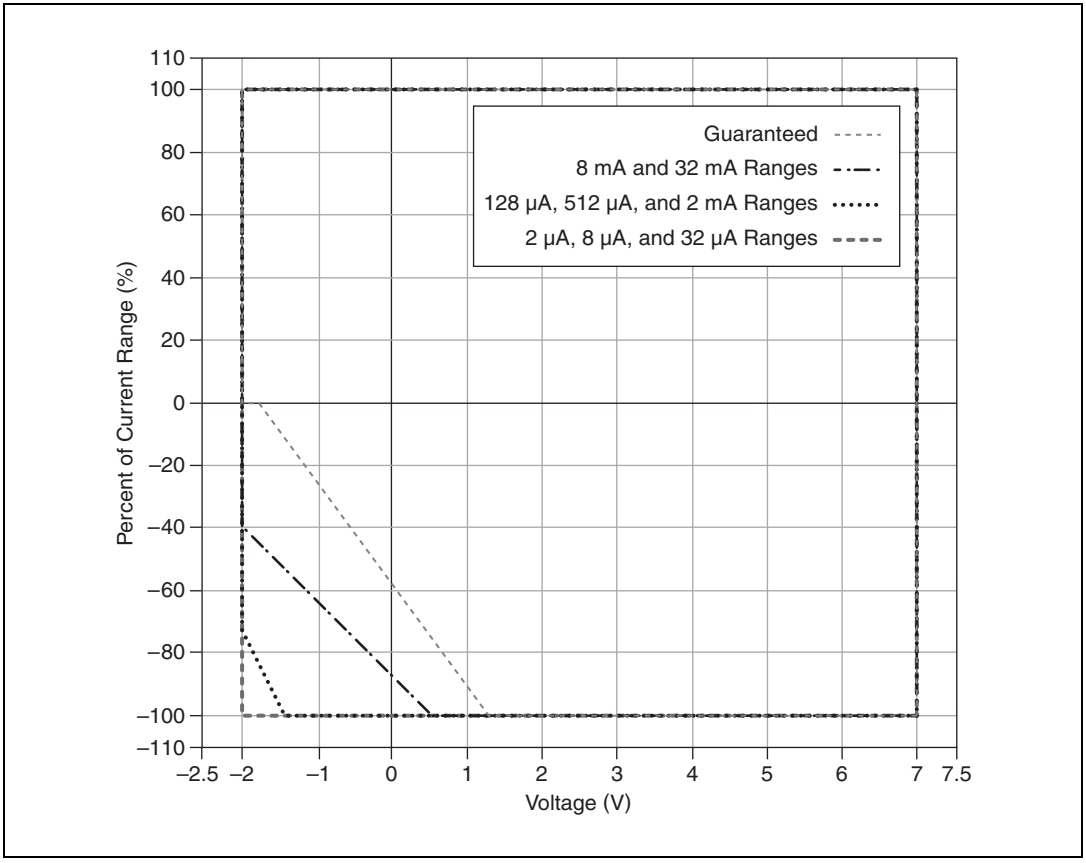


Figure 1. Characteristic Quadrant Behavior by Current Range

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td rowspan="3">Force voltage</td><td>Ranges</td><td>Resolution</td><td>Accuracy within ±5 ºC of Self-Calibration</td><td>Accuracy within ±15 ºC of Self-Calibration</td><td rowspan="3">Maximum accuracy at the sense location.</td></tr>
<tr><td>–2 V to 6 V (default)
–1 V to 7 V</td><td>122 µV</td><td>±11 mV</td><td>±16 mV</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="7">Force voltage settling time</td><td colspan="2">Current Range</td><td colspan="2">Settling Time</td><td rowspan="7">Settled to 1% of the final value. 1 V steps with 50% of the current range load into 100 pF.</td></tr>
<tr><td colspan="2">2 µA</td><td colspan="2">150 µs</td></tr>
<tr><td colspan="2">8 µA</td><td colspan="2">75 µs</td></tr>
<tr><td colspan="2">32 µA, 128 µA, 512 µA</td><td colspan="2">40 µs</td></tr>
<tr><td colspan="2">2 mA</td><td colspan="2">45 µs</td></tr>
<tr><td colspan="2">8 mA</td><td colspan="2">55 µs</td></tr>
<tr><td colspan="2">32 mA</td><td colspan="2">60 µs</td></tr>
<tr><td rowspan="9">Load capacitance</td><td colspan="2">Current Range</td><td colspan="2">Capacitance</td><td rowspan="9">These values represent the allowed load capacitance through a 1 m SHC68-C68-D4 cable to ensure a well-behaved transient response.</td></tr>
<tr><td colspan="2">2 µA</td><td colspan="2">1 nF</td></tr>
<tr><td colspan="2">8 µA</td><td colspan="2">1 nF</td></tr>
<tr><td colspan="2">32 µA</td><td colspan="2">1 nF</td></tr>
<tr><td colspan="2">128 µA</td><td colspan="2">1 nF</td></tr>
<tr><td colspan="2">512 µA</td><td colspan="2">4.7 nF</td></tr>
<tr><td colspan="2">2 mA</td><td colspan="2">10 nF</td></tr>
<tr><td colspan="2">8 mA</td><td colspan="2">47 nF</td></tr>
<tr><td colspan="2">32 mA</td><td colspan="2">100 nF</td></tr>
</table>

Characteristic Step Response

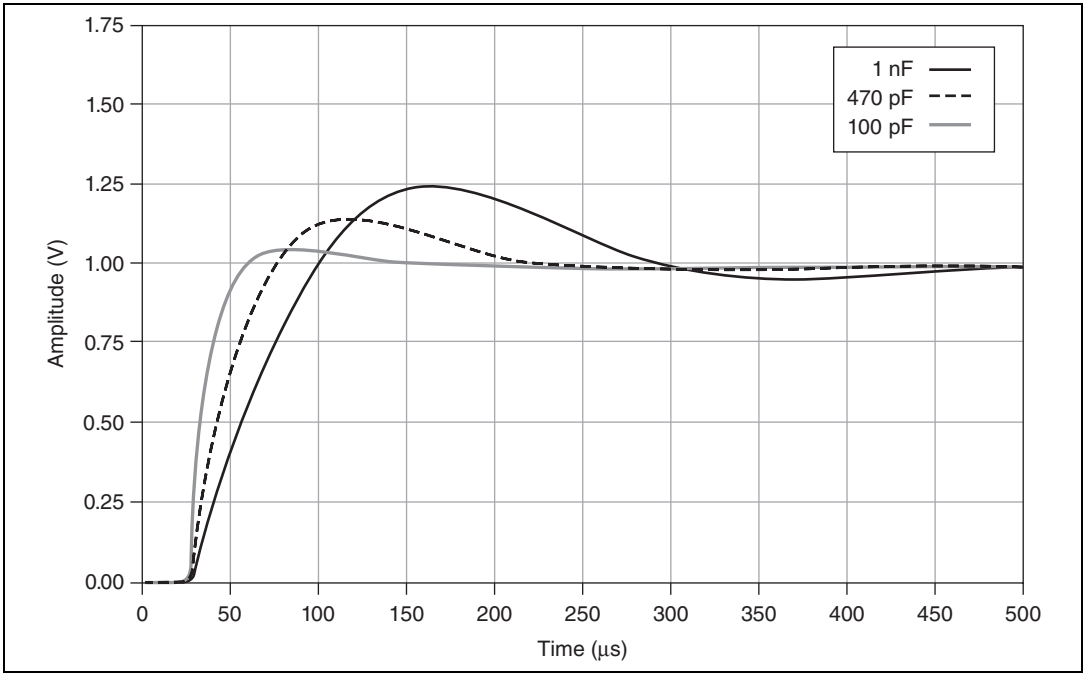


Figure 2. Characteristic Step Response into a Capacitive Load in the 2 µA Range

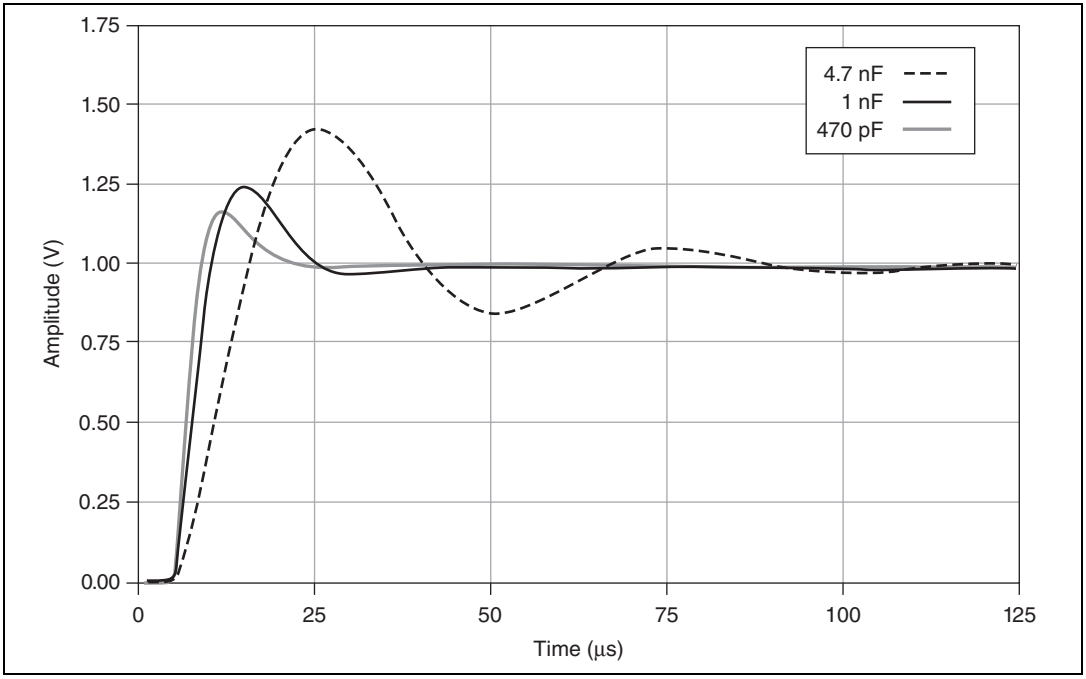


Figure 3. Characteristic Step Response into a Capacitive Load in the 512 µA Range

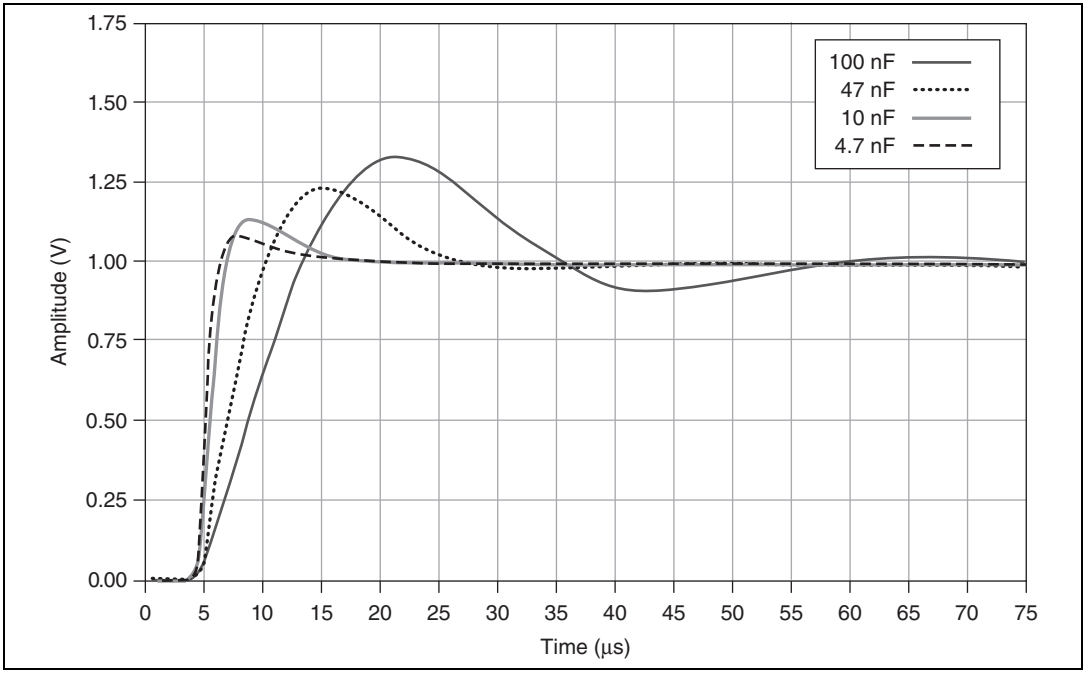


Figure 4. Characteristic Step Response into a Capacitive Load in the 32 mA Range

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td rowspan="9">Force current resolution</td><td colspan="2">Current Range</td><td colspan="2">Resolution</td><td rowspan="9">Nominal.</td></tr>
<tr><td colspan="2">±2 µA</td><td colspan="2">60 pA</td></tr>
<tr><td colspan="2">±8 µA</td><td colspan="2">240 pA</td></tr>
<tr><td colspan="2">±32 µA</td><td colspan="2">980 pA</td></tr>
<tr><td colspan="2">±128 µA</td><td colspan="2">3.9 nA</td></tr>
<tr><td colspan="2">±512 µA</td><td colspan="2">15.6 nA</td></tr>
<tr><td colspan="2">±2 mA</td><td colspan="2">60 nA</td></tr>
<tr><td colspan="2">±8 mA</td><td colspan="2">240 nA</td></tr>
<tr><td colspan="2">±32 mA</td><td colspan="2">980 nA</td></tr>
<tr><td rowspan="2">Force current accuracy</td><td colspan="2">Accuracy within ±5 ºC of Self-Calibration</td><td colspan="2">Accuracy within ±15 ºC of Self-Calibration</td><td rowspan="2">Maximum.</td></tr>
<tr><td colspan="2">1% of range</td><td colspan="2">1.3% of range</td></tr>
<tr><td rowspan="4">Force current voltage clamps</td><td colspan="2">Current Range</td><td>Resolution</td><td>Accuracy within ±15 ºC of Self-Calibration</td><td rowspan="4">Maximum. Voltage clamps begin to conduct within 700 mV of the programmable voltage level.</td></tr>
<tr><td>V_{CLO}</td><td>–2 V to 6 V</td><td rowspan="2">122 µV</td><td rowspan="2">±100 mV</td></tr>
<tr><td>V_{CHI}</td><td>–1 V to 7 V</td></tr>
<tr><td colspan="4">Note: (V_{CHI} – V_{CLO}) > 1 V</td></tr>
<tr><td>Aperture time range</td><td colspan="4">4 µs to 65 ms</td><td>—</td></tr>
<tr><td>Aperture time resolution</td><td colspan="4">4 µs</td><td>—</td></tr>
<tr><td rowspan="2">Measure voltage</td><td colspan="2">Range</td><td>Resolution</td><td>Accuracy within ±15 ºC of Self-Calibration</td><td rowspan="2">Maximum accuracy at the sense location with one 60 Hz PLC aperture.</td></tr>
<tr><td colspan="2">–2 V to 7 V</td><td>228 µV</td><td>±3 mV</td></tr>
</table>

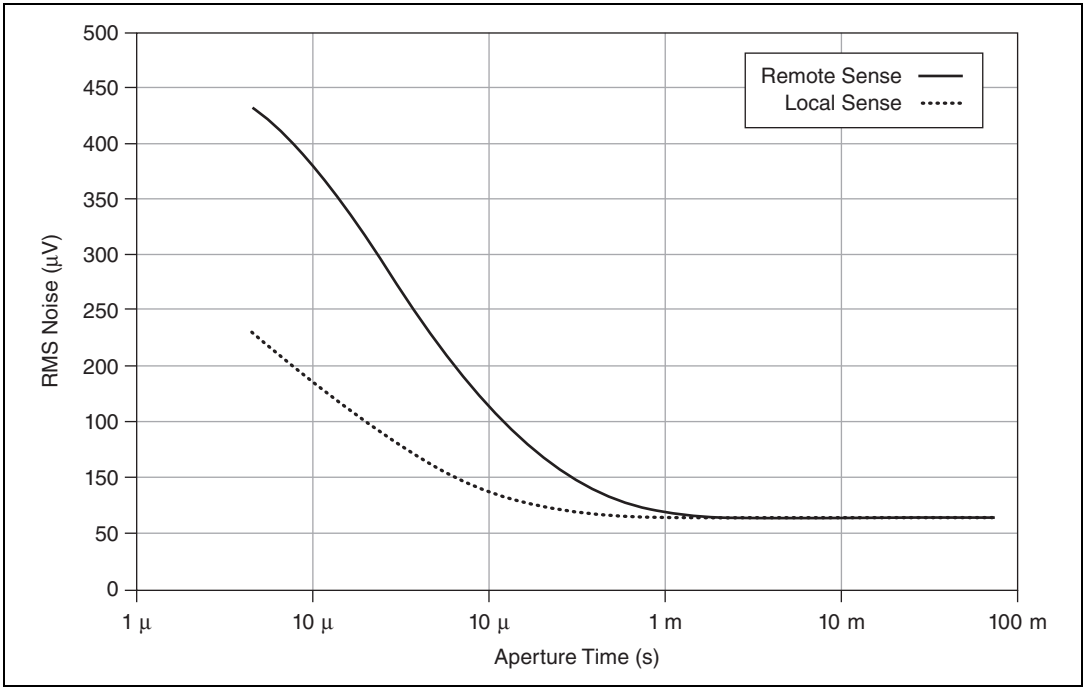


Figure 5. Typical Voltage Measurement Noise for Given Aperture Times

Specification	Value		Comments
Measure current resolution	**Current Range**	**Resolution**	Nominal.
	±2 µA	460 pA	
	±8 µA	1.8 nA	
	±32 µA	7.3 nA	
	±128 µA	30 nA	
	±512 µA	120 nA	
	±2 mA	460 nA	
	±8 mA	1.8 µA	
	±32 mA	7.3 µA	
Measure current accuracy	**Accuracy within ±5 ºC of Self-Calibration**	**Accuracy within ±15 ºC of Self-Calibration**	Maximum accuracy with one 60 Hz PLC aperture.
	1% of range	1.3% of range	

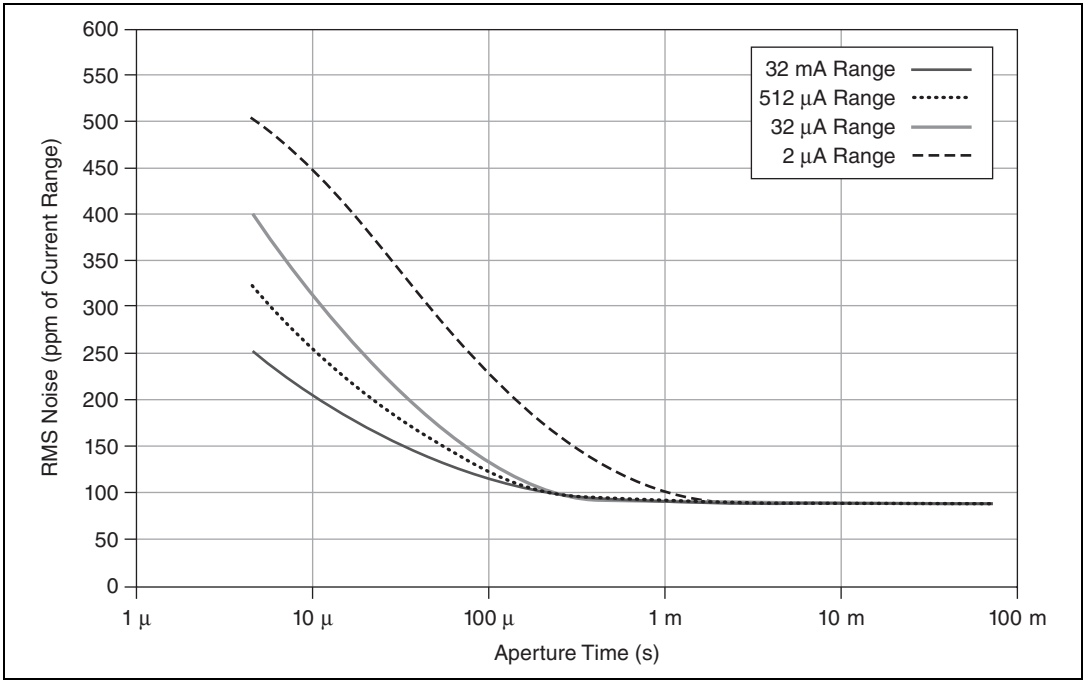


Figure 6. Typical Current Measurement Noise for Given Aperture Times

Note I_{RMS} *Noise* is represented by the following equation:

$$I_{RMS}\ Noise = (RMS\ Noise \times Current\ Range) / 10^6$$

For example, 100 ppm on a 32 mA range yields a noise of 3.2 µA RMS.

$$3.2\ \mu A\ RMS = (100\ ppm \times 32\ mA) / 10^6$$

Specification	Value	Comments
I/O switch resistance	5.5 Ω	Nominal.
Remote feedback impedance	100 kΩ	Nominal.
Output protection	The device can indefinitely sustain a short to any voltage between –3 V and 8.5 V, provided that you observe the maximum drive strength limitations.	—

General PFI Channels (PFI 0, PFI 3, and PFI <24..31>)

Specification	Value				Comments
Circuit type	PFI 0 and PFI 3: High-speed I/O circuits PFI <24..31>: 5V compatible I/O circuits				—
Generation voltage level	**Low Voltage Levels**		**High Voltage Levels**		100 µA load.
	Characteristic	**Maximum**	**Minimum**	**Characteristic**	
	0 V	0.2 V	3.1 V	3.3 V	
Drive strength	PFI 0 and PFI 3: ±33 mA PFI <24..31>: ±85 mA				—
Output impedance	50 Ω				Nominal.
Output protection	The device can indefinitely sustain a short to any voltage between 0 V and 5 V.				—
Acquisition voltage level	**Low Voltage Thresholds**		**High Voltage Thresholds**		Nominal.
	0.8 V		2 V		
Input protection	PFI 0 and PFI 3: –1 V to 5 V PFI <24..31>: –1 V to 6.5 V				Maximum.

EXTERNAL FORCE and EXTERNAL SENSE Channels

Note These specifications are valid for the EXTERNAL FORCE and EXTERNAL SENSE channels on the AUX I/O connector or on the REMOTE SENSE connector. The AUX I/O connector is available only on NI 6556 devices.

Specification	Value	Comments
Direction	EXTERNAL FORCE: input to the device EXTERNAL SENSE: output from the device	—
Analog bandwidth	EXTERNAL FORCE: 3 MHz EXTERNAL SENSE: 30 kHz	Characteristic with a single channel connected.
Range	–2 V to 7 V	—
Maximum current	±32 mA	Valid for EXTERNAL FORCE only.
Input protection	The device can indefinitely sustain a short to any voltage between –3 V and 8.5 V, provided that you observe the maximum drive strength limitations.	—

CAL Channels

Note These specifications are valid for the CAL channel on the AUX I/O connector and on the REMOTE SENSE connector. The AUX I/O connector is available only on NI 6556 devices.

Specification	Value	Comments
Direction	Output from the NI 6556 during external calibration. This channel is in a high-impedance or undriven state during normal operation.	—
Voltage level	5 V	Nominal.
Drive strength	1 mA	Maximum allowed. Sourcing only.

Timing Specifications

Sample Clock

Specification	Value	Comments
Sample clock sources	1. On Board Clock 2. CLK IN (SMA jack connector) 3. PXIe_DStarA (PXI Express backplane) 4. STROBE (Digital Data & Control (DDC) connector; acquisition only)	—
On Board Clock frequency range	800 Hz to 200 MHz	—
On Board Clock frequency resolution	<0.1 Hz	NI-HSDIO may be queried for the programmed frequency value.
On Board Clock frequency accuracy	±150 ppm	Nominal. Accuracy may be increased by using a higher performance external Reference clock.
CLK IN frequency range	20 kHz to 200 MHz	Refer to the *CLK IN (SMA Jack Connector)* section for restrictions based on waveform type.

Specification	Value	Comments
PXIe_DStarA frequency range	800 Hz to 200 MHz	Refer to the *PXIe_DStarA (PXI Express Backplane)* section for more information.
STROBE frequency range	800 Hz to 200 MHz	Refer to the *PFI 5 as STROBE (DDC Connector)* section for more information.
Sample clock relative delay adjustment range	±5 ns	To align multiple devices, apply a delay or phase adjustment to the On Board Clock.
Sample clock relative delay adjustment resolution	3.125 ps	
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMA jack connector)	Internal Sample clocks with sources other than STROBE can be exported.
Exported Sample clock offset range (t_{CO})	0 ns to 2.4 ns	Software programmable.
Exported Sample clock offset resolution (t_{CO})	13 ps	

Specification	Value		Comments
Exported Sample clock offset accuracy (t_{CO})	±200 ps		Software programmable.
Exported Sample clock duty cycle (DDC CLK OUT)	**Minimum**	**Maximum**	3.3 V at maximum clock rate (200 MHz). Not including the effects of system crosstalk.
	42%	55%	
Exported Sample clock period jitter	24 ps_{rms}		Characteristic; using On Board Clock.

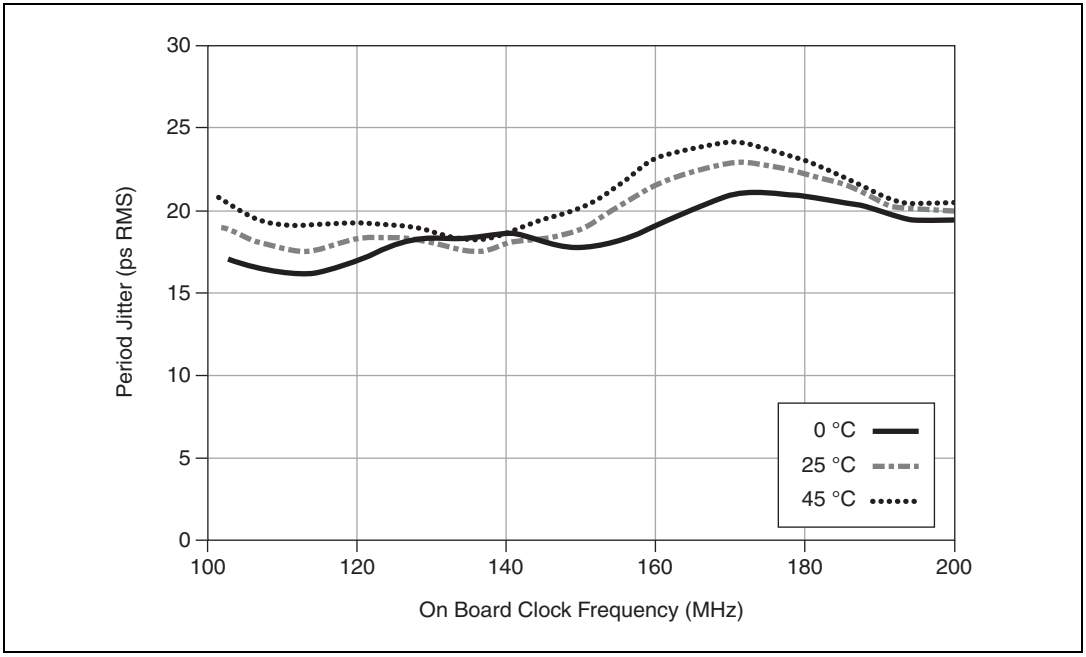


Figure 7. Characteristic Period Jitter (RMS) versus Frequency

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value	Comments
Maximum data rate per channel	200 Mbps Supported for all logic families	—
Maximum data channel toggle rate	3.3 V swing: 100 MHz 5 V swing: 50 MHz	Toggle rates exceeding these values may invalidate CE certifications. Refer to the *Electromagnetic Compatibility* section for more information.

Figure 8 shows an eye diagram of a 200 Mbps pseudorandom bit sequence (PRBS) waveform at 3.3 V. This waveform was captured on a characteristic DIO channel at room temperature into high-impedance.

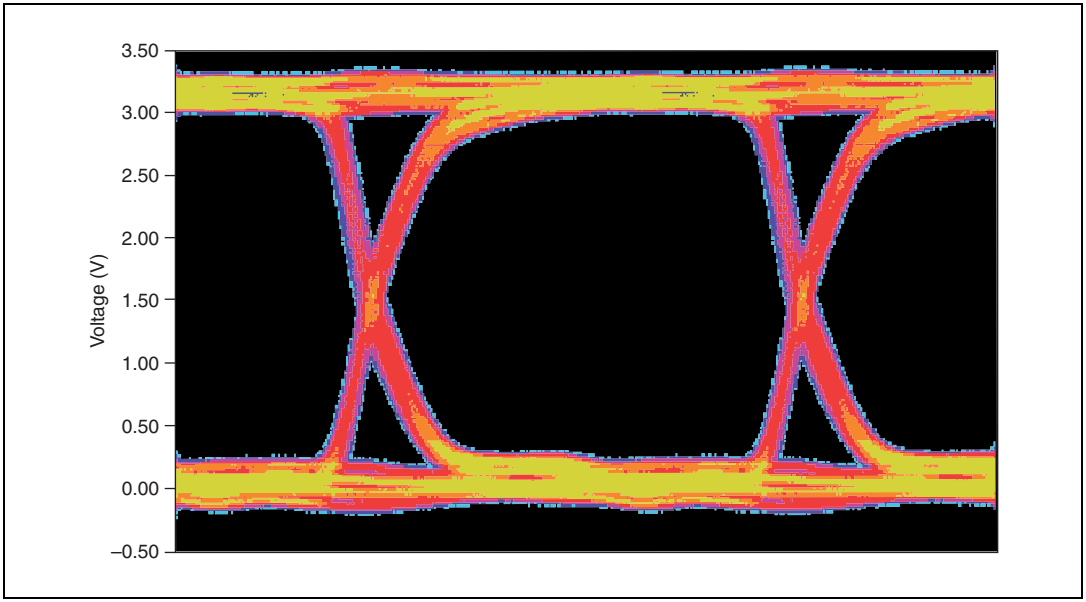


Figure 8. Characteristic Eye Diagram at 3.3 V

Figure 9 shows an eye diagram of a 200 Mbps PRBS waveform at 0.4 V. This waveform was captured on a characteristic DIO channel at room temperature into high-impedance.

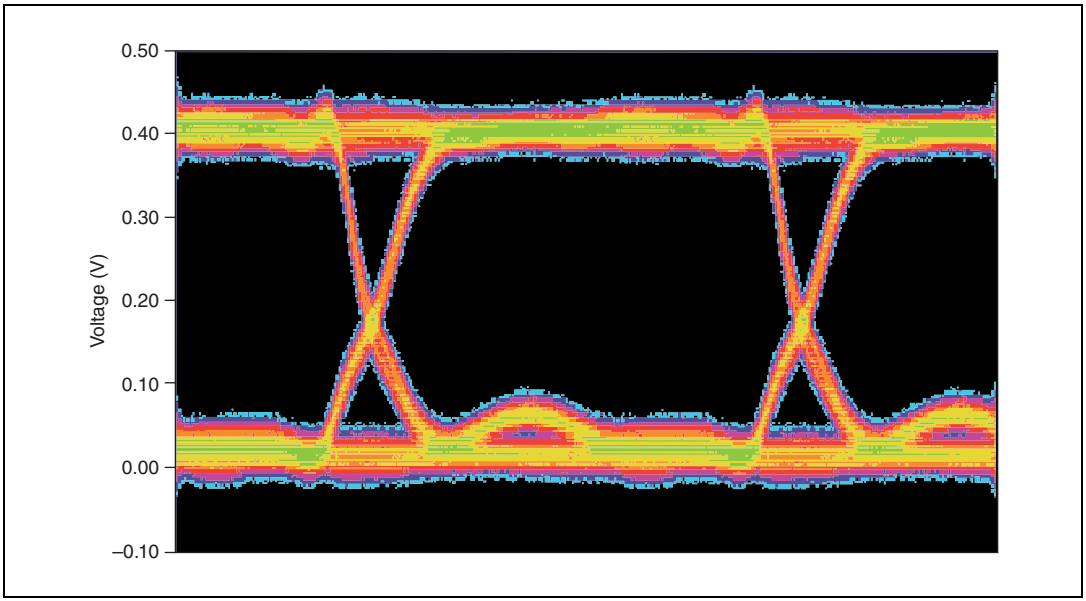


Figure 9. Characteristic Eye Diagram at 0.4 V

Specification	Value		Comments
Data channel-to-channel skew	Characteristic: ±300 ps Maximum: ±600 ps		Skew across all data channels and voltage levels. The maximum value includes temperature effects. Within ±15 ºC of self-calibration.
Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge		—
Generation data delay frequency	**On Board Clock**	**External Clock**	—
	All supported frequencies	Frequencies ≥ 20 MHz	

Specification	Value	Comments
Generation data delay range	–1 to 2 Sample clock cycles, expressed as a fraction of the Sample clock period	The sum of data delay and data deskew may not exceed –2 to 3 Sample clock cycles.
Generation data deskew range	–2 to 3 Sample clock cycles, expressed as a time in seconds	
Generation data delay and data deskew resolution	30 ps	Nominal.
Generation data delay and data deskew linearity accuracy	TBD	—
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	TBD	—

Generation Provided Setup and Hold Times

Exported Sample Clock Offset (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
Software-programmable	t_P–t_{CO} – 900 ps	t_{CO} – 600 ps

Compare the setup and hold times from the datasheet of your device under test (DUT) to the values in the table above. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode to Inverted and/or delay your clock or data relative to the Sample clock.

Refer to Figure 10 for a diagram illustrating the relationship between the exported Sample clock mode and the provided setup and hold times.

Notes: This table assumes the data position is set to Sample clock rising edge and the noninverted Sample clock is exported to the DDC connector with t_{CO} programmed using exported Sample clock offset.

This table includes worst-case effects of channel-to-channel skew and intersymbol interference.

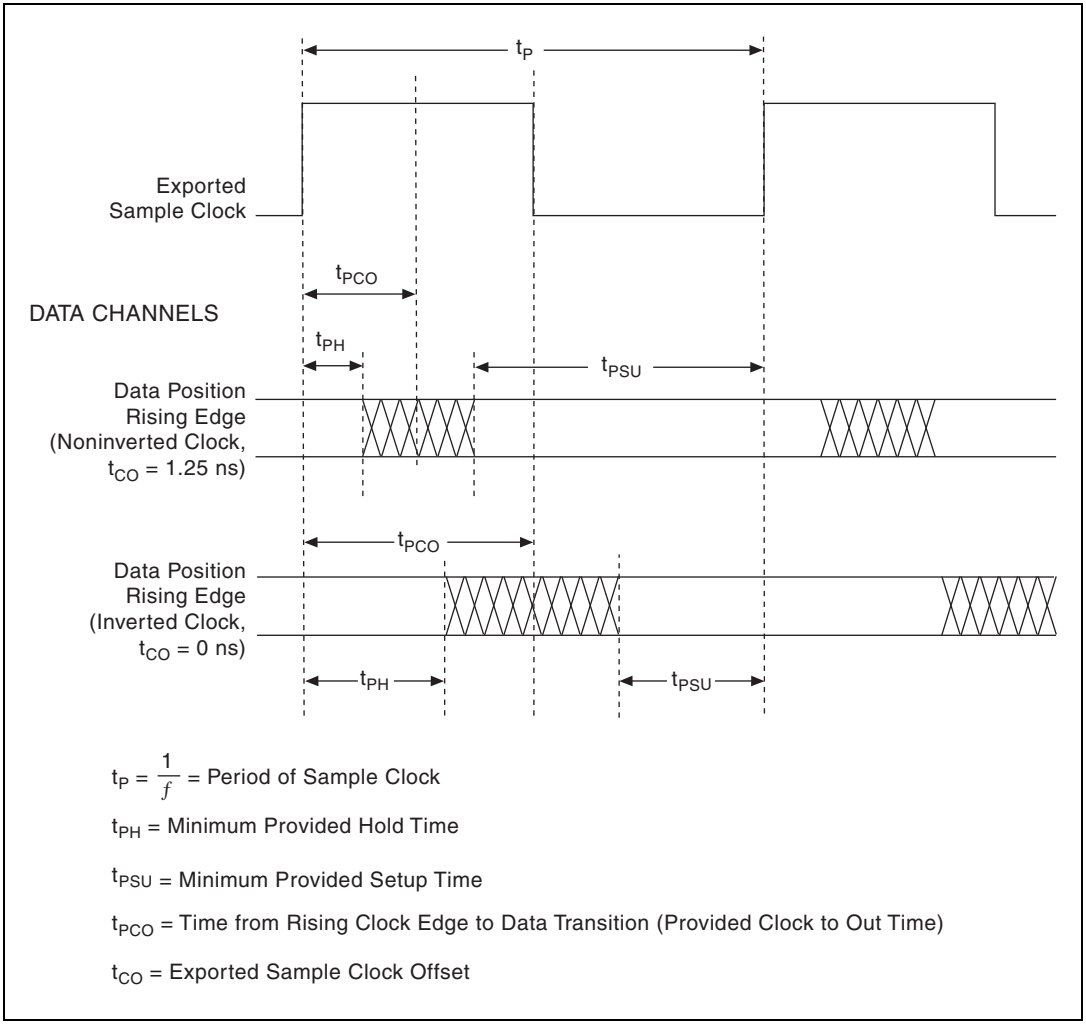
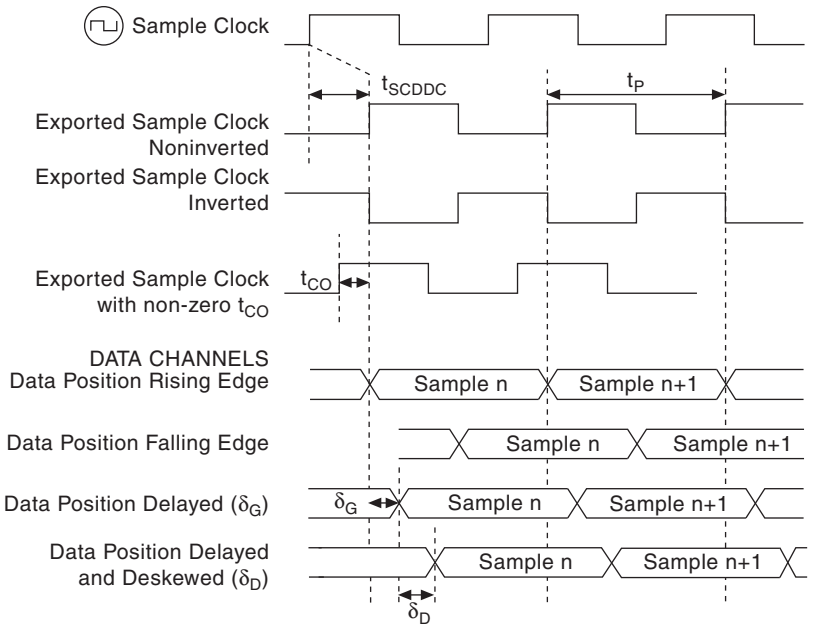


Figure 10. Generation Provided Setup and Hold Times Timing Diagram

Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.



t_{SCDDC} : Time Delay from Sample Clock (Internal) to DDC Connector

$-1 \le \delta_G \le 2$: Pattern Generation Channel Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset

δ_D = Pattern Generation Channel Deskew (Time)

Figure 11. Generation Timing Diagram

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value	Comments
Maximum data rate per channel	200 Mbps	—
Channel-to-channel skew	±300 ps	Maximum skew across all data channels set to the same voltage levels and overdrive. Within ±15 ºC of self-calibration.

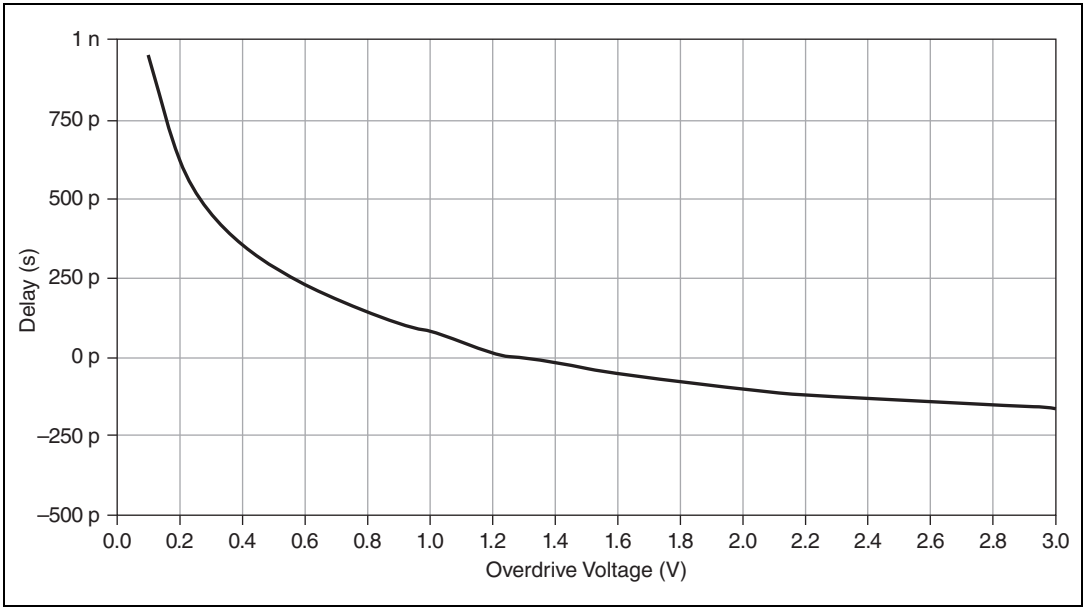


Figure 12. Typical Overdrive Dispersion Adjustment

Note Timing calibration executes with 1.25 V of overdrive.

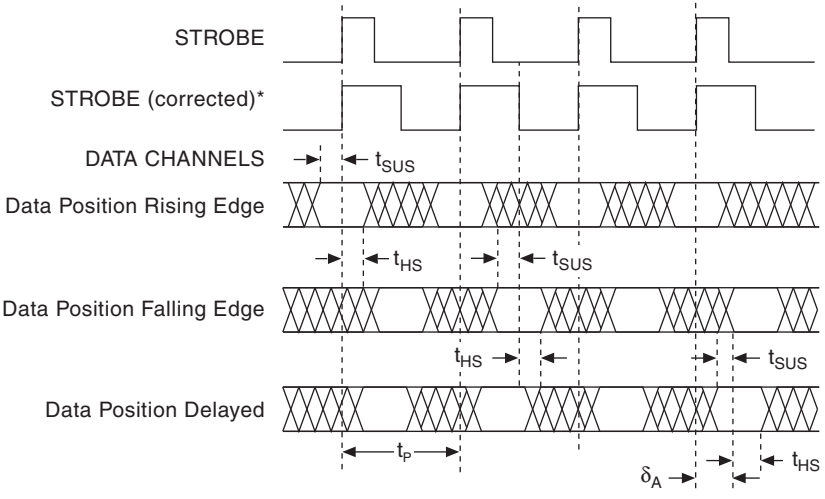
<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Data position modes</td><td colspan="2">Sample clock rising edge
Sample clock falling edge
Delay from Sample clock rising edge</td><td>—</td></tr>
<tr><td rowspan="2">Acquisition data delay and deskew frequency</td><td>On Board Clock</td><td>External Clock</td><td rowspan="2">—</td></tr>
<tr><td>All supported frequencies</td><td>Frequencies ≥ 20 MHz</td></tr>
<tr><td>Acquisition data delay range</td><td colspan="2">–1 to 2 Sample clock cycles expressed as a fraction of the Sample clock period.</td><td rowspan="2">The sum of data delay and data deskew may not exceed –2 to 3 Sample clock cycles.</td></tr>
<tr><td>Acquisition data deskew range</td><td colspan="2">–2 to 3 Sample clock cycles expressed as a time in seconds.</td></tr>
<tr><td>Acquisition data delay and data deskew resolution</td><td colspan="2">30 ps</td><td>—</td></tr>
<tr><td>Acquisition data delay and data deskew linearity accuracy</td><td colspan="2">TBD</td><td>—</td></tr>
<tr><td>Setup time to sample clock (t_{susc})</td><td colspan="2">TBD</td><td rowspan="2">Nominal; does not include channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}.</td></tr>
<tr><td>Hold time to sample clock (t_{HSC})</td><td colspan="2">TBD</td></tr>
<tr><td>Time delay from DDC connector to internal sample clock (t_{DDCSC})</td><td colspan="2">TBD</td><td>Nominal.</td></tr>
</table>

Setup and Hold Times to STROBE

Hold Time to STROBE (t_{HS})		Setup Time to STROBE (t_{SUS})	
f < 20 MHz	f ≥ 20 MHz	f < 20 MHz	f ≥ 20 MHz
1.85 ns	1.50 ns	3.12 ns	1.13 ns

Includes maximum data channel-to-channel skew, but does not include system crosstalk. 1.65 V overdrive on all channels. Overall performance may vary with system crosstalk performance.

Refer to Figure 13 for a diagram illustrating the relationship between the exported Sample clock mode and the setup and hold times to STROBE.



t_{SUS} = Set-Up Time to STROBE

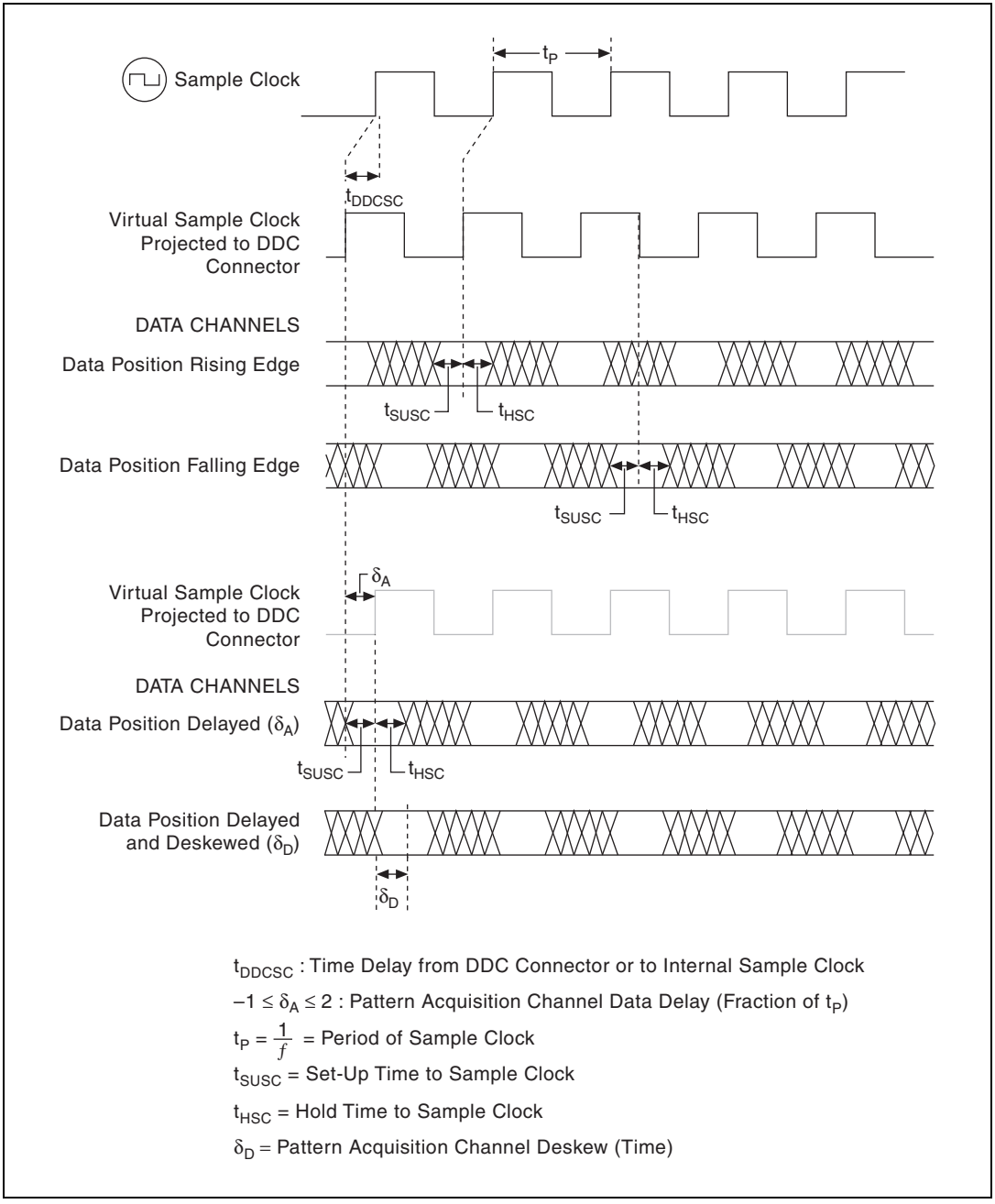
t_{HS} = Hold Time from STROBE

$-1 \le \delta_A \le 2$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

*Note: When using an external Sample clock greater than 20 MHz, the duty cycle is corrected to 50%.

Figure 13. Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{DDCSC} : Time Delay from DDC Connector or to Internal Sample Clock

$-1 \leq \delta_A \leq 2$: Pattern Acquisition Channel Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

δ_D = Pattern Acquisition Channel Deskew (Time)

Figure 14. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE

CLK IN (SMA Jack Connector)

Specification	Value			Comments
Direction	Input into device			—
Destinations	1. Reference clock—for the phase lock loop (PLL) 2. Sample clock			—
Input coupling	AC			—
Input protection	±10 VDC			Nominal.
Input impedance	50 Ω (default) or 1 kΩ			Software-selectable; Nominal.
Minimum detectable pulse width	2 ns			—
Clock requirements	Clock must be continuous and free-running.			—
Clock ranges	**Square Waves**			Nominal 3 dB cutoff point at 125 MHz when using 1 kΩ input impedance.
	Voltage range	300 mV_{pp} to 5.5 V_{pp}		
	Frequency range	20 kHz to 200 MHz		
	Duty cycle range	40% to 60%		
	Sine Waves			—
	Minimum voltage	630 mV_{pp} (0 dBm)	1.265 V_{pp} (6 dBm)	2.53 V_{pp} (12 dBm)
	Maximum voltage	5.5 V_{pp}		
	Minimum frequency	10 MHz	5 MHz	2.5 MHz
	Maximum frequency	200 MHz		

PFI 5 as STROBE (DDC Connector)

Specification	Value	Comments
Direction	Input to device	—
Electrical characteristics	Refer to the *Digital Acquisition Channels (DIO <0..23>, PFI 1, PFI 2, PFI 4, and PFI 5)* specifications in the *Channel Specifications* section.	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	800 Hz to 200 MHz	—
STROBE duty cycle range	40% to 60% for clock frequencies ≥ 20 MHz 25% to 75% for clock frequencies < 20 MHz **Note**: STROBE duty cycle is corrected to 50% at frequencies ≥ 20 MHz.	At the programmed voltage input high (V_{IH}) threshold.
Minimum detectable pulse width	2 ns	
Clock requirements	Clock must be continuous and free-running.	—

PXIe_DStarA (PXI Express Backplane)

Specification	Value	Comments
Direction	Input to device	—
Destinations	1. Reference clock—for the phase lock loop (PLL) 2. Sample clock	—
PXIe_DStarA frequency range	800 Hz to 200 MHz	—
PXIe_DStarA duty cycle range	40% to 60%	—
Clock requirements	Clock must be continuous and free-running.	—

CLK OUT (SMA Jack Connector)

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Direction</td><td colspan="4">Output from device</td><td>—</td></tr>
<tr><td>Sources</td><td colspan="4">1. Sample clock (excluding STROBE)
2. Reference clock (PLL)</td><td>—</td></tr>
<tr><td rowspan="3">Generation voltage level</td><td colspan="2">Low Voltage Levels</td><td colspan="2">High Voltage Levels</td><td rowspan="3">100 µA load.</td></tr>
<tr><td>Characteristic</td><td>Maximum</td><td>Minimum</td><td>Characteristic</td></tr>
<tr><td>0 V</td><td>0.2 V</td><td>3.1 V</td><td>3.3 V</td></tr>
<tr><td>Drive strength</td><td colspan="4">±33 mA</td><td>—</td></tr>
<tr><td>Output impedance</td><td colspan="4">50 Ω</td><td>Nominal.</td></tr>
<tr><td>Output protection</td><td colspan="4">The device can indefinitely sustain a short to any voltage between 0 V and 5 V.</td><td>—</td></tr>
</table>

PFI 4 as DDC CLK OUT (DDC Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock (generation only)	STROBE and acquisition Sample clock cannot be routed to DDC CLK OUT.
Electrical characteristics	Refer to the *Digital Generation Channels (DIO <0..23>, PFI 1, PFI 2, PFI 4, and PFI 5)* specifications in the *Channel Specifications* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK100 (PXI Express backplane) 2. CLK IN (SMA jack connector) 3. PXIe_DStarA (PXI Express backplane) 4. None (internal oscillator locked to an internal reference)	Provides the reference frequency for the PLL.
Reference clock frequency range	5 MHz to 100 MHz (integer multiple of 1 MHz)	—
Reference clock frequency accuracy	±5,000 ppm	Minimum required accuracy of the external Reference clock source.
Lock time	25 ms	Maximum, not including software latency.

Specification	Value	Comments
Reference clock duty cycle range	40% to 60%	—
Reference clock destinations	CLK OUT (SMA jack connector)	—

Waveform Specifications

Memory and Scripting

Specification	Value		Comments
Memory architecture	The NI 6556 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.		Refer to the *Onboard Memory* section in the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size (generation and acquisition)	**NI part number: 781949-01**	**NI part number: 781949-02**	Maximum limit for generation sessions assumes no scripting instructions.
	8 Mbit/channel	64 Mbit/channel	
Generation modes	**Single-waveform mode**: Generate a single waveform once, *n* times, or continuously.		—
	Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.		

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td rowspan="5">Generation minimum waveform size in samples (S)</td><td rowspan="2">Configuration</td><td colspan="2">Sample Rate</td><td rowspan="5">Sample rate dependent. Increasing sample rate increases minimum waveform size requirement. For more information about these configurations, refer to the Common Scripting Use Cases topic in the NI Digital Waveform Generator/ Analyzer Help.</td></tr>
<tr><td>200 MHz</td><td>100 MHz</td></tr>
<tr><td>Single waveform</td><td>1 S</td><td>1 S</td></tr>
<tr><td>Continuous waveform</td><td>128 S</td><td>64 S</td></tr>
<tr><td>Stepped sequence</td><td>128 S</td><td>64 S</td></tr>
<tr><td>Burst sequence</td><td>1056 S</td><td>512 S</td></tr>
<tr><td>Generation finite repeat count</td><td colspan="3">1 to 16,777,216</td><td>—</td></tr>
<tr><td rowspan="2">Generation waveform quantum</td><td colspan="2">Data Width = 4</td><td>Data Width = 2</td><td rowspan="2">—</td></tr>
<tr><td colspan="2">1 sample</td><td>2 samples</td></tr>
</table>

Specification	Value		Comments
Generation waveform block size (in physical memory)	**Data width = 4**	**Data width = 2**	Regardless of waveform size, NI-HSDIO allocates waveforms in blocks of physical memory.
	32 samples	64 samples	
Acquisition minimum record size	1 sample		Regardless of waveform size, NI-HSDIO allocates at least 640 bytes for a record.
Acquisition record quantum	1 sample		—
Acquisition maximum number of records	2,147,483,647		Session should fetch fast enough so that unfetched data is not overwritten.
Acquisition number of pre-Reference trigger samples	0 up to full record		—
Acquisition number of post-Reference trigger samples	0 up to full record		—
Hardware compare error FIFO depth	4,094		—

Specification	Value	Comments
Hardware compare number of unique enable states	255	—
Hardware compare maximum speed	200 MHz	—

Triggers (Inputs to the NI 6556)

Specification	Value	Comments
Trigger types	1. Start trigger 2. Pause trigger 3. Script trigger <0..3> (generation sessions only) 4. Reference trigger (acquisition sessions only) 5. Advance trigger (acquisition sessions only) 6. Stop Trigger (generation sessions only)	—
Sources	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PFI <24..31> (DDC connector) 4. PXI_TRIG<0..7> (PXI Express backplane) 5. Pattern match (acquisition sessions only) 6. Software (user function call) 7. Disabled (do not wait for a trigger)	—
Trigger detection	1. Start trigger (edge detection: rising or falling) 2. Pause trigger (level detection: high or low) 3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low) 4. Reference trigger (edge detection: rising or falling) 5. Advance trigger (edge detection: rising or falling) 6. Stop Trigger (edge detection: rising or falling)	—

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td>Minimum required trigger pulse width</td><td colspan="4">TBD</td><td>—</td></tr>
<tr><td>Destinations</td><td colspan="4">1. PFI 0 (SMA jack connectors)
2. PFI <1..3> (DDC connector)
3. PFI <24..31> (DDC connector)
4. PXI_TRIG<0..6> (PXI Express backplane)</td><td>Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.</td></tr>
<tr><td rowspan="2">Trigger rearm time</td><td>Start to Reference Trigger</td><td>Start to Advance Trigger</td><td>Advance to Advance Trigger</td><td>Reference to Reference Trigger</td><td rowspan="2">Maximum number of samples.</td></tr>
<tr><td>TBD</td><td>TBD</td><td>TBD</td><td>TBD</td></tr>
<tr><td rowspan="2">Delay from Pause trigger to Pause state and Stop trigger to Done state</td><td colspan="2">Generation Sessions</td><td colspan="2">Acquisition Sessions</td><td rowspan="2">Maximum; Use the Data Active event during generation to determine on a sample by sample basis when the device enters the Pause or Done states.</td></tr>
<tr><td colspan="2">TBD</td><td colspan="2">Synchronous with the data</td></tr>
<tr><td>Delay from trigger to digital data output</td><td colspan="4">TBD</td><td>Maximum; Start trigger and Script triggers.</td></tr>
</table>

Events (Generated from the NI 6556)

Specification	Value	Comments
Event type	1. Marker <0..2> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event 4. Ready for Advance event (acquisition sessions only) 5. End of Record event (acquisition sessions only)	—
Destinations	1. PFI 0 (SMA jack connectors) 2. PFI <1..3> (DDC connector) 3. PFI <24..31> (DDC connector) 4. PXI_TRIG<0..6> (PXI Express backplane)	Each event can be routed to any destination, except the Data Active event. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers can be placed at any sample.	—

Miscellaneous

Specification	Value	Comments
Warm-up time	30 minutes	From driver loaded.
External calibration interval	1 year	—

Power

Specification	12 V	3.3 V	Total Power	Comments
Maximum allowed current	5.2 A	5.7 A	—	Maximum allowed power before device shut down requiring reset of the device.
Maximum allowed device power	—	—	76 W	
3.3 V swing at 200 Mbps	4.5 A	4.1 A	67.5 W	Typical results are commensurate with an aggressive user application using all data channels into a high-impedance load with active loads disabled across temperature.
5.0 V swing at 100 Mbps	4.3 A	4.0 A	64.8 W	
8.0 V swing at 50 Mbps	4.3 W	3.8 W	64.1 W	

Physical

Specification	Value	Comments
Dimensions	21.6 × 2.0 × 13.0 cm Dual 3U CompactPCI Express slot; PXI Express compatible	—
Weight	28 oz (793 g)	—

I/O Panel Connectors

Label	Function(s)	Connector Type
CLK IN	External Sample clock, external Reference clock.	SMA jack
PFI 0	Events, triggers.	SMA jack
CLK OUT	External Sample clock, exported Reference clock.	SMA jack

Label	Function(s)	Connector Type
AUX I/O	External force, external sense, and analog calibration.	Combicon
Digital Data & Control (DDC)	Digital data channels, PPMU channels, exported Sample clock, STROBE, events, triggers.	68-pin VHDCI
REMOTE SENSE	PPMU remote sensing channels, external force, external sense, and analog calibration.	68-pin VHDCI

Software

Specification	Value	Comments
Driver software	NI-HSDIO driver software 1.8 or later. NI-HSDIO allows you to configure and control the NI 6556. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI application programming interface (API) guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments (ADEs): • National Instruments LabVIEW • National Instruments LabWindows™/CVI™ • Microsoft Visual C/C++	Refer to the *NI-HSDIO Instrument Driver Readme* for more information about supported ADE versions.
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6556. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 6556 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the NI 6556. The NI 6556 is intended for indoor use only.

Specification	Value	Comments
Operating temperature	0 to +45 ºC in all NI PXI Express and hybrid NI PXI Express chassis. (Meets IEC-60068-2-2.)	—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC 60068-2-56.)	—
Altitude	2,000 m at 25º C ambient temperature	—
Pollution Degree	2	—
Storage temperature	–20 to +70 ºC (Meets IEC-60068-2-2.)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC 60068-2-56.)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Storage shock	50 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Operating vibration	5 Hz to 500 Hz, 0.3 g_{rms} (Meets IEC 60068-2-64.)	—
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	—

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any individual, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications, refer to the *Online Product Certification* section of this document.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

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