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96-Bit and 24-Bit Parallel Digital I/O Interface for PCI, PXI, and CompactPCI

March 2009
374938B-01

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About This Manual

This manual describes the electrical and mechanical aspects of the PCI-DIO-96, PXI-6508, and PCI-6503 and contains information concerning their installation, operation, and programming. The PCI-DIO-96 and PCI-6503 are members of the National Instruments PCI Series of expansion boards for PCI bus computers. The PXI-6508 is a member of the National Instruments PXI family of expansion boards for PXI and CompactPCI chassis. These boards are designed for high-performance data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

Conventions

The following conventions are used in this manual:

<> — Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.

» — The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

 — This icon to the left of bold italicized text denotes a note, which alerts you to important information.

 — This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

bold — Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

italic — Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.
PPI *x*	PPI *x*, where the *x* is replaced by A, B, C, or D, refers to one of the four programmable peripheral interface (PPI) chips on the PCI-DIO-96 or PXI-6508. The PCI-6503 contains only one PPI, PPI A.
Your DIO board	Your DIO board refers to either the PCI-DIO-96, PXI-6508, or PCI-6503 board.

Related Documentation

The following National Instruments document contains information that you may find helpful as you read this manual.

- *Field Wiring and Noise Considerations for Analog Signals*—To access this document, go to `ni.com/info` and enter the info code `rdfwin`.
- *PCI Local Bus Specification*, Revision 2.1
- National Instruments *PXI Specification*, Revision 1.0
- *PICMG 2.0 R2.1 CompactPCI*
- Software documentation—Examples of software documentation you may have are the LabVIEW or LabWindows™/CVI™ documentation sets and the NI-DAQmx or Traditional NI-DAQ (Legacy) documentation. After you set up your hardware system, use either the application software or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.

1 Introduction

This chapter describes the PCI-DIO-96, PXI-6508, and PCI-6503; lists what you need to get started, software programming choices, and optional equipment; describes custom cabling options; and explains how to unpack your board.

About Your Board

Thank you for purchasing a National Instruments PCI-DIO-96, PXI-6508, or PCI-6503 board. The PCI-DIO-96 is a 96-bit, parallel, digital I/O interface for PCI bus computers. The PXI-6508 is a 96-bit, parallel, digital I/O interface for PXI and CompactPCI chassis. The PCI-6503 is a 24-bit, parallel, digital I/O interface for PCI bus computers.

Four 82C55A programmable peripheral interface (PPI) chips control the 96 bits of TTL-compatible digital I/O on the PCI-DIO-96 or PXI-6508. On the PCI-6503, one 82C55A PPI controls the 24 bits of TTL-compatible digital I/O. The 82C55A PPI chips can operate in unidirectional mode, bidirectional mode, or handshaking mode and can generate interrupt requests to your computer. The digital I/O lines are all accessible through a 100-pin female connector on the PCI-DIO-96 or PXI-6508 and a 50-pin male connector on the PCI-6503.

Your DIO board is a completely switchless and jumperless DAQ board. All resource allocation is completed automatically at startup, so you will not need to set interrupt levels or base addresses.

With your DIO board, you can use your computer as a digital I/O system controller for laboratory testing, production testing, and industrial process monitoring and control.

Detailed PCI-DIO-96, PXI-6508, and PCI-6503 specifications are in Appendix A, *Specifications*.

Using PXI with CompactPCI

Using PXI-compatible products with standard CompactPCI products is an important feature provided by the *PXI Specification*, Revision 1.0. If you use a PXI-compatible plug-in device in a standard CompactPCI chassis you can use the basic plug-in device functions, but the PXI-specific functions will be unavailable.

The CompactPCI specification permits vendors to develop sub-buses that coexist with the basic PCI interface on the CompactPCI bus. Compatible operation is not guaranteed between CompactPCI devices with different sub-buses nor between CompactPCI devices with sub-buses and PXI. The standard implementation for CompactPCI does not include these sub-buses. Your PXI-6508 device works in any standard CompactPCI chassis adhering to the *PICMG 2.0 R2.1 CompactPCI* core specification.

What You Need to Get Started

To set up and use your PCI-DIO-96/PXI-6508/PCI-6503 board, you will need the following:

- ❑ PCI-DIO-96, PXI-6508, or PCI-6503 board
- ❑ *PCI-DIO-96/PXI-6508/PCI-6503 User Manual*
- ❑ One of the following software packages and documentation:
  - LabVIEW
  - LabWindows/CVI
  - NI-DAQmx
  - Traditional NI-DAQ (Legacy)
  - Measurement Studio
- ❑ Your computer, or PXI or CompactPCI chassis and controller

Optional Equipment

National Instruments offers a variety of products to use with your DIO board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies
- Connector blocks, 50-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more information about optional equipment available from National Instruments, visit `ni.com`.

Custom Cabling

Caution For compliance with Electromagnetic Compatibility (EMC) requirements, this product must be operated with shielded cables and accessories. If unshielded cables or accessories are used, the EMC specifications are no longer guaranteed unless all unshielded cables and/or accessories are installed in a shielded enclosure with properly designed and shielded input/output ports.

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, the mating connector for the PCI-DIO-96 and PXI-6508 is a 100-position, right-angle receptacle without board locks. Recommended manufacturer part numbers for this mating connector are as follows:

- AMP Corporation (part number 749879-9)
- Honda Corporation (part number PCS-XE100LFD-HS)

The mating connector for the PCI-6503 is a 50-position, polarized ribbon socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connections. Recommended manufacturer part numbers for this mating connector are as follows:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 622-5041)

Unpacking

Your DIO board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. Do *not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

2

Installation and Configuration

This chapter describes how to install and configure your PCI-DIO-96, PXI-6508, or PCI-6503 board.

Software Installation

Before installing your DIO device, you must install the software you plan to use with the device.

If you are a register-level programmer, refer to Appendix B, *Register-Level Programming,* of this manual.

Installing NI-DAQ

The *DAQ Getting Started Guide*, which you can download at `ni.com/manuals`, offers NI-DAQ users step-by-step instructions for installing software and hardware, configuring channels and tasks, and getting started developing an application.

Installing Other Software

If you are using other software, refer to the installation instructions that accompany your software.

Hardware Installation

The following sections contain general installation instructions for each device. Consult your computer or chassis user manual or technical reference manual for specific instructions about installing new devices in your computer or chassis.

Installing the PCI-DIO-96 or PCI-6503

To install a PCI-DIO-96 or PCI-6503 in any available 5 V PCI expansion slot in your computer, complete the following steps:

1. Turn off and unplug your computer.
2. Remove the top cover or access port to the expansion slots.

3. Remove the expansion slot cover on the back panel of the computer.
4. Touch the metal part inside your computer to discharge any static electricity that might be on your clothes or body.
5. Insert the PCI-DIO-96 or PCI-6503 in a 5 V PCI slot. It may be a tight fit, but do *not* force the device into place.
6. Screw the mounting bracket of the PCI-DIO-96 or PCI-6503 to the back panel rail of the computer.
7. Visually verify the installation.
8. Replace the top cover of your computer.
9. Plug in and turn on your computer.

Installing the PXI-6508

To install a PXI-6508 in any available 5 V peripheral slot in your PXI or CompactPCI chassis, complete the following steps:

1. Turn off and unplug your PXI or CompactPCI chassis.
2. Choose an unused PXI or CompactPCI 5 V peripheral slot.
3. Remove the filler panel for the peripheral slot you have chosen.
4. Touch a metal part of your chassis to discharge any static electricity that might be on your clothes or body.
5. Insert the PXI-6508 in the selected 5 V slot. Use the injector/ejector handle to fully inject the device into place.
6. Screw the front panel of the PXI-6508 to the front panel mounting rails of the PXI or CompactPCI chassis.
7. Visually verify the installation.
8. Plug in and turn on the PXI or CompactPCI chassis.

Board Configuration

Your DIO board is completely software configurable. The PCI-DIO-96 and PCI-6503 are fully compliant with the *PCI Local Bus Specification*, Revision 2.1, and the PXI-6508 is fully compliant with the *PXI Specification*, Revision 1.0. Therefore, all board resources are automatically allocated by the PCI system, including the base address and interrupt level. The base address of the board is mapped into PCI memory space. You do not need to perform any configuration steps after the system powers up.

3

Signal Connections

This chapter describes how to make input and output signal connections to your PCI-DIO-96, PXI-6508, and PCI-6503 via the board I/O connector.

Caution Connections that exceed any of the maximum ratings of input or output signals on your DIO board can damage the board and your computer. The description of each signal in this chapter includes information about maximum input ratings. National Instruments is *not* liable for any damages resulting from signal connections that exceed these maximum ratings.

Note For information on adding signal conditioning into your applications and National Instruments signal conditioning devices, go to `ni.com/signalconditioning`.

I/O Connector (PCI-DIO-96, PXI-6508)

The I/O connector for the PCI-DIO-96 and PXI-6508 has 100 pins that you can connect to 50-pin accessories with the R1005050 cable.

I/O Connector Pin Assignments

Figure 3-1 shows the pin assignments for the PCI-DIO-96 and PXI-6508 digital I/O connector.

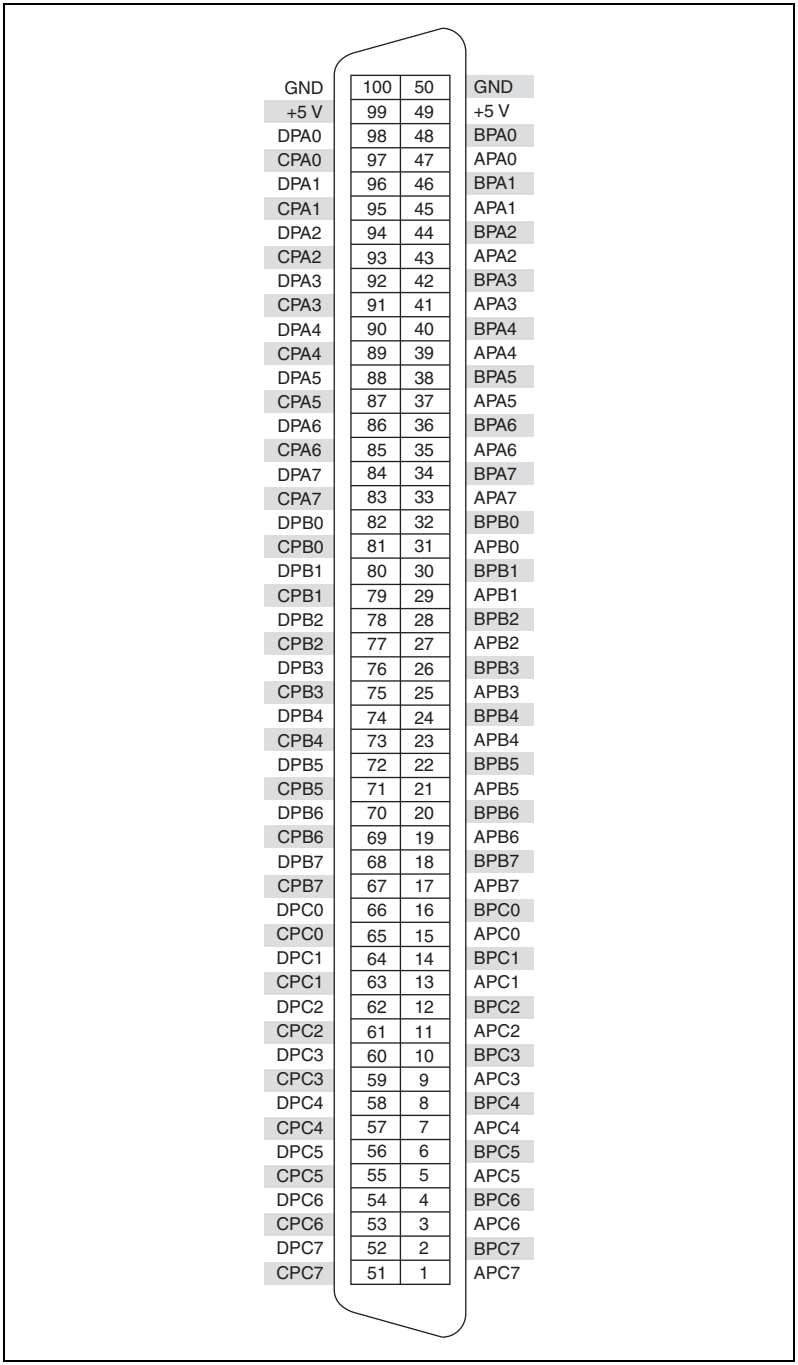


Figure 3-1. PCI-DIO-96 and PXI-6508 Connector Pin Assignments

Cable Assembly Connectors

The optional R1005050 cable assembly you can use with the PCI-DIO-96 or PXI-6508 is an assembly of two 50-pin cables and three connectors. Both cables are joined to a single connector on one end and to individual connectors on the free ends. The 100-pin connector that joins the two cables plugs into the I/O connector of the PCI-DIO-96 and PXI-6508. The other two connectors are 50-pin connectors, one of which is connected to pins 1 through 50 and the other connected to pins 51 through 100 of the PCI-DIO-96 and PXI-6508 connector. Figure 3-2 shows the pin assignments for each of the 50-pin connectors on the cable assembly.

Positions 1–50				Positions 51–100			
APC7	1	2	BPC7	CPC7	1	2	DPC7
APC6	3	4	BPC6	CPC6	3	4	DPC6
APC5	5	6	BPC5	CPC5	5	6	DPC5
APC4	7	8	BPC4	CPC4	7	8	DPC4
APC3	9	10	BPC3	CPC3	9	10	DPC3
APC2	11	12	BPC2	CPC2	11	12	DPC2
APC1	13	14	BPC1	CPC1	13	14	DPC1
APC0	15	16	BPC0	CPC0	15	16	DPC0
APB7	17	18	BPB7	CPB7	17	18	DPB7
APB6	19	20	BPB6	CPB6	19	20	DPB6
APB5	21	22	BPB5	CPB5	21	22	DPB5
APB4	23	24	BPB4	CPB4	23	24	DPB4
APB3	25	26	BPB3	CPB3	25	26	DPB3
APB2	27	28	BPB2	CPB2	27	28	DPB2
APB1	29	30	BPB1	CPB1	29	30	DPB1
APB0	31	32	BPB0	CPB0	31	32	DPB0
APA7	33	34	BPA7	CPA7	33	34	DPA7
APA6	35	36	BPA6	CPA6	35	36	DPA6
APA5	37	38	BPA5	CPA5	37	38	DPA5
APA4	39	40	BPA4	CPA4	39	40	DPA4
APA3	41	42	BPA3	CPA3	41	42	DPA3
APA2	43	44	BPA2	CPA2	43	44	DPA2
APA1	45	46	BPA1	CPA1	45	46	DPA1
APA0	47	48	BPA0	CPA0	47	48	DPA0
+5 V	49	50	GND	+5 V	49	50	GND

Figure 3-2. Cable-Assembly Connector Pinout for the R1005050 Ribbon Cable (PCI-DIO-96 and PXI-6508)

I/O Connector Signal Descriptions

Table 3-1 lists the signal descriptions for the PCI-DIO-96 and PXI-6508 I/O connector pins.

Table 3-1. Signal Descriptions for PCI-DIO-96 and PXI-6508 I/O Connectors

Pin	Signal Name	Alternate Port ID†	Description
1, 3, 5, 7, 9, 11, 13, 15	APC<7..0>	2	Bidirectional data lines for port C of PPI A—APC7 is the MSB, APC0 is the LSB.
2, 4, 6, 8, 10, 12, 14, 16	BPC<7..0>	5	Bidirectional data lines for port C of PPI B—BPC7 is the MSB, BPC0 is the LSB.
17, 19, 21, 23, 25, 27, 29, 31	APB<7..0>	1	Bidirectional data lines for port B of PPI A—APB7 is the MSB, APB0 is the LSB.
18, 20, 22, 24, 26, 28, 30, 32	BPB<7..0>	4	Bidirectional data lines for port B of PPI B—BPB7 is the MSB, BPB0 is the LSB.
33, 35, 37, 39, 41, 43, 45, 47	APA<7..0>	0	Bidirectional data lines for port A of PPI A—APA7 is the MSB, APA0 is the LSB.
34, 36, 38, 40, 42, 44, 46, 48	BPA<7..0>	3	Bidirectional data lines for port A of PPI B—BPA7 is the MSB, BPA0 is the LSB.
49, 99	+5 V supply	—	+5 Volts—These pins are fused for up to 1 A total of +4.65 to +5.25 V.
50, 100	GND	—	Ground—These pins are connected to the computer ground signal.
51, 53, 55, 57, 59, 61, 63, 65	CPC<7..0>	8	Bidirectional data lines for port C of PPI C—CPC7 is the MSB, CPC0 is the LSB.
52, 54, 56, 58, 60, 62, 64, 66	DPC<7..0>	11	Bidirectional data lines for port C of PPI D—DPC7 is the MSB, DPC0 is the LSB.

Table 3-1. Signal Descriptions for PCI-DIO-96 and PXI-6508 I/O Connectors (Continued)

Pin	Signal Name	Alternate Port ID†	Description
67, 69, 71, 73, 75, 77, 79, 81	CPB<7..0>	7	Bidirectional data lines for port B of PPI C—CPB7 is the MSB, CPB0 is the LSB.
68, 70, 72, 74, 76, 78, 80, 82	DPB<7..0>	10	Bidirectional data lines for port B of PPI D—DPB7 is the MSB, DPB0 is the LSB.
83, 85, 87, 89, 91, 93, 95, 97	CPA<7..0>	6	Bidirectional data lines for port A of PPI C—CPA7 is the MSB, CPA0 is the LSB.
84, 86, 88, 90, 92, 94, 96, 98	DPA<7..0>	9	Bidirectional data lines for port A of PPI D—DPA7 is the MSB, DPA0 is the LSB.

† This document refers to the ports as A, B, and C and the PPIs (82C55As) as A, B, C, and D. NI-DAQmx, Traditional NI-DAQ (Legacy), and LabVIEW documentation use numbers to identify each port and PPI. For example, this manual uses PPI A port A to refer to port A of the 82C55A identified as PPI A. NI-DAQmx, Traditional NI-DAQ (Legacy), LabWindows/CVI, LabVIEW, or other application software documentation, however, refer to this port as *0*. The Alternate Port ID column shows the correlation between the different port names.

I/O Connector (PCI-6503)

The PCI-6503 has 50 pins that you can connect to 50-pin accessories with the NB1 cable.

PCI-6503 I/O Connector Pin Descriptions

Figure 3-3 shows the pin assignments for the PCI-6503 digital I/O connector using the NB1 ribbon cable.

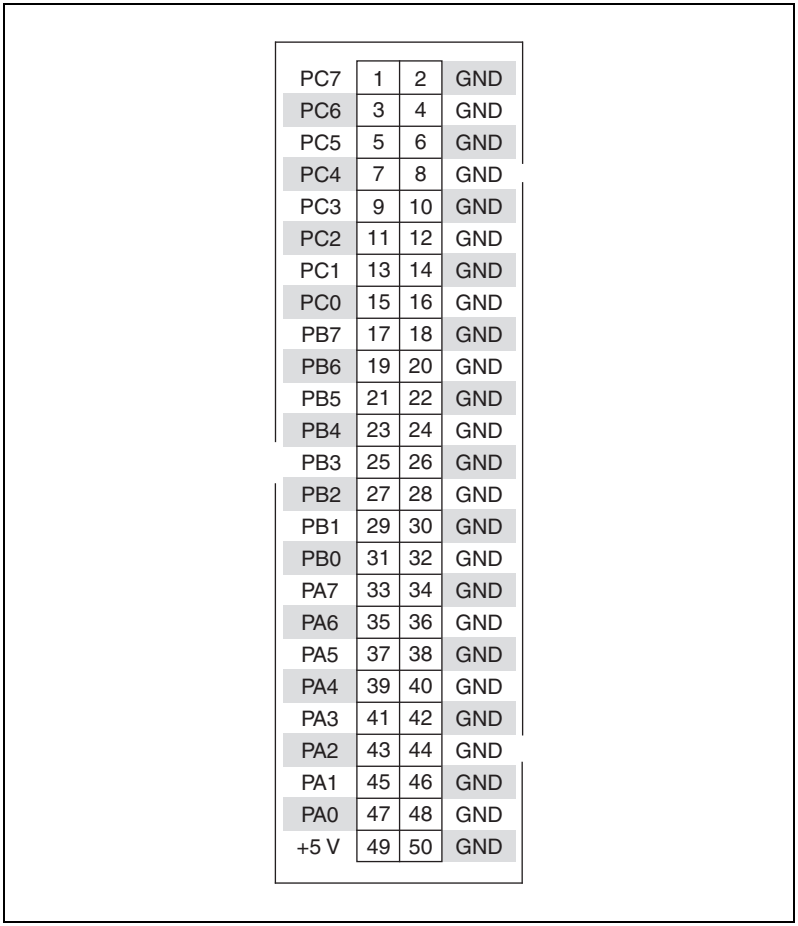


Figure 3-3. PCI-6503 I/O Connector Pin Assignments

Table 3-2 describes the PCI-6503 signals.

Table 3-2. PCI-6503 Signal Descriptions

Pin	Signal Name	Alternate Port ID†	Description
1, 3, 5, 7, 9, 11, 13, 15	PC<7..0>	2	Port C—Bidirectional data lines for port C. PC7 is the MSB, PC0 is the LSB.
17, 19, 21, 23, 25, 27, 29, 31	PB<7..0>	1	Port B—Bidirectional data lines for port B. PB7 is the MSB, PB0 is the LSB.
33, 35, 37, 39, 41, 43, 45, 47	PA<7..0>	0	Port A—Bidirectional data lines for port B. PA7 is the MSB, PA0 is the LSB.
49	+5 V	—	+5 Volts—This pin is fused for up to 1 A at +4.65 to 5.25 V.
All even-numbered pins	GND	—	Ground—These signals are connected to the computer ground reference.

† This document refers to the 82C55 ports as A, B, and C. NI-DAQmx, Traditional NI-DAQ (Legacy), and LabVIEW documentation use numbers to identify ports. For example, this manual uses port A to refer to the first port of the 82C55A. NI-DAQmx, Traditional NI-DAQ (Legacy), LabWindows/CVI, LabVIEW, or other application software documentation, however, refer to this port as *0*. The Alternate Port ID column shows the correlation between the different port names.

Port C Pin Assignments

The signals assigned to port C vary depending on how the 82C55A is configured. In mode 0—or no handshaking configuration—port C is configured as two 4-bit I/O ports. In modes 1 and 2—or handshaking configuration—port C is used for status and handshaking signals with any leftover lines available for general-purpose I/O. Table 3-3 summarizes the port C signal assignments for each configuration. You can also use ports A and B in different modes; the table does not show every possible combination. Consult Appendix B, *Register-Level Programming*, for register-level programming information.

Note Table 3-3 shows both the port C signal assignments and the terminology correlation between different documentation sources. The 82C55A terminology refers to the different 82C55A configurations as modes whereas NI-DAQmx, Traditional NI-DAQ (Legacy), LabWindows/CVI, and LabVIEW documentation refers to them as handshaking and no handshaking. On the PCI-DIO-96 and PXI-6508, these signal assignments are the same for all four 82C55A PPIs. Refer to Table 3-1 for more information.

Table 3-3. Port C Signal Assignments

Configuration Terminology		**Signal Assignments**							
82C55A/ *PCI-DIO-96/ PXI-6508/ PCI-6503 User Manual*	**National Instruments Software**	**APC7, BPC7, CPC7, or DPC7**	**APC6, BPC6, CPC6, or DPC6**	**APC5, BPC5, CPC5, or DPC5**	**APC4, BPC4, CPC4, or DPC4**	**APC3, BPC3, CPC3, or DPC3**	**APC2, BPC2, CPC2, or DPC2**	**APC1, BPC1, CPC1, or DPC1**	**APC0, BPC0, CPC0, or DPC0**
Mode 0 (Basic I/O)	No Handshaking	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 (Strobed Input)	Handshaking	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 (Strobed Output)	Handshaking	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2 (Bidirectional Bus)	Handshaking	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O

Notes: Indicates that the signal is active low.
Subscripts A and B denote port A or port B handshaking signals.

Digital I/O Signal Connections

Pins 1 through 48 and, on the PCI-DIO-96 and PXI-6508, pins 51 through 98 of the I/O connector are digital I/O signal pins. The following specifications and ratings apply to the digital I/O lines. The maximum input logic high and output logic high voltages assume a V_{cc} supply voltage of 5.0 V.

The absolute maximum voltage rating is –0.5 to +5.5 V with respect to GND. For more information on the digital I/O signal specifications, refer to Appendix A, *Specifications*.

Figure 3-4 depicts signal connections for three typical digital I/O applications.

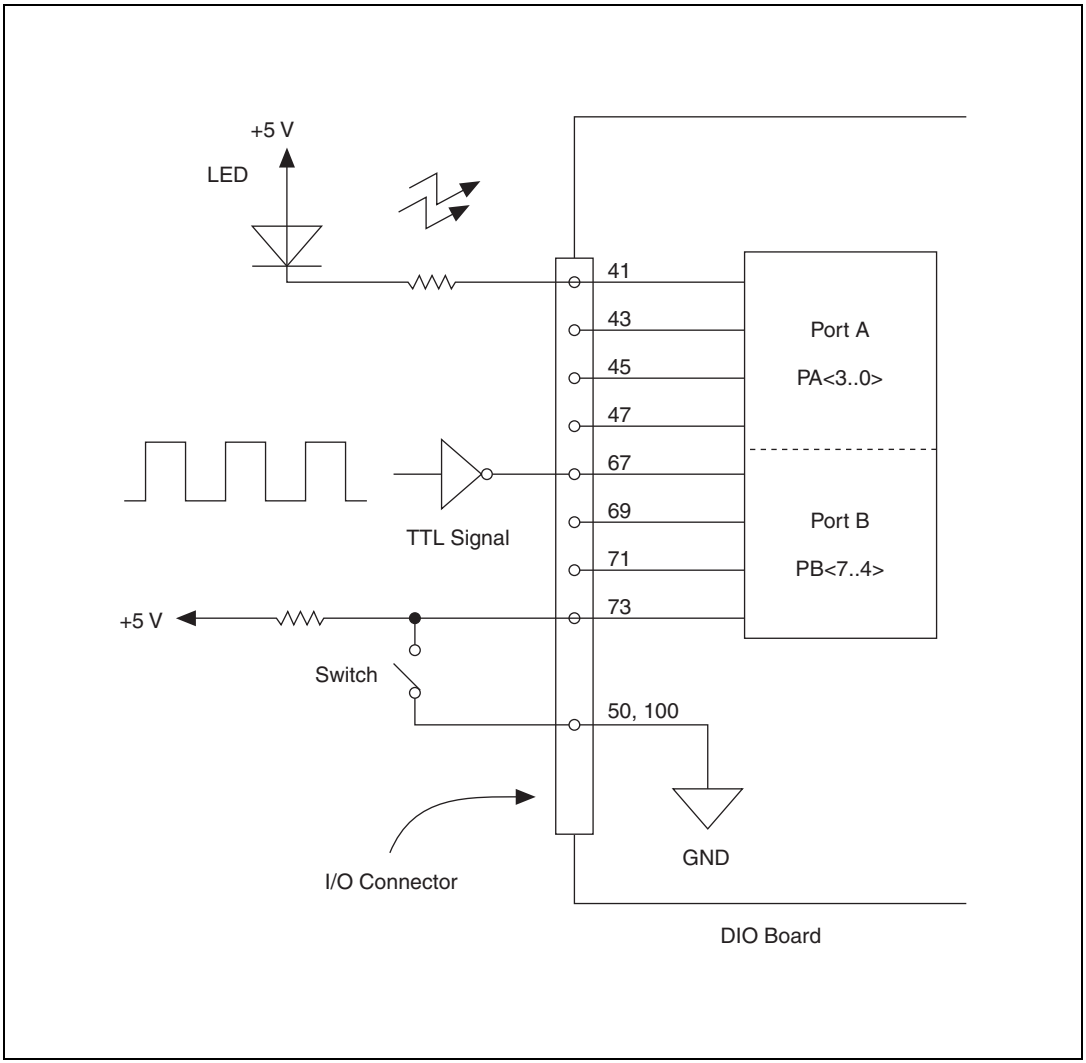


Figure 3-4. Digital I/O Connections Block Diagram

In Figure 3-4, port A of one PPI is configured for digital output, and port B is configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch in Figure 3-4. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 3-4.

Power Connections

Pin 49 and, on the PCI-DIO-96 and PXI-6508, pin 99 of the I/O connector supply +5 V from the computer power supply via a self-resetting fuse. The fuse resets automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to GND and can be used to power external digital circuitry.

Power rating..... 1 A at +4.65 to +5.25 V

Caution Never connect the +5 V power pins directly to ground or to any other voltage source on your DIO board or to any other device. Doing so can damage your DIO board and the computer. National Instruments is *not* liable for damage resulting from such a connection.

Digital I/O Power-up State Selection

The PCI-DIO-96, PXI-6508, and PCI-6503 contain bias resistors that control the state of the digital I/O lines at power up. At power up, each digital I/O line is configured as an input, pulled either high or low by a 100 kΩ bias resistor.

On the PCI-DIO-96, all of the 100 kΩ bias resistors pull up. Therefore, the default power-up state of each line on the PCI-DIO-96 is high.

On the PXI-6508 and PCI-6503, you can select the direction of the 100 kΩ bias resistors. Set jumper W1 to high to configure the resistors as pull-up resistors. Set jumper W1 to low to configure the resistors as pull-down resistors.

You can change individual lines from pulled up to pulled down—or, on the PXI-6508 and PCI-6503, from pulled down to pulled up—by adding your own external resistors. This section describes the procedure.

High DIO Power-up State

If you select the pulled-high mode, each DIO line is pulled to V_{cc} (approximately +5 VDC) with a 100 kΩ resistor. To pull a specific line low, connect between that line and ground a pull-down resistor (R_L) whose value will give you a maximum of 0.4 VDC. The DIO lines provide a maximum of 2.5 mA at 3.7 V in the high state. Using the largest possible resistor ensures that you do not use more current than necessary to perform the pull-down task.

However, ensure the resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-up resistor drives the voltage at the resistor above a TTL low level of 0.4 VDC.

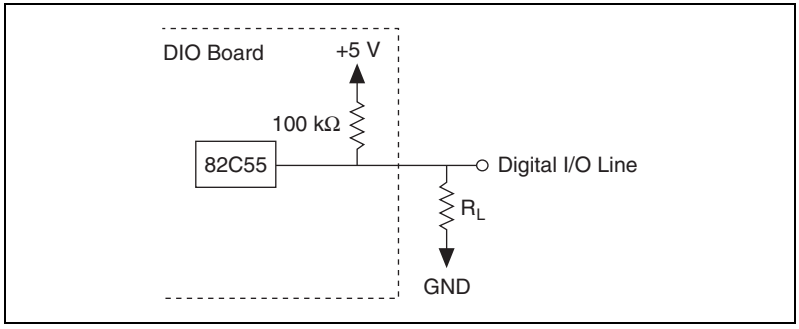


Figure 3-5. DIO Channel Configured for High DIO Power-up State with External Load

Example:

By default, all DIO lines are pulled high at power up. To pull one channel low, complete the following steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the lower the voltage.
2. Using the following formula, calculate the largest possible load to maintain a logic low level of 0.4 V and supply the maximum driving current:

   $V = I \times R_L \Rightarrow R_L = V/I$,

   where $V = 0.4$ V; Voltage across R_L

   $I = 46\ \mu A + 10\ \mu A$; 4.6 V across the 100 kΩ pull-up resistor and 10 µA maximum leakage current(except lines PC0 and PC3)

   therefore $R_L = 7.1$ kΩ; 0.4 V/56 µA

This resistor value, 7.1 kΩ, provides a maximum of 0.4 V on the DIO line at power up. You can substitute smaller resistor values to lower the voltage or to provide a margin for V_{cc} variations and other factors. However, smaller values draw more current, leaving less drive current for other circuitry connected to this line. The 7.1 kΩ resistor reduces the amount of logic high source current by 0.4 mA with a 2.8 V output.

The maximum leakage current on most lines is 10 µA. The maximum leakage current on the PC(0) and PC(3) lines is 20 µA.

Low DIO Power-up State (PXI-6508, PCI-6503 Only)

If you select pulled-low mode, each DIO line will be pulled to GND (0 VDC) using a 100 kΩ resistor. If you want to pull a specific line high, connect a pull-up resistor that will give you a minimum of 2.8 VDC. The DIO lines are capable of sinking a maximum of 2.5 mA at 0.4 V in the low state. Using the largest possible resistance value ensures that you do not use more current than necessary to perform the pull-up task.

Also, ensure the pull-up resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-down resistor brings the voltage at the resistor below a TTL high level of 2.8 VDC.

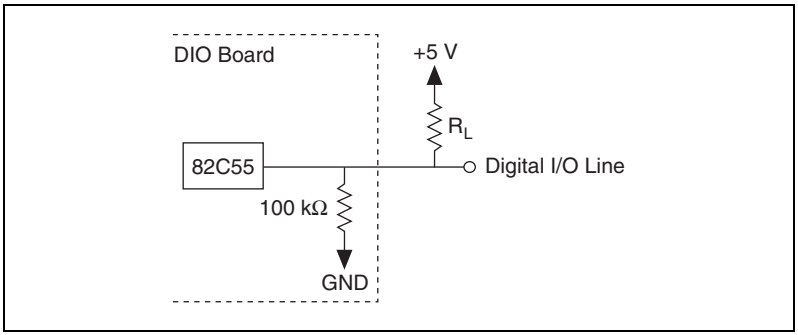


Figure 3-6. DIO Channel Configured for Low DIO Power-up State with External Load

Example:

Set jumper W1 to low, which means all DIO lines are pulled low at power up. To pull one channel high, complete the following steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the higher the voltage.
2. Using the following formula, calculate the largest possible load to maintain a logic high level of 2.8 V and supply the maximum sink current:

   $V = I \times R_L \Rightarrow R_L = V/I$

   where $V = 2.2$ V; Voltage across R_L

   $I = 28\ \mu A + 10\ \mu A$; 2.8 V across the 100 kΩ pull-up resistor and 10 µA maximum leakage current (except lines PC0 and PC3)

   therefore $R_L = 5.7$ kΩ; 2.2 V/38 µA

This resistor value, 5.7 kΩ, provides a maximum of 2.8 V on the DIO line at power up. You can substitute smaller resistor values to lower the voltage drop or to provide a margin for V_{CC} variations and other factors. However, smaller values draw more current, leaving less sink current for other circuitry connected to this line. The 5.7 kΩ resistor reduces the amount of a logic low sink current by 0.8 mA with a 0.4 V output.

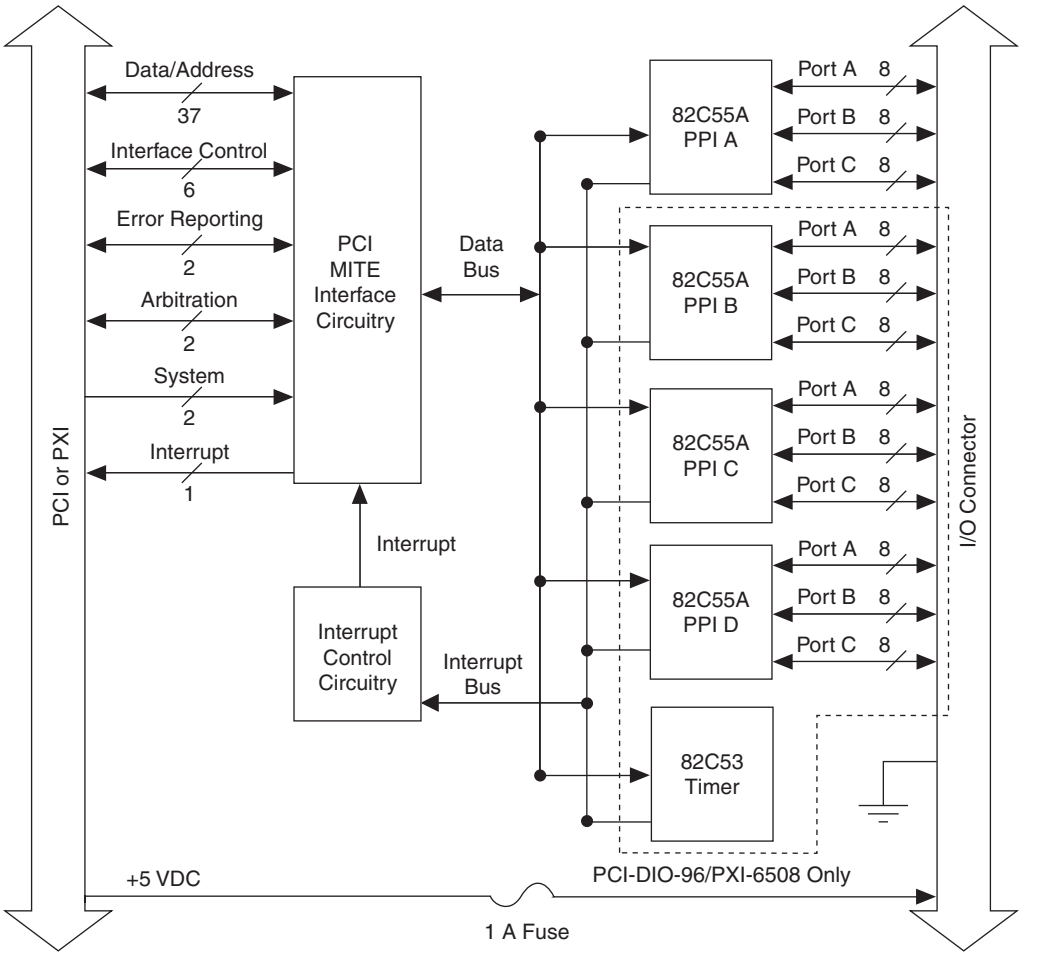
4

Theory of Operation

This chapter contains a functional overview of the PCI-DIO-96, PXI-6508, and PCI-6503 and explains the operation of each functional unit.

Functional Overview

The block diagram in Figure 4-1 illustrates the key functional components of your DIO board.



Note: Current revisions of the NI PCI-DIO-96 and PXI-6508 no longer support the OKI 82C53 programmable interval timer. If you are using a PCI-DIO-96 revision G or earlier or PXI-6508 revision D or earlier, refer to Appendix B, *Register-Level Programming*, for more information about using the 82C53.

Figure 4-1. PCI-DIO-96/PXI-6508 Block Diagram

PCI Interface Circuitry

Your DIO board uses the PCI MITE ASIC to communicate with the PCI bus. The PCI MITE ASIC was designed by National Instruments specifically for data acquisition. The PCI MITE is fully compliant with *PCI Local Bus Specification*, Revision 2.1.

The base memory address and interrupt level for the board are stored inside the PCI MITE at power on. You do not need to set any switches or jumpers.

82C55A Programmable Peripheral Interface

The 82C55A PPI chip is the heart of your DIO board. The PCI-DIO-96 and PXI-6508 contain four PPIs. The PCI-6503 contains one PPI. Each of these chips has 24 programmable I/O pins that represent three 8-bit ports: PA, PB, and PC. Each port can be programmed as an input or output port. The 82C55A has three modes of operation: simple I/O (mode 0), strobed I/O (mode 1), and bidirectional I/O (mode 2). In modes 1 and 2, the three ports are divided into two groups: group A and group B. Each group has eight data bits, plus control and status bits from port C (PC). Modes 1 and 2 use handshaking signals from the computer to synchronize data transfers. Refer to Appendix B, *Register-Level Programming*, for more detailed information.

Different revisions of the PCI-DIO-96, PXI-6508, and PCI-6503 use different 82C55A chips from Intersil Corporation or OKI Semiconductor. For the most recent data sheet for the Intersil CMS82C55A or CS82C55A, visit `www.intersil.com`. For the most recent data sheet for the OKI MSM82C55A, visit `www2.okisemi.com`.

Table 4-1 describes the 82C55A used in the PCI-DIO-96, PXI-6508, and PCI-6503.

Table 4-1. The 82C55A Chips Used in the PCI-DIO-96, PXI-6508, and PCI-6503

Type	Bus Hold†	PCI-DIO-96	PXI-6508	PCI-6503
Intersil CMS82C55A	No	Revision K or later	Revision G or later	Revision G or later
Intersil CS82C55A	Yes	182920H-01	184836E-01	185183E-01
OKI MSM82C55A	No	182920J-01, revision G or earlier	184836F-01, revision D or earlier	185183F-01, revision D or earlier

† Indicates whether the chip has the bus hold feature on the port pins.

Timing Specifications

This section lists the timing specifications for handshaking with your DIO board. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

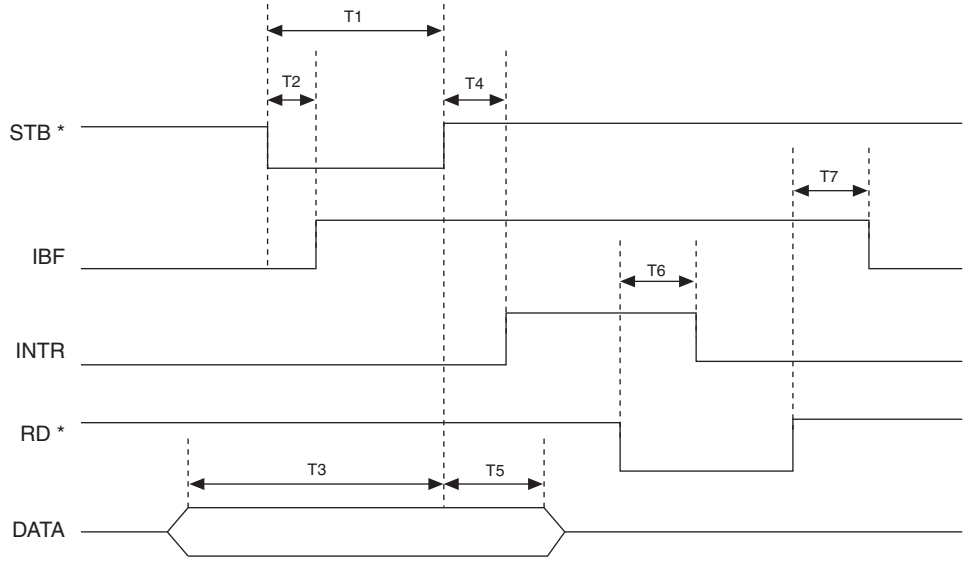
Table 4-2 describes signals appearing in the handshaking diagrams.

Table 4-2. Signal Names Used in Timing Diagrams

Name	Type	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. A low signal indicates the board is ready for more data. This is an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written to the port has been accepted. This signal is a response from the external device indicating that it has received the data from your DIO board.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written to the port.
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A requests service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal.
RD*	Internal	Read—This signal is the read signal generated from the control lines of the computer I/O expansion bus.
WR*	Internal	Write—This signal is the write signal generated from the control lines of the computer I/O expansion bus.
DATA	Bidirectional	Data Lines at the Specified Port—For output mode, this signal indicates the availability of data on the data line. For input mode, this signal indicates when the data on the data lines should be valid.

Mode 1 Input Timing

Figure 4-2 shows the timing specifications for an input transfer in mode 1.



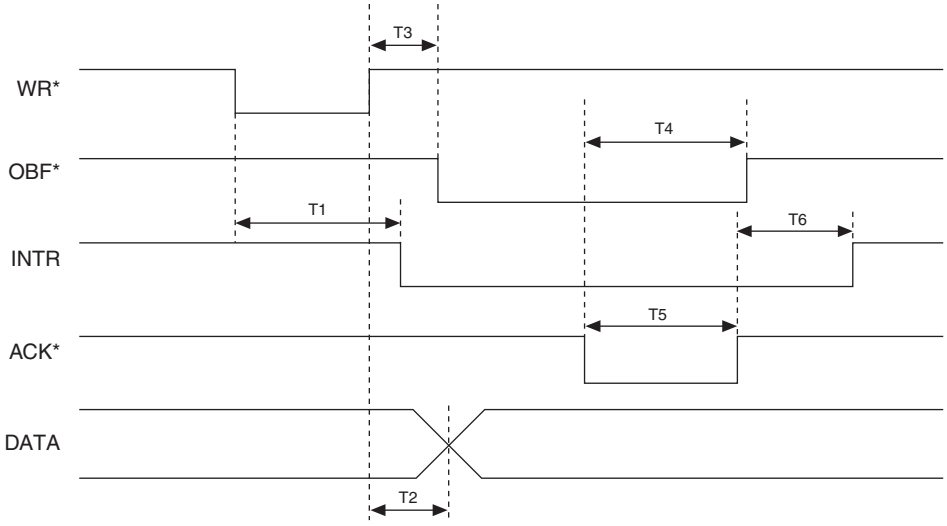
Name	Description	Minimum†	Maximum†
T1	STB* Pulse Width	100	—
T2	STB* = 0 to IBF = 1	—	150
T3	Data before STB* = 1	20	—
T4	STB* = 1 to INTR = 1	—	150
T5	Data after STB* = 1	50	—
T6	RD* = 0 to INTR = 0	—	200
T7	RD* = 1 to IBF = 0	—	150

† All timing values are in nanoseconds.

Figure 4-2. Timing Specifications for Mode 1 Input Transfer

Mode 1 Output Timing

Figure 4-3 shows the timing specifications for an output transfer in mode 1.



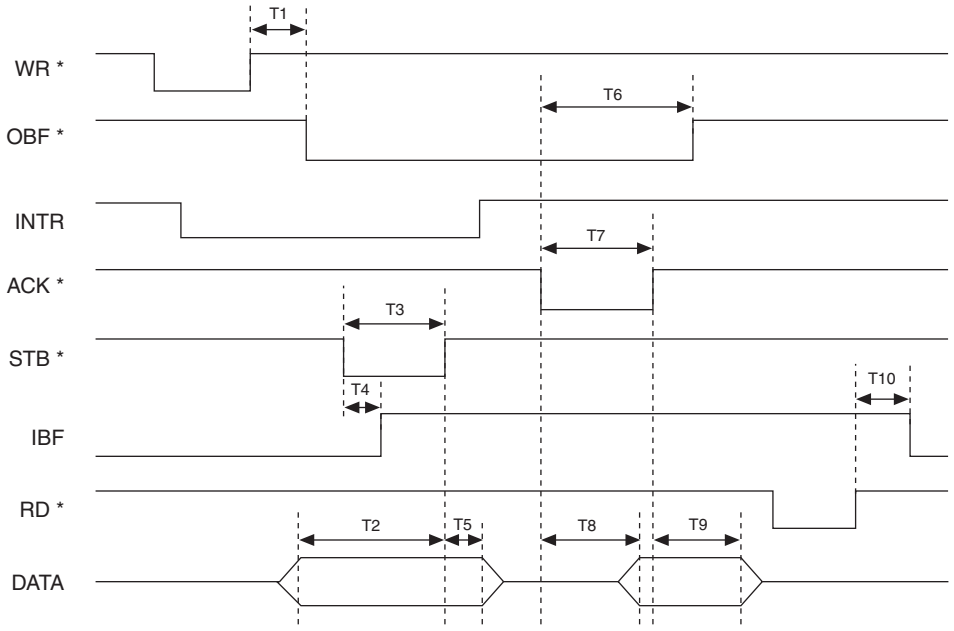
Name	Description	Minimum†	Maximum†
T1	WR* = 0 to INTR = 0	—	250
T2	WR* = 1 to Output	—	200
T3	WR* = 1 to OBF* = 0	—	150
T4	ACK* = 0 to OBF* = 1	—	150
T5	ACK* Pulse Width	100	—
T6	ACK* = 1 to INTR = 1	—	150

† All timing values are in nanoseconds.

Figure 4-3. Timing Specifications for Mode 1 Output Transfer

Mode 2 Bidirectional Timing

Figure 4-4 shows the timing specifications for bidirectional transfers in mode 2.



Name	Description	Minimum†	Maximum†
T1	WR* = 1 to OBF* = 0	—	150
T2	Data before STB* = 1	20	—
T3	STB* Pulse Width	100	—
T4	STB* = 0 to IBF = 1	—	150
T5	Data after STB* = 1	50	—
T6	ACK* = 0 to OBF* = 1	—	150
T7	ACK* Pulse Width	100	—
T8	ACK* = 0 to Output	—	150
T9	ACK* = 1 to Output Float	20	250
T10	RD* = 1 to IBF = 0	—	150

† All timing values are in nanoseconds.

Figure 4-4. Timing Specifications for Mode 2 Bidirectional Transfer

A

Specifications

This appendix lists the specifications for the PCI-DIO-96, PXI-6508, and PCI-6503. These specifications are typical at 25 °C unless otherwise noted.

Digital I/O

Number of channels

PCI-DIO-96 and PXI-6508 ..... 96 I/O

PCI-6503 ..... 24 I/O

Compatibility ..... TTL

Power on state

PCI-DIO-96 ..... Inputs (high-Z), pulled up through 100 kΩ

PXI-6508, PCI-6503 ..... Inputs (high-Z), pulled up or down through 100 kΩ (jumper selectable)

Handshaking..... Input, output, or bidirectional

Data transfers ..... Interrupts, programmed I/O

Digital Logic Levels

Input Signals

The maximum input logic high and output logic high voltages assume a V_{cc} supply voltage of 5.0 V. Given a V_{cc} supply voltage of 5.0 V, the absolute maximum voltage rating for each I/O line is –0.5 V to 5.5 V with respect to GND.

Level	Min	Max
Input logic high voltage	2.2 V	5.3 V
Input logic low voltage	–0.3 V	0.8 V
Input high current (V_{in} = 5 V, resistors set to pull-up†)	—	10 µA‡
Input high current (V_{in} = 5 V, resistors set to pull-down†)	—	75 µA
Input logic low current (V_{in} = 0 V, resistors set to pull-up†)	—	–75 µA
Input logic low current (V_{in} = 0 V, resistors set to pull-down†)	—	–10 µA‡

† The PCI-DIO-96 bias resistors are always set to pull-up. On the PXI-6508 and PCI-6503, use jumper W1 to select pull-up or pull-down.

‡ Exception: Lines PC3 and PC0 are 20 µA.

Output Signals

Pin 49 (at +5 V) .....1.0 A max

Level	Min	Max
Output logic high voltage (I_{ol} = –2.5 mA)	3.0 V	5.0 V
Output logic high voltage (I_{oh} = –4 mA)	2.7 V	5.0 V
Output logic low voltage (I_{ol} = 2.5 mA)	0 V	0.4 V
Output logic low voltage (I_{ol} = 4 mA)	0 V	0.5 V

Output current.....2.5 mA typ

Caution Drawing more than the typical 2.5 mA current (<2 kΩ load at 5 V output) can cause serious damage to the device 82C55 PPI. The 82C55 PPI is intended for use as a logic device, and should not be used as current driver for LEDs, SSRs, mechanical relays, and so on, which can have low impedance loads and/or require high current drive. If you require higher current drive, consider using the NI PCI/PXI-6509 5V/TTL 96-line Industrial DIO board with 24 mA current driver, using an NI PCI/PXI-651*x* high-current drive Industrial DIO board, or using external circuitry such as Darlington Arrays to increase the current drive of digital output lines. For more information about the breakdown levels of your device and for a link to the 82C55 data sheets, refer to `ni.com/info` and enter the info code `82c55`.

Transfer Rates

Max with NI-DAQ software ..... 50 kbytes/s

Constant sustainable rate (typ)..... 1 to 10 kbytes/s

Transfer rates are a function of the speed with which your program reads data from or writes data to the board, and therefore vary with your system, software, and application. The following primary factors control your DIO board transfer rates:

- Computer system performance
- Programming environment (register-level programming or NI-DAQ)
- Programming language and code efficiency
- Execution mode (foreground or background, with background execution typically using interrupts)
- Other operations in progress
- Application

For example, you can obtain higher transfer rates in a handshaking or data-transfer application, requiring an average rate, than in a pattern generation, data acquisition, or waveform generation application, requiring a constant sustainable rate.

The maximum rate shown was obtained using a 233 MHz Pentium computer running Traditional NI-DAQ (Legacy) and LabWindows/CVI software, with interrupt-based execution, and with no other high-speed operations in progress.

Bus Interface

Type ..... Slave

Power Requirement

Power consumption..... 400 mA at +5 VDC (±5%)

Power available at I/O connector..... +4.65 to +5.25 V fused at 1 A

Physical

Dimensions

PCI-DIO-96 ..... 13.7 × 10.7 cm (5.4 × 4.2 in.)
PXI-6508 ..... 17.5 × 10.7 cm (6.9 × 4.2 in.)
PCI-6503..... 12.2 × 9.5 cm (4.8 × 3.7 in.)

Weight

PCI-DIO-96 ..... 101 g (3.6 oz)
PXI-6508 ..... 148 g (5.2 oz)
PCI-6503..... 55 g (1.9 oz)

I/O connector

PCI-DIO-96 and PXI-6508..... 100-pin female 0.050 series D-type
PCI-6503..... 50-pin male ribbon-cable connector

Environment

If you need to clean the module, use a soft, non-metallic brush.

Operating temperature ..... 0 to 55 °C

Storage temperature ..... –20 to 70 °C

Relative humidity ..... 5% to 90%, noncondensing

Maximum altitude..... 2,000 meters

Pollution Degree 2

Indoor use only.

Shock and Vibration

Functional shock (PXI-6508)..... MIL-T-28800 E Class 3 (per Section 4.5.5.4.1); half-sine shock pulse, 11 ms duration, 30 g peak, 30 shocks per face

Operational random vibration (PXI-6508) ..... 5 to 500 Hz, 0.31 grms, 3 axes

Nonoperational random vibration (PXI-6508) ..... 5 to 500 Hz, 2.5 grms, 3 axes

Note Random vibration profiles were developed in accordance with MIL-T-28800E and MIL-STD-810E Method 514. Test levels exceed those recommended in MIL-STD-810E for Category 1 (Basic Transportation, Figures 514.4-1 through 514.4-3).

Safety

The PCI-DIO-96/PXI-6508/PCI-6503 meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit `ni.com/environment/weee.htm`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

B

Register-Level Programming

This appendix describes in detail the address and function of each PCI-DIO-96, PXI-6508, and PCI-6503 register, contains instructions on how to operate DIO board circuitry, and provides examples of the programming steps necessary to execute an operation.

Note Current revisions of the NI PCI-DIO-96 and PXI-6508 no longer support the OKI 82C53 programmable interval timer. If you are using a PCI-DIO-96 revision G or earlier or PXI-6508 revision D or earlier, refer to the information in this appendix.

Note If you plan to use a programming software package such as LabVIEW, LabWindows/CVI, NI-DAQmx, or Traditional NI-DAQ (Legacy) with your DIO board, you need not read this appendix.

While it is possible to program your DAQ device at the register level, National Instruments strongly recommends using NI-DAQmx, Traditional NI-DAQ (Legacy), or driver software and application development software such as LabVIEW, Measurement Studio for Visual Studio .NET, or LabWindows/CVI to program your NI PCI-DIO-96, PXI-6508, and PCI-6503 device for improved productivity. NI-DAQmx and Traditional NI-DAQ (Legacy) software provides easier programming with the same flexibility as register-level programming.

NI-DAQmx and Traditional NI-DAQ (Legacy) driver software will not work for your programming needs in some cases, however. For example, if you are programming your 82C53 for hardware-timed interrupts or you are programming your DAQ device in an OS that is unsupported in NI-DAQmx or Traditional NI-DAQ (Legacy), NI-DAQmx Base software could be used as an alternative. If your OS is also unsupported in NI-DAQmx Base, you would then need to program your device using this appendix.

The NI Measurement Hardware Driver Development Kit (MHDDK) provides register-level programming examples and a bus interface for many operating systems. The MHDDK is a good starting point for developing a custom driver. You will also need the register map in this appendix. Note that some advanced functionalities such as interrupts are only covered in the examples in this appendix and not in the MHDDK examples. To access this document, go to `ni.com/info` and enter the info code `mhddk`.

82C53 Programmable Interval Timer (PCI-DIO-96, PXI-6508 Only)

The PCI-DIO-96 and PXI-6508 contain an 82C53 programmable interval timer for use by register-level programmers only. The 82C53 programmable interval timer can generate timed interrupt requests to your computer. The 82C53 has three 16-bit counters, which can each be used in one of six different modes. The PCI-DIO-96 and PXI-6508 can use two of the counters to generate interrupt requests; the third counter is not used and is not accessible. Refer to the *Programming Considerations for the 82C53* section for more detailed information.

Interrupt Control Circuitry

Two software-controlled registers determine which devices, if any, generate interrupts. Each of the 82C55A devices has two interrupt lines, PC3 and PC0, connected to the interrupt circuitry. On the PCI-DIO-96 and PXI-6508, the 82C53 device has two of its three counter outputs connected to the interrupt circuitry. Any of these 10 signals can interrupt the computer if the interrupt circuitry is enabled and the corresponding enable bit is set. Refer to the *Programming Considerations for the 82C53* section for more information. Normally, the handshaking circuitry controls PC3 and PC0 of the 82C55A devices; however, you can configure either of these two lines for input and then use them as external interrupts. An interrupt occurs on the signal line low-to-high transition.

Refer to the *Programming Considerations for the 82C53* section for more detailed information concerning interrupts.

The block diagram in Figure B-1 illustrates the interrupt control circuitry.

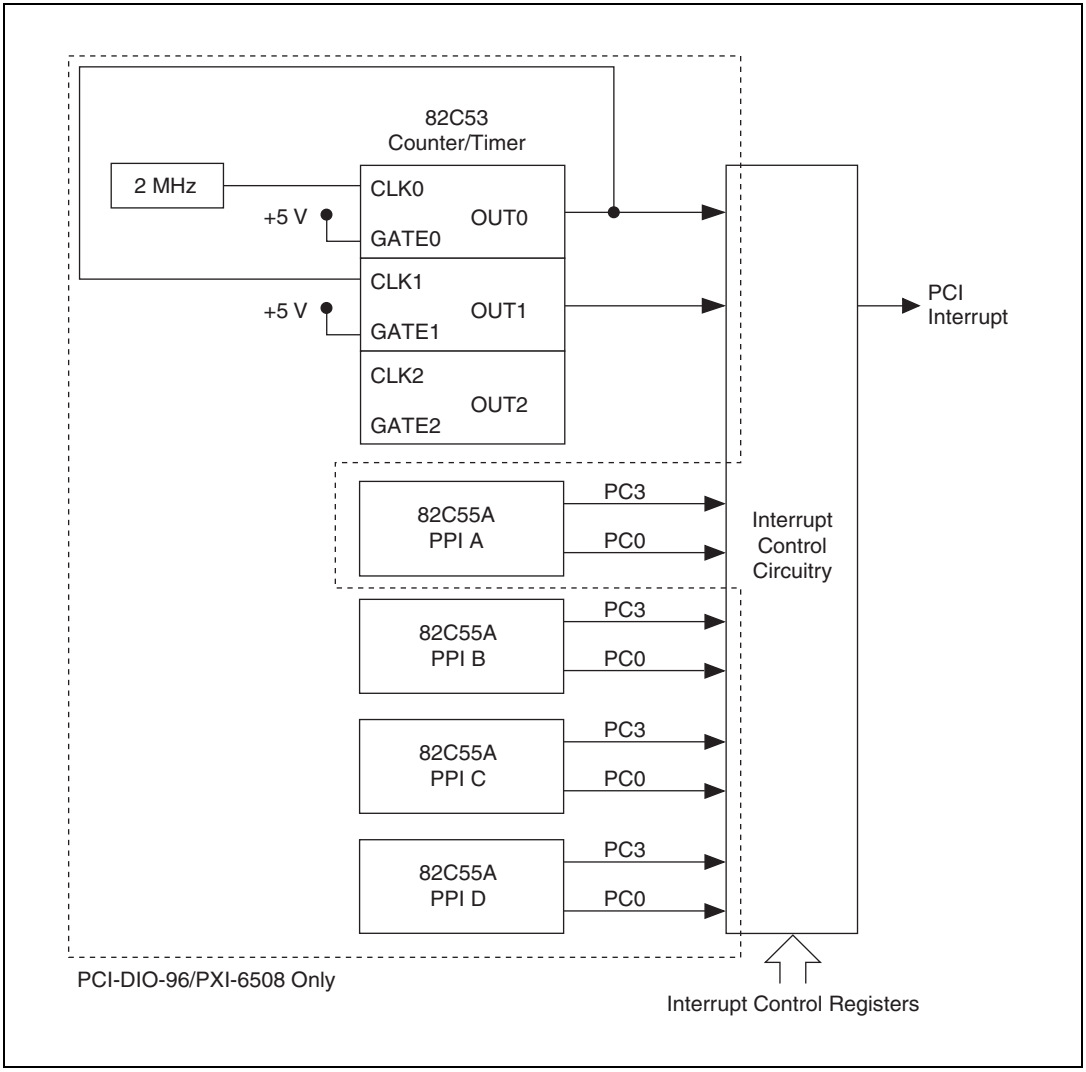


Figure B-1. Interrupt Control Circuitry Block Diagram

Register Map and Description

This section describes in detail the address and function of each PCI-DIO-96, PXI-6508, and PCI-6503 register.

Introduction

The three 8-bit ports of the 82C55A are divided into two groups of 12 signals: group A and group B. One 8-bit control word selects the mode of operation for each group. The group A control bits configure port A (A<7..0>) and the upper 4 bits (nibble) of port C (C<7..4>). The group B control bits configure port B (B<7..0>) and the lower nibble of port C (C<3..0>). These configuration bits are defined in the *Register Description for the 82C55A* section. When differentiation is required between the four 82C55A PPI devices on the PCI-DIO-96 and PXI-6508, they are referenced as PPI A, PPI B, PPI C, and PPI D.

On the PCI-DIO-96 and PXI-6508, the three 16-bit counters of the 82C53 are accessed through individual data ports and controlled by one 8-bit control word. The control word selects how the counter data ports are accessed and what mode the counter uses. The *Register Description for the 82C53 (PCI-DIO-96, PXI-6508 Only)* section contains definitions for these configuration bits.

In addition to the 82C55A and 82C53 devices, there are two registers that select which onboard signals are capable of generating interrupts. There are two interrupt signals from each of the 82C55A devices and two interrupt signals from the 82C53 device. Individual enable bits select which of these 10 signals can generate interrupts. Also, a master enable signal determines whether the board can actually send a request to the computer. The *Register Description for the Interrupt Control Registers* section contains definitions for the configuration bits for these registers.

Register Map

Table B-1 lists the address map for your DIO board. The PCI-DIO-96 and PXI-6508 use all of the registers. The PCI-6503 uses a subset of the registers, as indicated in the table.

Table B-1. Register Address Map

Register Name	Offset Address (Hex)	Size	Type	Present on the PCI-6503
82C55A Register Group				
PPI A				
PORTA Register	00	8-bit	Read-and-write	Yes
PORTB Register	01	8-bit	Read-and-write	Yes
PORTC Register	02	8-bit	Read-and-write	Yes
Configuration Register	03	8-bit	Write-only	Yes
82C55A Register Group (Continued)				
PPI B				
PORTA Register	04	8-bit	Read-and-write	No
PORTB Register	05	8-bit	Read-and-write	No
PORTC Register	06	8-bit	Read-and-write	No
Configuration Register	07	8-bit	Write-only	No
PPI C				
PORTA Register	08	8-bit	Read-and-write	No
PORTB Register	09	8-bit	Read-and-write	No
PORTC Register	0A	8-bit	Read-and-write	No
Configuration Register	0B	8-bit	Write-only	No
PPI D				
PORTA Register	0C	8-bit	Read-and-write	No
PORTB Register	0D	8-bit	Read-and-write	No
PORTC Register	0E	8-bit	Read-and-write	No
Configuration Register	0F	8-bit	Write-only	No
82C53 Register Group				
Counter 0	10	8-bit	Read-and-write	No
Counter 1	11	8-bit	Read-and-write	No
Configuration Register	13	8-bit	Write-only	No
Interrupt Control Register Group				
Register 1	14	8-bit	Write-only	Yes
Register 2	15	8-bit	Write-only	Yes
Interrupt Clear Register	16	8-bit	Write-only	No

Register Descriptions

The following sections contain the register descriptions for the devices used on your DIO board. The register description bits labeled with an *X* indicate reserved bits. Always write a 0 to these bits.

Register Description Format

This section discusses each of the DIO board registers in the order shown in Table B-1. Each register group is introduced, followed by a detailed bit description of each register. Individual register descriptions give the address (in hexadecimal), type, data size, and bit map of the register, followed by a description of each bit.

The register bit map shows a diagram of the register with the MSB (bit 7) shown on the left, and the LSB (bit 0) shown on the right. A rectangle with the bit name inside represents each bit.

The bit map for the Interrupt Clear Register states *not applicable, no bits used*. The data is ignored when you write to this register; therefore, any bit pattern is sufficient.

Register Description for the 82C55A

Figure B-2 shows the two control word formats used to completely program the 82C55A. The control word flag (bit 7) determines which control word format is being programmed. When the control word flag is 1, bits 6 through 0 select the I/O characteristics of the 82C55A ports. These bits also select the mode in which the ports are operating; that is, mode 0, mode 1, or mode 2. When the control word flag is 0, bits 3 through 0 select the bit set/reset format of port C.

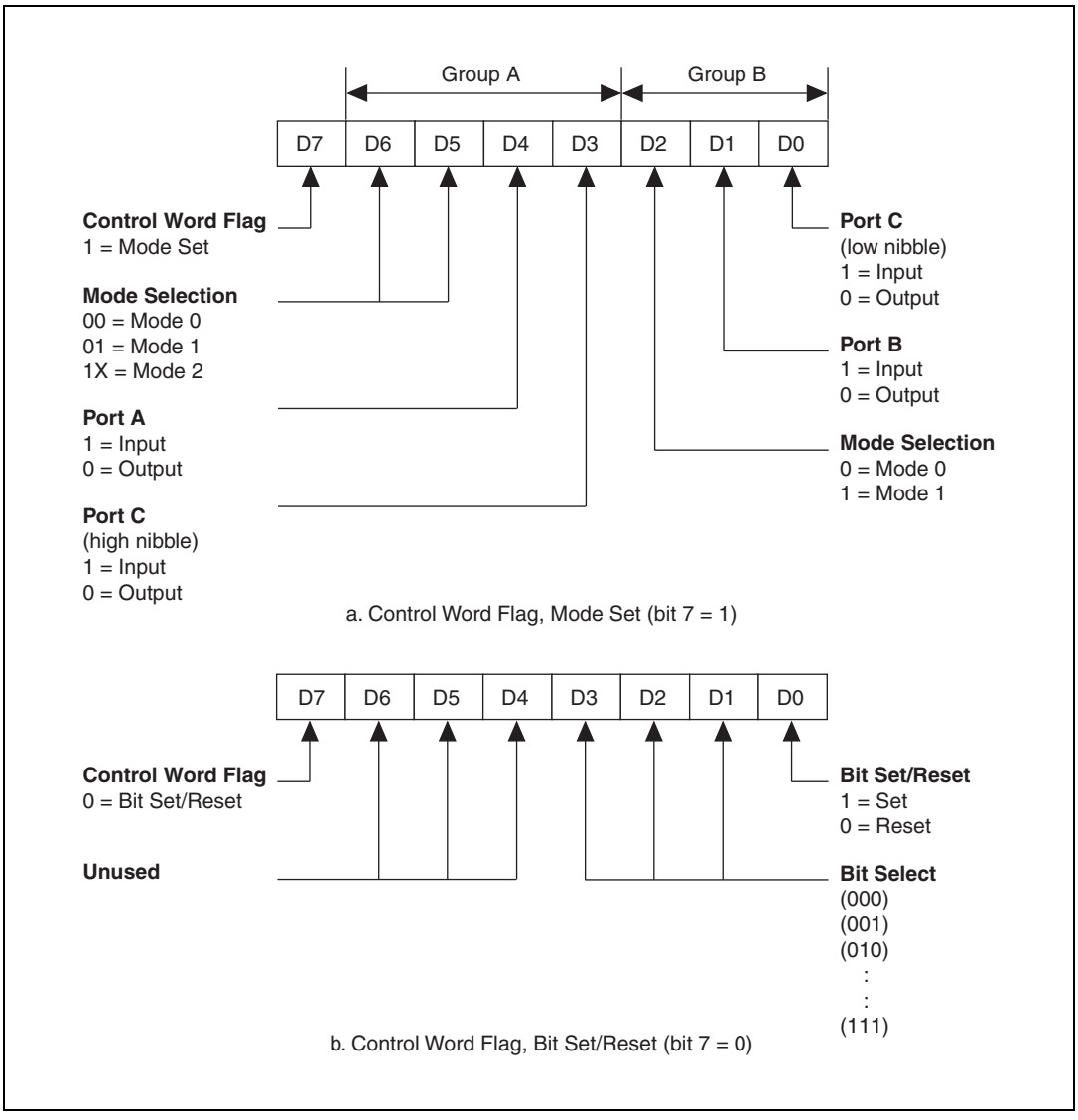


Figure B-2. Control Word Formats for the 82C55A

Table B-2 shows the control words for setting or resetting each bit in port C. Notice that programming the set/reset option for the bits of port C clears bit 7 of the control word.

Table B-2. Port C Set/Reset Control Words

Bit Number	Bit Set Control Word	Bit Reset Control Word	Bit Set or Reset in Port C
0	0xxx0001	0xxx0000	xxxxxxxb
1	0xxx0011	0xxx0010	xxxxxxbx
2	0xxx0101	0xxx0100	xxxxxbxx
3	0xxx0111	0xxx0110	xxxxbxxx
4	0xxx1001	0xxx1000	xxxbxxxx
5	0xxx1011	0xxx1010	xxbxxxxx
6	0xxx1101	0xxx1100	xbxxxxxx
7	0xxx1111	0xxx1110	bxxxxxxx

Register Description for the 82C53 (PCI-DIO-96, PXI-6508 Only)

Figure B-3 shows the control word format used to program the 82C53. Bits 7 and 6 of the control word select the counter to be programmed. Bits 5 and 4 select the mode by which the count data is written to and read from the selected counter. Bits 3, 2, and 1 select the mode for the selected counter. Bit 0 selects whether the counter counts in binary or BCD format. After writing to the Configuration Register to configure a counter, you can read or write the counter itself eight bits at a time, as controlled by the access mode.

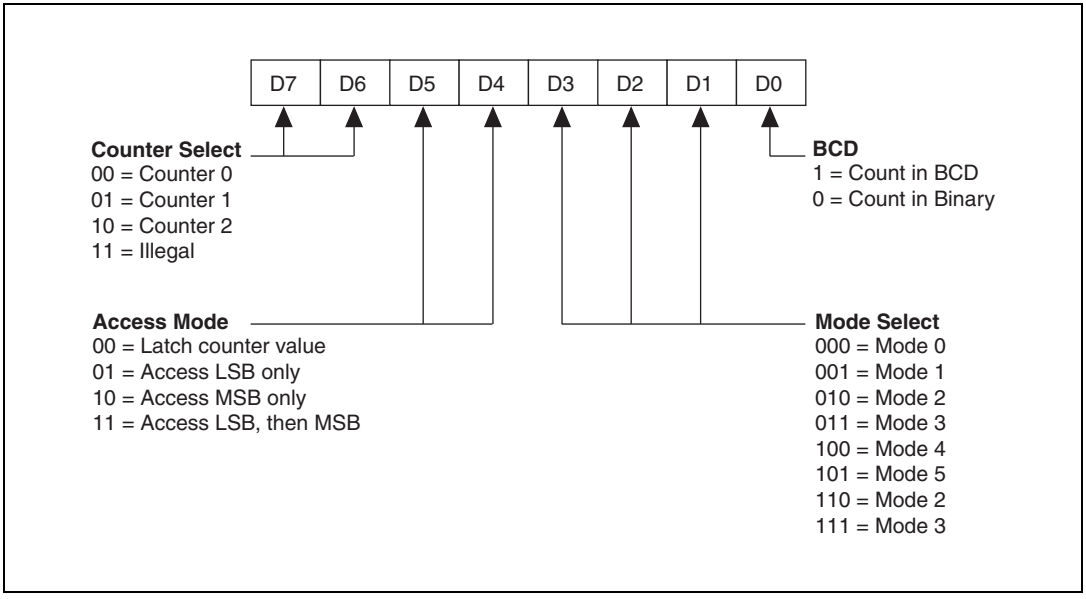


Figure B-3. Control Word Format for the 82C53

Register Description for the Interrupt Control Registers

There are two interrupt control registers on your DIO board. One of these registers has individual enable bits for the two interrupt lines from each of the 82C55A devices. The other register has a master interrupt enable bit and two bits for the timed interrupt circuitry. Of the latter two bits, one bit enables counter interrupts, while the other selects counter 0 or counter 1. This appendix lists the bit maps and signal definitions.

Interrupt Control Register 1

Address: Base address + 14 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map (PCI-DIO-96/PXI-6508):

7	6	5	4	3	2	1	0
DIRQ1	DIRQ0	CIRQ1	CIRQ0	BIRQ1	BIRQ0	AIRQ1	AIRQ0

Bit Map (PCI-6503):

7	6	5	4	3	2	1	0
X	X	X	X	X	X	AIRQ1	AIRQ0

Bit	Name	Description
7–2	X	Reserved on the PCI-6503.
7	DIRQ1	PPI D Port B Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI D sends an interrupt, INTRB, to the computer. If this bit is cleared, PPI D does not send the interrupt INTRB to the computer, regardless of the setting of INTEN.
6	DIRQ0	PPI D Port A Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI D sends an interrupt, INTRA, to the computer. If this bit is cleared, PPI D does not send the interrupt INTRA to the computer, regardless of the setting of INTEN.

5	CIRQ1	PPI C Port B Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI C sends an interrupt, INTRB, to the computer. If this bit is cleared, PPI C does not send the interrupt INTRB to the computer, regardless of the setting of INTEN.
4	CIRQ0	PPI C Port A Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI C sends an interrupt, INTRA, to the computer. If this bit is cleared, PPI C does not send the interrupt INTRA to the computer, regardless of the setting of INTEN.
3	BIRQ1	PPI B Port B Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI B sends an interrupt, INTRB, to the computer. If this bit is cleared, PPI B does not send the interrupt INTRB to the computer, regardless of the setting of INTEN.
2	BIRQ0	PPI B Port A Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI B sends an interrupt, INTRA, to the computer. If this bit is cleared, PPI B does not send the interrupt INTRA to the computer, regardless of the setting of INTEN.
1	AIRQ1	PPI A Port B Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI A sends an interrupt, INTRB, to the computer. If this bit is cleared, PPI A does not send the interrupt INTRB to the computer, regardless of the setting of INTEN.
0	AIRQ0	PPI A Port A Interrupt Enable Bit—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI A sends an interrupt, INTRA, to the computer. If this bit is cleared, PPI A does not send the interrupt INTRA to the computer, regardless of the setting of INTEN.

Interrupt Control Register 2

Address: Base address + 15 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map (PCI-DIO-96/PXI-6508):

7	6	5	4	3	2	1	0
X	X	X	X	X	INTEN	CTRIRQ	CTR1

Bit Map (PCI-6503):

7	6	5	4	3	2	1	0
X	X	X	X	X	INTEN	X	X

Bit	Name	Description
7–3	X	Reserved.
2	INTEN	Interrupt Enable Bit—If this bit is set, the DIO board can interrupt the computer. If this bit is cleared, the DIO board cannot generate interrupts to the computer, regardless of the status of the bits in Interrupt Control Register 2.
1–0	X	Reserved on the PCI-6503.
1	CTRIRQ	Counter Interrupt Enable Bit—If this bit is set, the 82C53 counter outputs can interrupt the computer. If this bit is cleared, the counter outputs have no effect. To avoid a spurious interrupt, keep INTEN low when you set CTRIRQ; that is, set CTRIRQ before setting INTEN.
0	CTR1	Counter Select Bit—If this bit is set, the output from counter 1 of the 82C53 is connected to the interrupt request circuitry. In this mode, counter 0 of the 82C53 acts as a frequency scaler for counter 1, which generates the interrupt. If CTR1 is cleared, the output from counter 0 of the 82C53 is connected to the interrupt request circuitry. In this mode, counter 0 generates the interrupt. For more information, refer to the *Interrupt Programming Example* section for the 82C53 in this appendix.

Interrupt Clear Register (PCI-DIO-96, PXI-6508 Only)

The interrupt clear register has no bits associated with it. Use this register to reset the state of the interrupt request signal once the interrupt routine has been entered. To clear the interrupt, perform an 8-bit write to this register address; the data is irrelevant.

Address: Base address + 16 (hex)

Type: Write-only

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Bit	Name	Description
7–0	X	Don't care bit.

Programming

This section contains instructions on how to operate your DIO board circuitry, and examples of the programming steps necessary to execute an operation. If you are not using NI-DAQ, you must first initialize your board.

Programming your DIO board involves writing to and reading from registers on the board. The *Register Map and Description* section contains a listing of these registers. For additional programming examples, including initialization, refer to the Measurement Hardware Driver Development Kit (MHDDK) examples. To access the MHDDK, go to `ni.com/info` and enter the info code `mhddk`.

PCI Local Bus

The PCI-DIO-96, PXI-6508, and PCI-6503 are fully compatible with the *PCI Local Bus Specification*, Revision 2.1, from the PCI Special Interest Group (SIG). The PXI-6508 is fully compliant with the National Instruments *PXI Specification*, Revision 1.0. All three boards use the PCI Local Bus to move data. The PCI Local Bus is a high performance, 32-bit bus with multiplexed address and data lines. The PCI system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. Bus-related resources must be configured before you attempt to execute a register-level program. This entails assigning a base address and interrupt channel to your DIO board.

Programming Examples

The programming examples in this section demonstrate the programming steps needed to perform several different operations. The instructions are language independent; that is, they tell you to read or write a given register or to detect if a given bit is set or cleared, without presenting the actual code. The information given is not intended to be used without proper modification in a practical solution.

Before you can implement any of the examples into a real application, you must know the base memory address for your board. To generate and process any interrupts, you must write and install an applicable interrupt service routine.

Note In this appendix, all numbers preceded by 0x are hexadecimal.

Table B-3 contains common terms used in the programming examples.

Table B-3. Common Programming Example Terms

Term	Definition
Port A	Address of PPI A Port A Register (Base Address + 0x00)
Port B	Address of PPI A Port B Register (Base Address + 0x01)
Port C	Address of PPI A Port C Register (Base Address + 0x02)
8255Cnfg	Address of PPI A Configuration Register (Base Address + 0x03)
Ctr0	Address of 82C53 Counter 0 Register (Base Address + 0x10)
Ctr1	Address of 82C53 Counter 1 Register (Base Address + 0x11)
CntrCnfg	Address of 82C53 Configuration Register (Base Address + 0x13)
IREG1	Address of Interrupt Control Register 1 (Base Address + 0x14)
IREG2	Address of Interrupt Control Register 2 (Base Address + 0x15)
Write (address, data)	Generic function call for a memory space Write of data to address
Read (address)	Generic function call for a memory space Read from address
CWrite (offset, data)	PCI configuration space write of data to PCI configuration space offset

PCI Initialization

To program at the register level without NI-DAQmx or Traditional NI-DAQ (Legacy), you must know the PCI-DIO-96 or PXI-6508 base memory address and, if using interrupts, install an interrupt handler. This manual does not discuss writing an interrupt handler. In order for the board to operate properly, you must configure the PCI MITE ASIC. NI-DAQmx or Traditional NI-DAQ (Legacy) usually performs this function, but if you are not using NI-DAQ, then you must configure the PCI MITE ASIC.

The following sections explain how to configure the PCI MITE ASIC. You must implement the references made to PCI BIOS[1] calls.

To configure the PCI MITE chip, you must first write an algorithm that finds and stores all configuration information about the board. To do this, use PCI BIOS calls to search PCI configuration space for the National Instruments vendor ID (0x1093) and PCI-DIO-96 device ID (0x0160), PXI-6508 device ID (0x13c0), or PCI-6503 device ID (0x17d0). If a board is found, the algorithm can store all the board's configuration information into a data structure.

[1] To obtain more information on PCI BIOS calls from the PCI SIG, go to `www.pcisig.com`.

Base Address Register 0 (BAR0) corresponds to the base address of the PCI MITE, while Base Address Register 1 (BAR1) is the base address of the board registers. The size of each of these windows is 4 KB. Both addresses will most likely be mapped above 1 MB in the memory map. This means that you must know how to perform memory cycles to extended memory to communicate with the board. The memory map provides information to re-map the board under 1 MB, which simplifies communication with the board. To accomplish this, use PCI BIOS read and write calls. Use the pseudocode in this section to re-map the board below 1 MB. If you choose not to re-map the board, you must still perform steps 4 and 5. All values in this example are 32 bits.

1. Write the address to which you want to re-map the PCI MITE to *PCI configuration space offset 0x10 (BAR0)*.
2. Write the value *0x0000aeae* to offset *0x340* from the new PCI MITE address.
3. Write the address to which you want to re-map the board (other than the PCI MITE) to *PCI configuration space offset 0x14 (BAR1)*.
4. Create the window data value by masking the new board address:

   window data value = ((0xffffff00 *and* new board address) *or* (0x00000080))

   If you are not remapping the board, then the new board address is the value in *BAR1*.
5. Write the window data value to offset 0xc0 from the new PCI MITE address.
   If you are not remapping the board, then the new PCI MITE address is the value in *BAR0*.

The following pseudocode re-maps the PCI MITE to memory address *0xd0000* and the board to memory address *0xd1000*.

```
CWrite(0x10,0x000d0000)
Write(0xd0340,0x0000aeae)
CWrite(0x14,0x000d1000)
Write(0xd00c0,0x000d1080)
```

In this example, the new base address for the PCI-DIO-96 or PXI-6508 is now *0xd1000*. It is important that the memory range to which you re-map the board is not being used by another device or system resource. You can exclude this memory from use with a memory manager.

Programming Considerations for the 82C55A

Modes of Operation

The following list contains the three basic modes of operation for the 82C55A. Ports A and B can operate in different modes.

- Mode 0—Basic I/O—This mode is used for simple input and output operations for each port. No handshaking is required; a specified port simply writes to or reads from data. Mode 0 has the following features:
  - Two 8-bit ports (A and B) and two 4-bit ports (upper and lower nibbles of port C).
  - Any port can be input or output.
  - Outputs are latched, but inputs are not latched.
- Mode 1—Strobed I/O—This mode transfers data that is synchronized by handshaking signals. Ports A and B use the eight lines of port C to generate or receive the handshake signals. This mode divides the ports into two groups (group A and group B) and includes the following features:
  - Each group contains one 8-bit data port (port A or port B) and one 3-bit control/data port (upper or lower portion of port C).
  - The 8-bit data ports can be either input or output; both are latched.
  - The 3-bit ports are used for control and status of the 8-bit data ports.
  - Interrupt generation and enable/disable functions are available.
- Mode 2—Bidirectional bus—This mode is used for communication over a bidirectional 8-bit bus. Handshaking signals are used in a manner similar to mode 1. Mode 2 is available for use in group A only (port A and the upper portion of port C). Other features of this mode include the following:
  - One 8-bit bidirectional port (port A) and a 5-bit control/status port (port C).
  - Latched inputs and outputs.
  - Interrupt generation and enable/disable functions.

The 82C55A also has a single bit set/reset feature for port C, which is programmed by the 8-bit control word. Any of the eight bits of port C can be set or reset with one control word. This feature generates control signals for port A and port B when these ports are operating in mode 1 or mode 2.

Mode 0—Basic I/O

Use mode 0 for simple I/O functions (no handshaking) for each of the three ports and assign each port as an input or an output port. Table B-4 shows the 16 possible I/O configurations. Notice that programming the mode of operation for each port sets bit 7 of the control word.

Table B-4. Mode 0 I/O Configurations

Number	Control Word Bit 76543210	Group A		Group B	
		Port A	Port C†	Port B	Port C‡
0	10000000	Output	Output	Output	Output
1	10000001	Output	Output	Output	Input
2	10000010	Output	Output	Input	Output
3	10000011	Output	Output	Input	Input
4	10001000	Output	Input	Output	Output
5	10001001	Output	Input	Output	Input
6	10001010	Output	Input	Input	Output
7	10001011	Output	Input	Input	Input
8	10010000	Input	Output	Output	Output
9	10010001	Input	Output	Output	Input
10	10010010	Input	Output	Input	Output
11	10010011	Input	Output	Input	Input
12	10011000	Input	Input	Output	Output
13	10011001	Input	Input	Output	Input
14	10011010	Input	Input	Input	Output
15	10011011	Input	Input	Input	Input

† Upper nibble of port C

‡ Lower nibble of port C

Mode 0 Basic I/O Programming Example

The following example shows how to configure PPI A for mode 0 input and output.

```
Write (8255Cnfg,0x80)     Set mode 0—ports A, B, and C are outputs
Write (PortA, Data)       Write data to port A
Write (PortB, Data)       Write data to port B
Write (PortC, Data)       Write data to port C

Write (8255Cnfg,0x90)     Set mode 0—port A is Input;ports B and
                          C are outputs
Write (PortB, Data)       Write data to port B
Read (PortA)              Read data from port A
```

Mode 1—Strobed Input

Note For mode 1 examples, you must configure the don't care bits appropriately in the control word if you want to use the other ports in combination with the example.

In mode 1, the digital I/O bits are divided into two groups: group A and group B. Each of these groups contains one 8-bit port and one 3-bit control/data port. The 8-bit port can be either an input or an output port, and the 3-bit port is used for control and status information for the 8-bit port. Handshaking signals in the 3-bit port synchronize the transfer of data.

Figure B-4 shows the control word written to the Configuration Register to configure port A for input in mode 1. You can use bits PC6 and PC7 of port C as extra input or output lines.

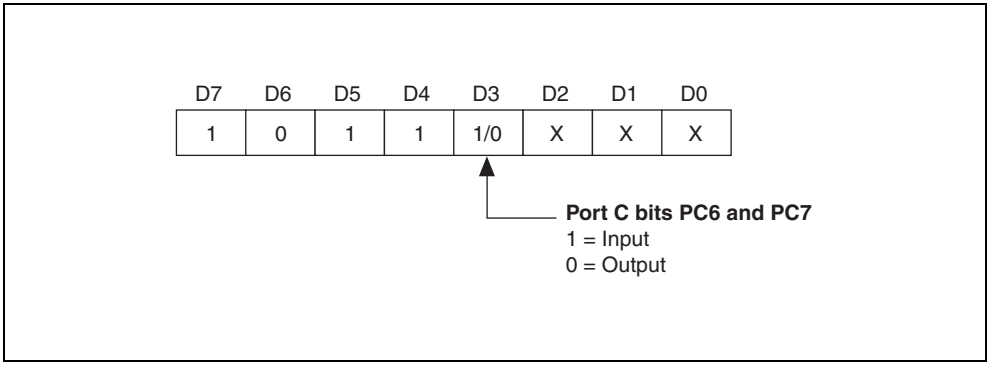


Figure B-4. Control Word to Configure Port A for Mode 1 Input

Figure B-5 shows the control word written to the Configuration Register to configure port B for input in mode 1. Notice that port B does not have extra input or output lines left from port C when ports A and B are both enabled for handshaking.

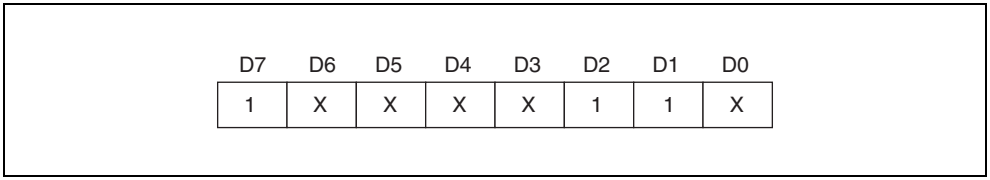


Figure B-5. Control Word to Configure Port B for Mode 1 Input

During a mode 1 data read transfer, read port C to obtain the status of the handshaking lines and interrupt signals. Refer to the *Port C Status-Word Bit Definitions for Input (Ports A and B)* section, the *Port C Status-Word Bit Definitions for Output (Ports A and B)* section, and the *Port C Status-Word Bit Definitions for Bidirectional Data Path (Port A Only)* section for detailed definitions.

Port C Status-Word Bit Definitions for Input (Ports A and B)

Address: Base address + 02 (hex) for PPI A
Base address + 06 (hex) for PPI B
Base address + 0A (hex) for PPI C
Base address + 0E (hex) for PPI D

Type: Read and write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB

Bit	Name	Description
7–6	I/O	Input/Output—These bits can be used for general-purpose I/O when port A is in mode 1 input. If these bits are configured for output, the port C bit set/reset function must be used to manipulate them.
5	IBFA	Input Buffer Full for Port A—A high setting indicates that data has been loaded into the input latch for port A.
4	INTEA	Interrupt Enable Bit for Port A—Setting this bit enables the INTRA flag from port A of the 82C55A. Control INTEA by setting/resetting PC4.
3	INTRA	Interrupt Request Status for Port A—This status flag, which operates only when INTEA is high, indicates that port A has acquired data and is ready to be read. If you have enabled interrupts (by setting INTEN and the appropriate bit in Interrupt Control Register 2), this status flag also indicates that an interrupt request is pending for port A.
2	INTEB	Interrupt Enable Bit for Port B—Setting this bit enables the INTRB flag from port B of the 82C55A. Control INTEB by setting/resetting PC2.
1	IBFB	Input Buffer Full for Port B—A high setting indicates that data has been loaded into the input latch for port B.

0	INTRB	Interrupt Request Status for Port B—Interrupt Request Status for Port B. This status flag, which operates only when INTEA is high, indicates that port B has acquired data and is ready to be read. If you have enabled interrupts (by setting INTEN and the appropriate bit in Interrupt Control Register 2), this status flag also indicates that an interrupt request is pending for port B.

At the digital I/O connector, port C has the pin assignments shown in Figure B-6 when in mode 1 input. Notice that the status of STBA* and the status of STBB* are not included in the port C status word.

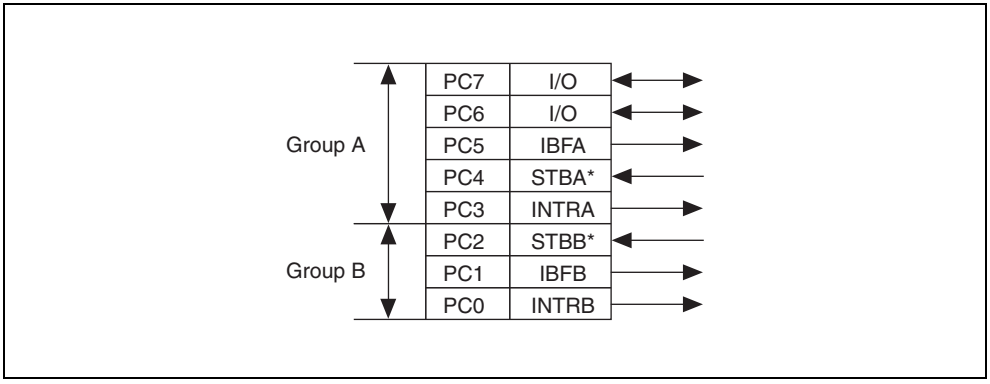


Figure B-6. Port C Pin Assignments on I/O Connector when Port C Configured for Mode 1 Input

Mode 1 Strobed Input Programming Example

The following example shows how to configure PPI A for mode 1 input.

```
Write (8255Cnfg, 0xB0)  Set mode 1—port A is an input
Write (8255Cnfg, 0x09)  Set PC4 to enable the INTRA status flag
Loop until the INTRA (PC3) and IBFA (PC5) status flags are set,
                        indicating that the 82C55A is ready for a
                        transfer and that the input buffer is full
Read (PortA)            Read data from port A
```

Mode 1—Strobed Output

Note For mode 1 examples, you must configure the don't care bits appropriately in the control word if you want to use the other ports in combination with the example.

Figure B-7 shows the control word written to the Configuration Register to configure port A for output in mode 1. You can use bits PC4 and PC5 of port C as extra input or output lines.

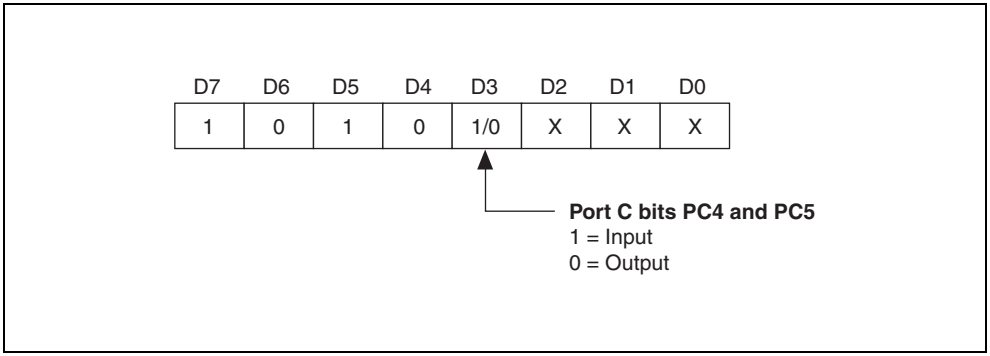


Figure B-7. Control Word to Configure Port A for Mode 1 Output

Figure B-8 shows the control word written to the Configuration Register to configure port B for output in mode 1. Notice that port B does not have extra input or output lines left from port C when ports A and B are both configured for handshaking.

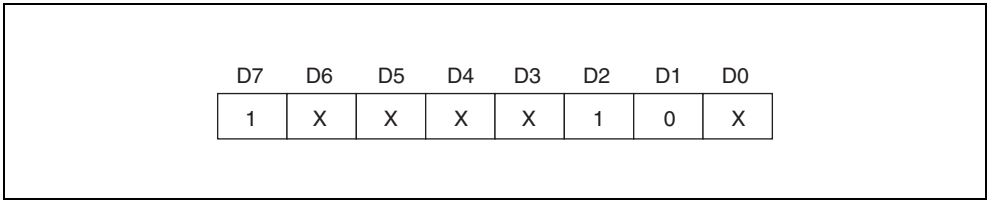


Figure B-8. Control Word to Configure Port B for Mode 1 Output

During a mode 1 data write transfer, you can obtain the status of the handshaking lines and interrupt signals by reading port C. Notice that the bit definitions are different for a write and a read transfer.

Port C Status-Word Bit Definitions for Output (Ports A and B)

Address: Base address + 02 (hex) for PPI A
Base address + 06 (hex) for PPI B
Base address + 0A (hex) for PPI C
Base address + 0E (hex) for PPI D

Type: Read and write

Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
OBFA*	INTEA	I/O	I/O	INTRA	INTEB	OBFB*	INTRB

Bit	Name	Description
7	OBFA*	Output Buffer Full for Port A—A low setting indicates that the CPU has written data to port A.
6	INTEA	Interrupt Enable Bit for Port A—Setting this bit enables the INTRA flag from port A of the 82C55A. Control this bit by setting/resetting PC6.
5–4	I/O	Input/Output—These bits can be used for general-purpose I/O when port A is in mode 1 output. If these bits are configured for output, you must use the port C bit set/reset function to manipulate them.
3	INTRA	Interrupt Request Status for Port A—This status flag, which operates only when INTEA is high, indicates that port A has acquired data and is ready to be read. If you have enabled interrupts (by setting INTEN and the appropriate bit in Interrupt Control Register 2), this status flag also indicates that an interrupt request is pending for port A.
2	INTEB	Interrupt Enable Bit for Port B—Setting this bit enables the INTRB flag from port B of the 82C55A. Control this bit by setting/resetting PC2.
1	OBFB*	Output Buffer Full for Port B—A low setting indicates that the CPU has written data to port B.

0	INTRB	Interrupt Request Status for Port B—This status flag, which operates only when INTEA is high, indicates that port B has acquired data and is ready to be read. If you have enabled interrupts (by setting INTEN and the appropriate bit in Interrupt Control Register 2), this status flag also indicates that an interrupt request is pending for port B.

At the digital I/O connector, port C has the pin assignments shown in Figure B-9 when in mode 1 output. Notice that the status of ACKA* and ACKB* are not included when port C is read.

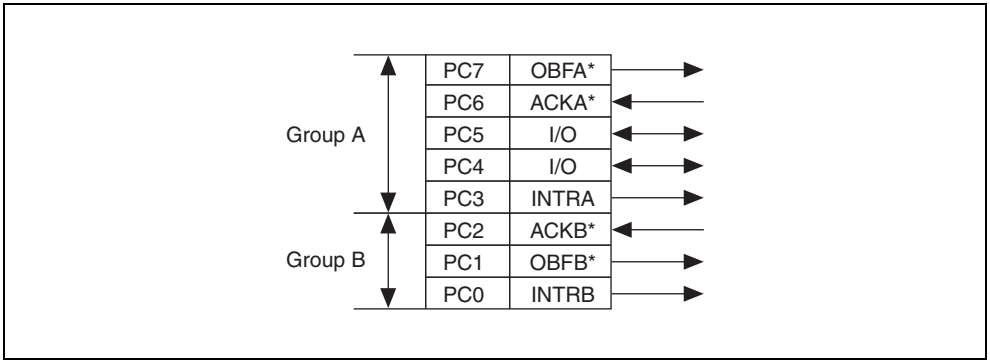


Figure B-9. Port C Pin Assignments on I/O Connector when Port C Configured for Mode 1 Output

Mode 1 Strobed Output Programming Example

The following example shows how to configure PPI A for mode 1 output.

```
Write (8255Cnfg, 0xA0)    Set mode 1—port A is an output
Write (8255Cnfg, 0x0D)    Set PC6 to enable the INTRA status flag
Loop until the INTRA (PC3) and OBFA* (PC7) status flags are set,
                          indicating that the 82C55A is ready for a
                          transfer and that the output buffer is not
                          full
Write (PortA, Data)       Write data to port A
```

Mode 2—Bidirectional Bus

Note For mode 2 examples, you must configure the don't care bits appropriately in the control word if you want to use the other ports in combination with the example.

Mode 2 has an 8-bit bus that can transfer both input and output data without changing the configuration. The data transfers are synchronized with handshaking lines in port C. This mode uses only port A; however, port B can be used in either mode 0 or mode 1 while port A is configured for mode 2.

Figure B-10 shows the control word written to the Configuration Register to configure port A as a bidirectional data bus in mode 2. If port B is configured for mode 0, you can use PC2, PC1, and PC0 of port C as extra input or output lines.

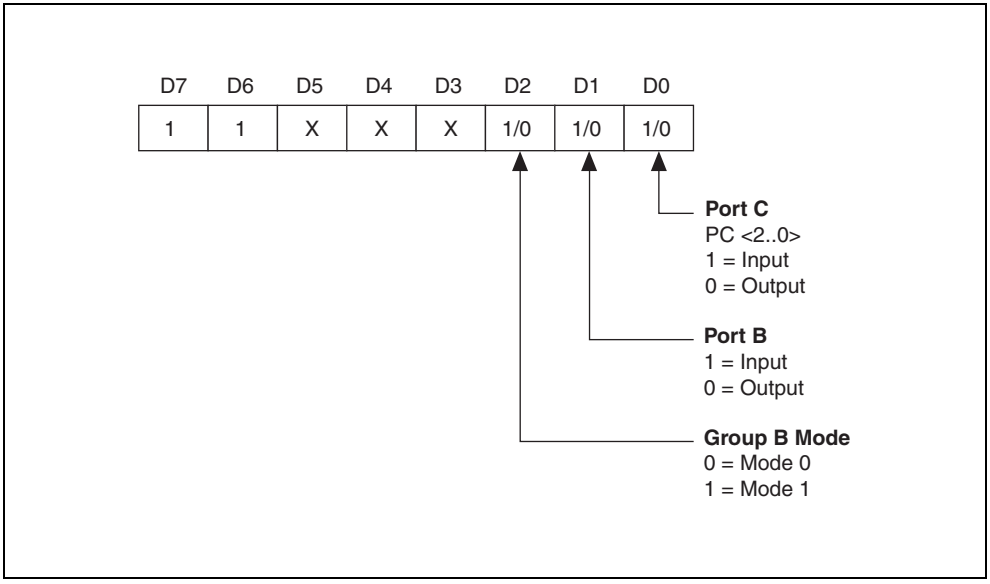


Figure B-10. Control Word to Configure Port A as Mode 2 Bidirectional Data Bus

During a mode 2 data transfer, you can obtain the status of the handshaking lines and interrupt signals by reading port C. The following sections show the port C status-word bit definitions for a mode 2 transfer.

Port C Status-Word Bit Definitions for Bidirectional Data Path (Port A Only)

Address: Base address + 02 (hex) for PPI A
Base address + 06 (hex) for PPI B
Base address + 0A (hex) for PPI C
Base address + 0E (hex) for PPI D

Type: Read and write

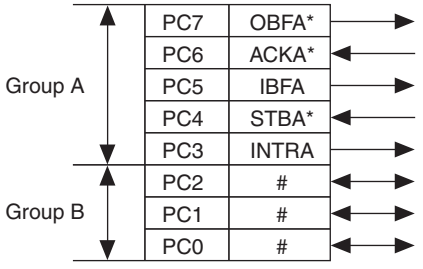
Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
OBFA*	INTE1	IBFA	INTE2	INTRA	I/O	I/O	I/O

Bit	Name	Description
7	OBFA*	Output Buffer Full for Port A—A low setting indicates that the CPU has written data to port A.
6	INTE1	Interrupt Enable Bit for Port A Output Interrupts—Setting this bit enables the INTRA flag from port A of the 82C55A for output. Control this bit by setting/resetting PC6.
5	IBFA	Input Buffer Full for Port A—A high setting indicates that data has been loaded into the input latch of port A.
4	INTE2	Interrupt Enable Bit for Port A Input Interrupts—Setting this bit enables the INTRA flag from port A of the 82C55A for input. Control this bit by setting/resetting PC4.
3	INTRA	Interrupt Request Status for Port A—This status flag, which operates only when INTE1 or INTE2 is high, indicates that port A is ready to be read or written; check the IBF and OBFA* flags to determine which. If you have enabled interrupts (by setting INTEN and the appropriate bit in Interrupt Control Register 2), the INTRA status flag also indicates that an interrupt request is pending for port A.
2–0	I/O	Input/Output—Use these bits for general-purpose I/O lines if group B is configured for mode 0. If group B is configured for mode 1, refer to the bit explanations shown in the preceding mode 1 sections.

Figure B-11 shows the port C pin assignments on the digital I/O connector when port C is configured for mode 2. Notice that the port C status word does not include the status of STBA* or the status of ACKA*.



The three port C lines associated with group B function based on the mode selected for group B; that is, if group B is configured for mode 0, PC<2..0> function as general-purpose I/O, but if group B is configured for mode 1 input or output, PC<2..0> function as handshaking lines as shown in the preceding mode 1 sections.

Figure B-11. Port C Pin Assignments on I/O Connector when Port C is Configured for Mode 2

Mode 2 Bidirectional Bus Programming Example

The following example shows how to configure PPI A for mode 2 input and output.

```
Write (8255Cnfg, 0xC0)            Set mode 2—port A is bidirectional
Write (8255Cnfg, 0x09)            Set PC4 to enable the INTRA status
                                  flag for input
Write (8255Cnfg, 0x0D)            Set PC6 to enable the INTRA status
                                  flag for output
Loop until the INTRA (PC3) status flag is set, indicating the 82C55
                                  is ready for a transfer
If IBFA (PC5) is set, read (PortA)If input buffer is full, read data
If OBFA* (PC7) is set,
   write (PortA, data)            If output buffer is not full, write
                                  data
```

Interrupt Handling

You must set the INTEN bit of Interrupt Control Register 2 to enable interrupts. Clear this bit first to disable unwanted interrupts. After all sources of interrupts have been disabled or placed in an inactive state, you can set INTEN. You must set INTEN before you generate an interrupt for proper operation.

To interrupt the computer using one of the 82C55A devices, program the selected 82C55A for the I/O mode desired. In mode 1, set either the INTEA or the INTEB bit to enable interrupts from port A or port B, respectively. In mode 2, set either INTE1 or INTE2 for interrupts on output or input transfers, respectively. The INTE1 and INTE2 interrupt outputs are cascaded into a single interrupt output for port A. After you enable interrupts from the 82C55A, set the appropriate enable bit for the selected 82C55A; for example, if you select both mode 2 interrupts for PPI C, set CIRQ0 to interrupt the computer.

To interrupt the computer using one of the 82C53 counter outputs on the PCI-DIO-96 or PXI-6508, program the counters as described in the *Interrupt Programming Example* section.

You can use external signals to generate interrupts when port A or port B is in mode 0 and the low nibble of port C is configured for input. If port A is in mode 0, use PC3 to generate an interrupt; if port B is in mode 0, use PC0 to generate an interrupt. After you have configured the selected 82C55A, you must set the corresponding interrupt enable bit in Interrupt Control Register 1. If you are using PC3, set *x*IRQ0; if you are using PC0, set *x*IRQ1, where *x* is the letter corresponding to the PPI you want to generate interrupts (A–D). When the external signal becomes logic high, an interrupt request occurs. To disable the external interrupt, ensure that the interrupt service routine that you have written acknowledges the interrupt. On the PCI-DIO-96 and PXI-6508, ensure that the interrupt service routine also writes the interrupt clear register.

Interrupt Programming Examples for the 82C55A

The following examples show the process required to enable interrupts for several different operating modes. You must write and install an interrupt service routine in order to process the interrupt and gain any useful knowledge from it. You should clear all interrupt sources and interrupt enable bits first to disable unwanted interrupts.

Mode 1 Strobed Input Programming Example

The following example shows how to set up interrupts for mode 1 input for port A.

```
Write (8255Cnfg, 0xB0)    Set mode 1—port A is an input
Write (8255Cnfg, 0x09)    Set PC4 to enable interrupts from
                          the 82C55A
Write (IREG2, 0x04)       Set INTEN bit
Write (IREG1, 0x01)       Set AIRQ0 to enable PPI A,
                          port A interrupts
```

Mode 1 Strobed Output Programming Example

The following example shows how to set up interrupts for mode 1 output for port A.

```
Write(8255Cnfg, 0xA0)     Set mode 1—port A is an output
Write(8255Cnfg, 0x0D)     Set PC6 to enable interrupts from 82C55A
Write(IREG2, 0x04)        Set INTEN bit
Write(IREG1, 0x01)        Set AIRQ0 to enable PPI A,
                          port A interrupts
```

Mode 2 Bidirectional Bus Programming Example

The following example shows how to set up interrupts for mode 2 output transfers.

```
Write (8255Cnfg, 0xC0)    Set mode 2—port A is bidirectional
Write (8255Cnfg, 0x0D)    Set PC6 to enable interrupt from 82C55A
Write (IREG2, 0x04)       Set INTEN bit
Write (IREG1, 0x01)       Set AIRQ0 to enable PPI A,
                          port A interrupts
```

The following example shows how to set up interrupts for mode 2 input transfers.

```
Write (8255Cnfg, 0xC0)    Set mode 2—port A is bidirectional
Write (8255Cnfg, 0x09)    Set PC4 to enable interrupt from 82C55A
Write (IREG2, 0x04)       Set INTEN bit
Write (IREG1, 0x01)       Set AIRQ0 to enable PPI A,
                          port A interrupts
```

Programming Considerations for the 82C53

The PCI-DIO-96 and PXI-6508 contain an 82C53 programmable interval timer. The following section contains a general overview and configuration information for the 82C53.

General Information

The 82C53 contains three counter/timers, each of which can operate in one of six different modes. However, only counter 0 and counter 1 are configured for operation; counter 2 is not connected, nor is it available on the external I/O connector. In addition, the counter gates are wired in such a way (tied to logic high) that modes 1 and 5 are unusable; the recommended counter mode is mode 2.

The source for counter 0 is a 2 MHz clock. If you use counter 0 to interrupt the computer, configure the counter for rate generation, or mode 2. If you use counter 1 to interrupt the computer, counter 0 is a frequency scale that feeds the source input for counter 1. In this case, configure both counters for rate generation, or mode 2.

To determine the time between pulses generated by counter 0, multiply the load value by 500 ns (1/(2 MHz)). To determine the time between pulses generated by counter 1, multiply the load value by the time between pulses of counter 0. The following section shows a sample configuration procedure.

Interrupt Programming Example

The following example shows how to set up counter 0 to generate interrupts:

```
Write(IREG1, 0x00)      Disable all 82C55A interrupts
Write(IREG2, 0x00)      Disable counter interrupts
Write(CntrCnfg, 0x34)   Set counter 0 to mode 2
Write(IREG2, 0x02)      Enable counter interrupts and select the
                        output from counter 0 before enabling board
                        interrupts
Write(IREG2, 0x06)      Enable board interrupts
Write(Ctr0, Data0)      Send the least significant byte
                        of the counter data to counter 0
Write(Ctr0, Data1)      Send the most significant byte
                        of the counter data to counter 0
```

The counter begins counting as soon as the most significant byte is written. When you are ready to exit your program, disable the counter and interrupts as shown below.

```
Write(Cnfg, 0x30)       Turn off counter 0
Write(IREG2, 0x00)      Disable all PCI-DIO-96/PXI-6508
                        interrupts
```

Note In order for any of the interrupts to be processed, you must write and install an interrupt service routine. Failure to do so could cause the system to fail upon the interrupt generation.

C

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Glossary

Symbol	Prefix	Value
n	nano	10^{-9}
µ	micro	10^{-6}
m	milli	10^{-3}
k	kilo	10^{3}
M	mega	10^{6}

Numbers/Symbols

°	degrees
>	greater than
≥	greater than or equal to
<	less than
–	negative of, or minus
Ω	ohms
/	per
%	percent
±	plus or minus
+	positive of, or plus
+5 V	+5 Volts signal

A

A	amperes
ACK*	acknowledge input signal

AIRQ0	PPI A port A interrupt enable bit
AIRQ1	PPI A port B interrupt enable bit
ANSI	American National Standards Institute
APA	PPI A port A
APB	PPI A port B
APC	PPI A port C
ASIC	Application Specific Integrated Circuit
AWG	American Wire Gauge

B

BCD	binary coded decimal
BIRQ0	PPI B port A interrupt enable bit
BIRQ1	PPI B port B interrupt enable bit
BPA	PPI B port A
BPB	PPI B port B
BPC	PPI B port C

C

C	Celsius
CIRQ0	PPI C port A interrupt enable bit
CIRQ1	PPI C port B interrupt enable bit
cm	centimeters
CompactPCI	refers to the core specification defined by the PCI Industrial Computer Manufacturer's Group (PICMG)
CPA	PPI C port A

CPB	PPI C port B
CPC	PPI C port C
CTR1	counter select bit
CTRIRQ	counter interrupt enable bit

D

DAQ	a system that uses the personal computer to collect, measure, and generate electrical signals
DI	digital input
DIO	digital input/output
DIRQ0	PPI D port A interrupt enable bit
DIRQ1	PPI D port B interrupt enable bit
DMA	direct memory access—a method by which data can be transferred to/from computer memory from/to a device or memory on the bus while the processor does something else. DMA is the fastest method of transferring data to/from computer memory.
DO	digital output
DPA	PPI D port A
DPB	PPI D port B
DPC	PPI D port C

F

ft	feet

G

GND	ground signal

H

hex	hexadecimal

I

I/O	input/output
IBF	input buffer full signal
in.	inches
INTE1	port A output interrupt enable bit
INTE2	port A input interrupt enable bit
INTEA	port A interrupt enable bit
INTEB	port B interrupt enable bit
INTEN	interrupt enable bit
INTRA	port A interrupt request status
INTRB	port B interrupt request status

L

LED	light-emitting diode
LSB	least significant bit

M

m	meters
max	maximum
MB	megabytes of memory
min.	minutes

min	minimum
MSB	most significant bit

O

OBF*	output buffer full signal

P

PA, PB, PC <0..7>	port A, B, or C 0 through 7 lines
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA. It is achieving widespread acceptance as a standard for PCs and workstations; it offers a theoretical maximum transfer rate of 132 Mbytes/s.
port	a digital port, consisting of four or eight lines of digital input and/or output
PPI	programmable peripheral interface
PXI	PCI eXtensions for Instrumentation. PXI is an open specification that builds off the CompactPCI specification by adding instrumentation-specific features.

R

RD*	read signal

S

S	samples
s	seconds
SCXI	Signal Conditioning eXtensions for Instrumentation—the National Instruments product line for conditioning low-level signals within an external chassis near sensors so only high-level signals are sent to DAQ boards in the noisy PC environment

signal conditioning	the manipulation of signals to prepare them for digitizing
STB	strobe input signal

T

TTL	transistor-transistor logic
typ	typical

V

V	volts
V_{cc}	supply voltage; for example, the voltage a computer supplies to its plug-in devices
VDC	volts direct current
VI	virtual instrument—a combination of hardware and/or software elements, typically used with a PC, that has the functionality of a classic standalone instrument
V_{in}	input voltage

W

W	watts
WRT*	write signal

Index

Symbols

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