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NI PXI/PCI-6551/6552 Specifications

50/100 MHz Digital Waveform Generator/Analyzer

このドキュメントには、日本語ページも含まれています。

This document provides the specifications for the NI PXI/PCI-6551 (NI 6551) and the NI PXI/PCI-6552 (NI 6552).

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 6551/6552 specifications, visit `ni.com/manuals`.

To access the NI 6551/6552 documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 6551/6552 signals, navigate to **Start»Programs»National Instruments»NI-HSDIO»Documentation**.

Hot Surface If the NI 6551/6552 has been in use, it may exceed safe handling temperatures and cause burns. Allow time to cool before removing it from the chassis.

Note All values were obtained using a 1 meter cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

NATIONAL INSTRUMENTS

Contents

Channel Specifications

Specification	Value	Comments
Number of data channels	20	—
Direction control of data channels	Per channel, per cycle, bidirectional	—
Number of programmable function interface (PFI) channels	4	Refer to the *Waveform Characteristics* section for more details.
Direction control of PFI channels	Per channel	—
Number of clock terminals	3 input 2 output	Refer to the *Timing Specifications* section for more details.

Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)

Specification	Value	Comments
Generation voltage range	–2.0 V to 5.5 V	Into 1 MΩ
Generation signal type	Single-ended	—
Number of programmable voltage levels	1 voltage low level 1 voltage high level **Note**: While you can only set one voltage low level and one voltage high level for all generation channels, you can set a different voltage low level and voltage high level for all acquisition channels. You can also set the channels to the high-impedance state (tristate).	For all data, CLK OUT (Sample clock only), and PFI channels
Generation voltage range restrictions	–0.5 V to 5.5 V (up to 50 MHz clock rate) –2.0 V to 3.7 V (up to 50 MHz clock rate) –0.5 V to 3.7 V (50 MHz to 100 MHz clock rate; NI 6552 only)	Into 1 MΩ
Generation voltage swing	400 mV to 6 V (up to 50 MHz clock rate) 400 mV to 4.2 V (50 MHz to 100 MHz clock rate; NI 6552 only)	Into 1 MΩ
Generation voltage level resolution	10 mV	Into 1 MΩ
DC generation voltage level accuracy	±20 mV	Into 1 MΩ; does not include system crosstalk
Output impedance	50 Ω nominal	At 25 °C
Output impedance temperature coefficient	0.2 Ω/°C	Typical
Maximum DC drive strength	±50 mA maximum per channel ±600 mA maximum for all data, clock, and PFI channels	—

Specification	Value		Comments
Data channel driver enable/disable control	Per channel per cycle		—
Channel power-on state	**Module Assemblies Labeled A and B**	**Module Assemblies Labeled C and Later**	—
	Drivers disabled, 10 kΩ input impedance	Drivers disabled, 50 kΩ input impedance	
Output protection	The device can indefinitely sustain a short to any voltage in the generation voltage range.		—

Acquisition Channels (Data, STROBE, and PFI <0..3>)

Specification	Value	Comments
Number of voltage comparators per channel	2	—
Acquisition voltage range	–2.0 V to 5.5 V	—
Number of programmable acquisition thresholds	1 voltage low threshold 1 voltage high threshold **Note**: While you can set only one voltage low level and one voltage high level for all acquisition channels, you can set a different voltage low level and voltage high level for all generation channels. You can also set the channels to the high-impedance state (tristate).	For all data, STROBE, and PFI channels
Minimum detectable voltage swing	50 mV	10 kΩ input impedance, measured with 50% duty cycle input signal
Acquisition voltage threshold resolution	10 mV	10 kΩ input impedance

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>DC acquisition voltage threshold accuracy</td><td colspan="2">±30 mV</td><td>10 kΩ input impedance, does not include system crosstalk</td></tr>
<tr><td rowspan="2">Input impedance</td><td>Module Assemblies Labeled A and B</td><td>Module Assemblies Labeled C and Later</td><td rowspan="2">Software-selectable per channel when powered on and within valid voltage range.</td></tr>
<tr><td>50 Ω nominal or
10 kΩ (default)</td><td>50 Ω nominal or
50 kΩ (default)</td></tr>
<tr><td>Input protection</td><td colspan="2">–2.3 V to 6.8 V</td><td>Diode clamps in the design may provide additional protection outside this range.</td></tr>
</table>

Hardware Comparison

Specification	Value	Comments
Error FIFO depth	4,094	For information about fetching error data, refer to the *NI Digital Waveform Generator/ Analyzer Help*.
Number of repeated errors	255	—
Speed (maximum)	**NI 6551**: 50 MHz **NI 6552**: 100 MHz	—

Timing Specifications

Sample Clock

Specification	Value	Comments
Sample clock sources	1. On Board Clock (internal voltage-controlled crystal oscillator (VCXO) with divider) 2. CLK IN (SMB jack connector) 3. PXI_STAR (PXI backplane—PXI only) 4. STROBE (DDC connector; acquisition only)	—
On Board Clock frequency range	**NI 6551**: 48 Hz to 50 MHz Configurable to 200 MHz/*N*, where $4 \le N \le 4{,}194{,}304$ **NI 6552**: 48 Hz to 100 MHz Configurable to 200 MHz/*N*, where $2 \le N \le 4{,}194{,}304$	—
CLK IN frequency range	**NI 6551**: 20 kHz to 50 MHz **NI 6552**: 20 kHz to 100 MHz	Refer to the *CLK IN (SMB Jack Connector)* section for restrictions based on waveform type.
PXI_STAR frequency range (PXI only)	**NI 6551**: 48 Hz to 50 MHz **NI 6552**: 48 Hz to 100 MHz	Refer to the *PXI_STAR (PXI Backplane—PXI only)* section.
STROBE frequency range	**NI 6551**: 48 Hz to 50 MHz **NI 6552**: 48 Hz to 100 MHz	Refer to the *STROBE (DDC Connector)* section.
Sample clock relative delay adjustment	0.0 to 1.0 Sample clock periods	You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	10 ps	

Specification	Value		Comments
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)		Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range (δ_C)	0.0 to 1.0 Sample clock periods		For clock frequencies ≥25 MHz
Exported Sample clock delay resolution (δ_C)	1/256 of Sample clock period		For clock frequencies ≥25 MHz
Exported Sample clock jitter	**Period Jitter**	**Cycle-to-Cycle Jitter**	Typical; using On Board Clock
	20 ps_{rms}	35 ps_{rms}	

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

Specification	Value		Comments
Data channel-to-channel skew	**Typical**	**Maximum**	Across all channels
	±300 ps	±900 ps	
Maximum data channel toggle rate	**NI 6551**: 25 MHz **NI 6552**: 50 MHz		—
Data formats	Non-return to zero (NRZ)		—
Data position modes	Sample Clock Rising Edge, Sample Clock Falling Edge, or Delay from Sample Clock Rising Edge		Per channel
Generation data delay range (δ_G)	0.0 to 1.0 Sample clock periods		Supported for clock frequencies ≥25 MHz
Generation data delay resolution (δ_G)	1/256 of Sample clock period		Supported for clock frequencies ≥25 MHz

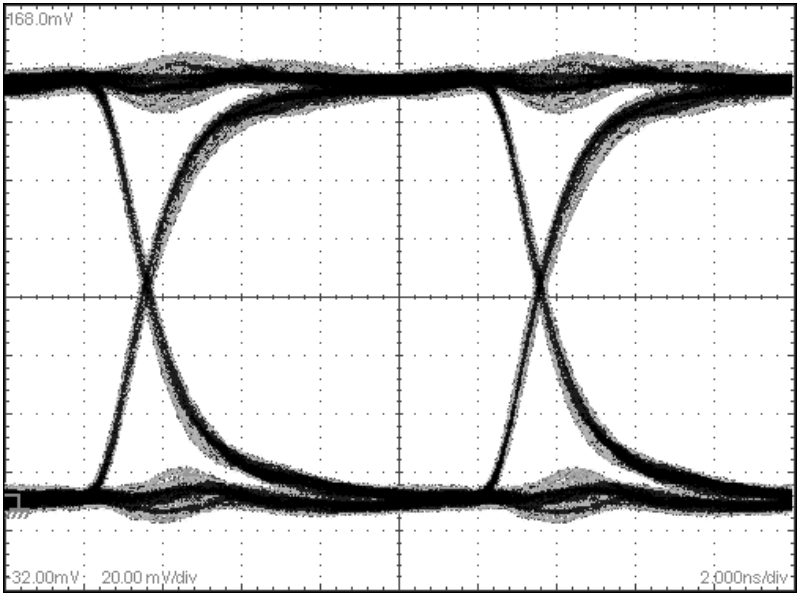
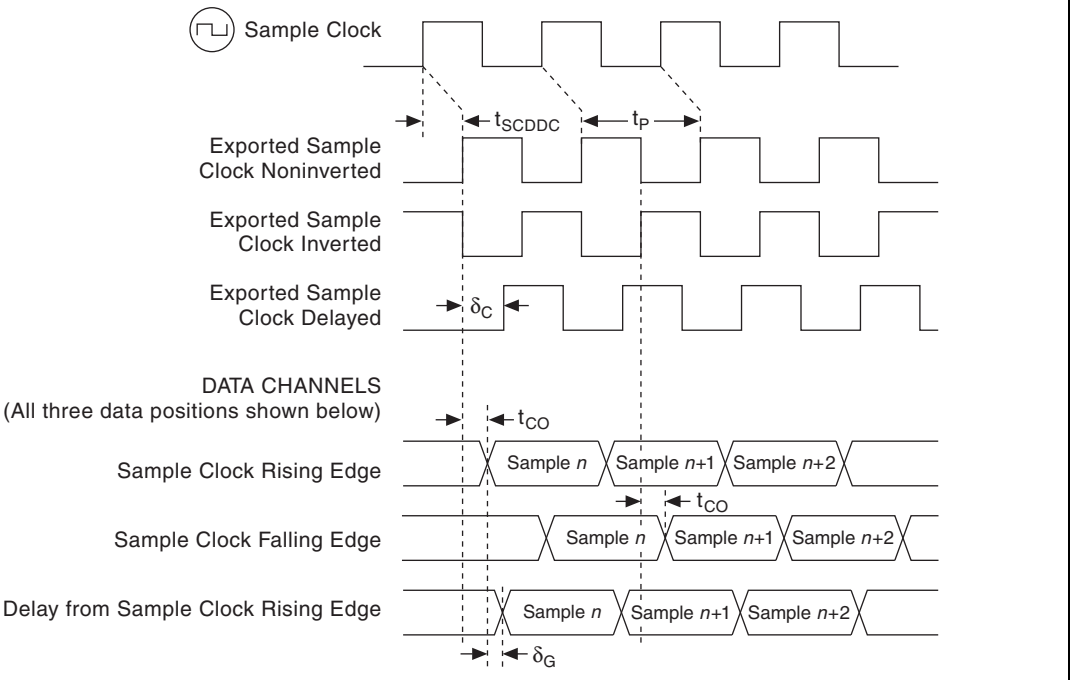


Figure 1. Eye Diagram[1]

Specification	Value		Comments
Rise time (0 V to 3.3 V swing)	**Into 50 Ω**	**Into 1 MΩ**	20% to 80%, typical
	2.25 ns	2.75 ns into 475 pF test system capacitance	
Fall time (0 V to 3.3 V swing)	2.25 ns	2.75 ns into 475 pF test system capacitance	20% to 80%, typical
Exported Sample clock offset (t_{CO})	0 ns or 2.5 ns (default)		Software-selectable
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	32.5 ns		Typical

[1] This eye diagram was captured on DIO 0 (100 MHz clock rate) at 3.3 V at room temperature into 50 Ω termination.



t_{SCDDC} : Time delay from Internal Sample Clock to DDC Connector Exported Sample Clock

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (fraction of t_P)

$0 \le \delta_G \le 1$: Generation Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

t_{CO} = Exported Sample Clock Offset; 0 or 2.5 ns, software-selectable

Figure 2. Generation Timing Diagram

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value		Comments
Data channel-to-channel skew	**Typical**	**Maximum**	Across all channels
	±400 ps	±900 ps	
Minimum detectable pulse width	4 ns		Required at both acquisition voltage thresholds

Specification	Value	Comments
Set-up time to STROBE (t_{SUS})	2.3 ns	Maximum; includes maximum data channel-to-channel skew
Hold time to STROBE (t_{HS})	1.9 ns	Maximum; includes maximum data channel-to-channel skew
Time delay from DDC connector to internal Sample clock (t_{DDCSC})	27.5 ns	Typical
Set-up time to Sample clock (t_{SUSC})	0.4 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Hold time to Sample clock (t_{HSC})	0 ns	Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}
Data position modes	Sample Clock Rising Edge, Sample Clock Falling Edge, or Delay from Sample Clock Rising Edge	Per channel
Acquisition data delay range (δ_A)	0.0 to 1.0 Sample clock periods	For clock frequencies ≥25 MHz
Acquisition data delay resolution (δ_A)	1/256 of Sample clock period	For clock frequencies ≥25 MHz

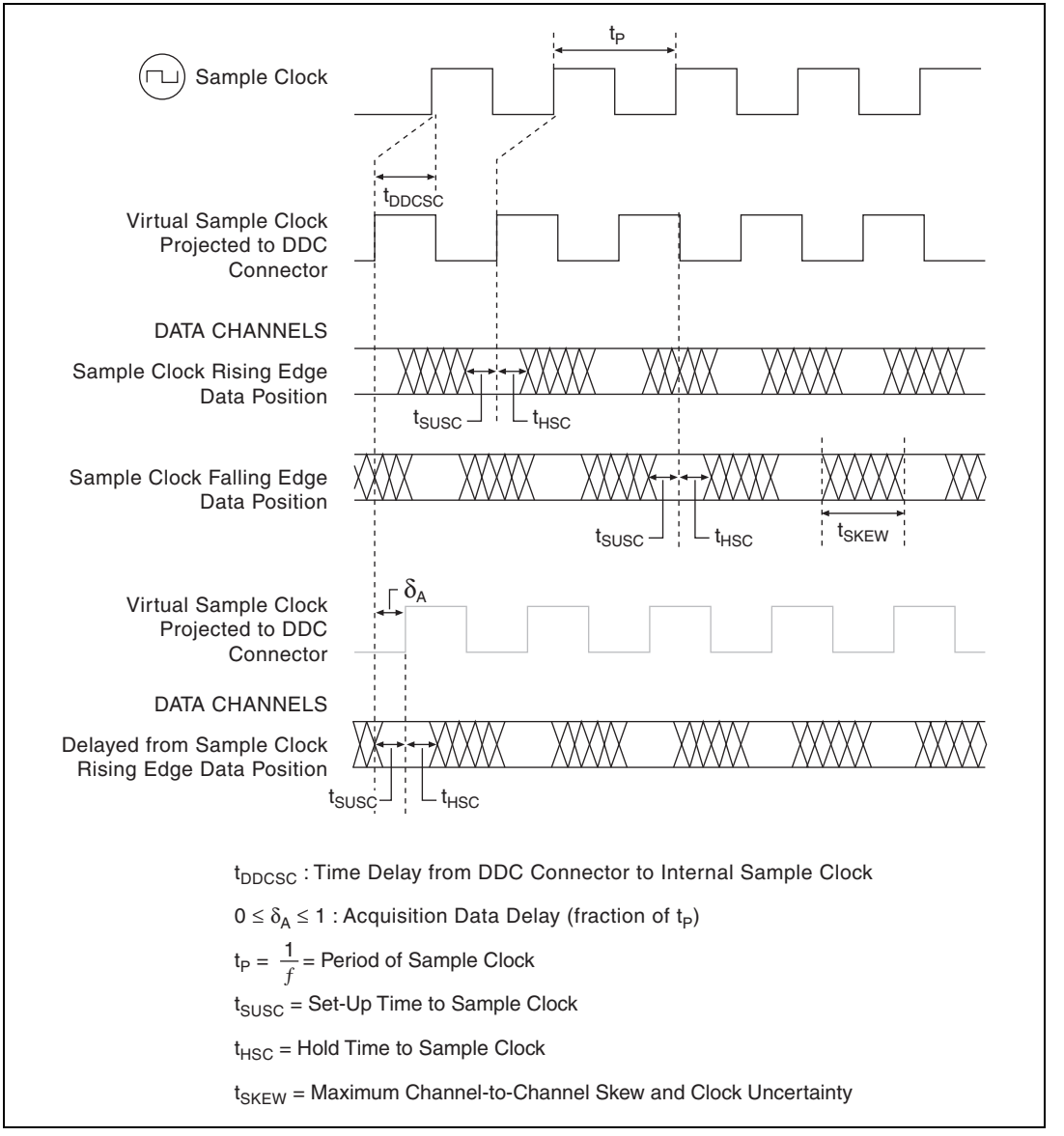


Figure 3. Acquisition Timing Diagram

Note Provided set-up and hold times account for maximum channel-to-channel skew and jitter.

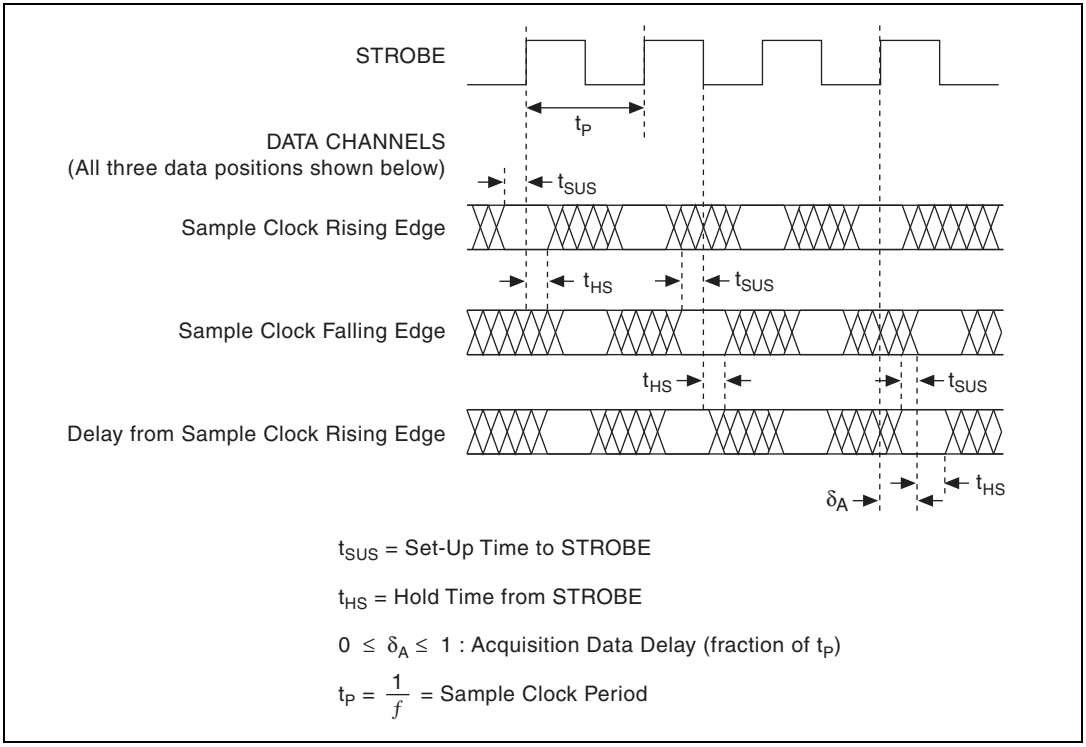


Figure 4. Acquisition Timing Diagram Using STROBE as the Sample Clock

CLK IN (SMB Jack Connector)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Reference clock (for the phase lock loop (PLL)) 2. Sample clock	—
Input coupling	AC	—
Input protection	±10 VDC	—
Input impedance	50 Ω (default) or 1 kΩ	Software-selectable
Minimum detectable pulse width	4 ns	Required at V_{rms} mean
Clock requirements	Clock must be continuous and free-running	—

Specification	Value				Comments
As Sample clock					
External Sample clock requirements	**Square Waves**				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}			—
	Frequency range	**NI 6551**: 20 kHz to 50 MHz			—
		NI 6552: 20 kHz to 100 MHz			—
	Duty cycle range	f < 50 MHz: 25% to 75% f ≥ 50 MHz: 40% to 60%			—
	Sine Waves				—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	1.0 V_{pp} to 5.0 V_{pp}	2.0 V_{pp} to 5.0 V_{pp}	—
	Frequency range	**NI 6551**: 5.5 MHz to 50 MHz	**NI 6551**: 3.5 MHz to 50 MHz	**NI 6551**: 1.8 MHz to 50 MHz	—
		NI 6552: 5.5 MHz to 100 MHz	**NI 6552**: 3.5 MHz to 100 MHz	**NI 6552**: 1.8 MHz to 100 MHz	—
As Reference Clock					
Reference clock frequency range	10 MHz ± 50 ppm				—
Reference clock voltage range	0.65 V_{pp} to 5.0 V_{pp}				—
Reference clock duty cycle	25% to 75%				—

STROBE (DDC Connector)

Specification	Value		Comments
Direction	Input into device		—
Destinations	Sample clock (acquisition only)		—
STROBE frequency range	**NI 6551**: 48 Hz to 50 MHz **NI 6552**: 48 Hz to 100 MHz		—
STROBE duty cycle range	**NI 6551**: 25% to 75% **NI 6552**: $f \leq$ 50 MHz: 25% to 75% $f >$ 50 MHz: 40% to 60%		At the programmed thresholds
Minimum detectable pulse width	4 ns		Required at both acquisition voltage thresholds
Voltage thresholds	Refer to the *Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.		—
Clock requirements	Clock must be continuous and free-running.		—
Input impedance	**Module Assemblies Labeled A and B**	**Module Assemblies Labeled C and Later**	Software-selectable
	50 Ω or 10 kΩ (default)	50 Ω or 50 kΩ (default)	

PXI_STAR (PXI Backplane—PXI only)

Specification	Value	Comments
Direction	Input into device	—
Destinations	1. Sample clock 2. Start trigger 3. Reference trigger (acquisition sessions only) 4. Advance trigger (acquisition sessions only) 5. Pause trigger (generation sessions only) 6. Script trigger (generation sessions only)	—

Specification	Value	Comments
PXI_STAR frequency range	**NI 6551**: 48 Hz to 50 MHz **NI 6552**: 48 Hz to 100 MHz	—
Clock requirements	Clock must be continuous and free-running.	—

CLK OUT (SMB Jack Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω nominal	—
As Sample Clock		
Electrical characteristics	Refer to the *Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)* specifications in the *Channel Specifications* section.	—
As Reference Clock		
Maximum drive current	24 mA	—
Logic type	3.3 V CMOS	—

DDC CLK OUT (DDC Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock	STROBE cannot be routed to DDC CLK OUT
Electrical characteristics	Refer to the *Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK10 (PXI backplane—PXI only) 2. RTSI 7 (RTSI bus—PCI only) 3. CLK IN (SMB jack connector) 4. None (On Board Clock not locked to a reference)	Provides the reference frequency for the PLL
Lock time	400 ms	Typical
Reference clock frequencies	10 MHz ± 50 ppm	—
Reference clock duty cycle	25% to 75%	—
Reference clock destinations	CLK OUT (SMB jack connector)	—

Waveform Characteristics

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 6551/6552 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *NI Digital Waveform Generator/ Analyzer Help* for more information.
Onboard memory size	1 Mbit/channel for generation sessions 1 Mbit/channel for acquisition sessions	8 Mbit/channel for generation sessions 8 Mbit/channel for acquisition sessions	64 Mbit/channel for generation sessions 64 Mbit/channel for acquisition sessions	Maximum limit for generation sessions assumes no scripting instructions.

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Generation modes</td><td colspan="3">Single-waveform mode: Generate a single waveform once, N times, or continuously.

Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.</td><td>—</td></tr>
<tr><td rowspan="5">Generation minimum waveform size</td><td rowspan="2">Configuration</td><td colspan="2">Sample Rate</td><td rowspan="5">Sample rate dependent. Increasing sample rate increases minimum waveform size requirement.

For information about these configurations, refer to the Common Scripting Use Cases topic in the NI Digital Waveform Generator/ Analyzer Help.</td></tr>
<tr><td>100 MHz (NI 6552 only)</td><td>50 MHz</td></tr>
<tr><td>Finite waveform</td><td>2 S</td><td>2 S</td></tr>
<tr><td>Continuous waveform</td><td>32 S</td><td>16 S</td></tr>
<tr><td>Stepped triggered script</td><td>128 S</td><td>64 S</td></tr>
<tr><td>Burst triggered script</td><td>512 S</td><td>256 S</td></tr>
<tr><td>Generation finite repeat count</td><td colspan="3">1 to 16,777,216</td><td>—</td></tr>
<tr><td>Generation waveform quantum</td><td colspan="3">Waveform size must be an integer multiple of 2 S.</td><td>Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.</td></tr>
</table>

Specification	Value	Comments
Acquisition minimum record size	1 S	—
Acquisition record quantum	1 record	—
Acquisition maximum number of records	2,147,483,647	—
Acquisition number of pre-Reference trigger samples	0 up to full record	—
Acquisition number of post-Reference trigger samples	0 up to full record	—

Triggers (Inputs to the NI 6551/6552)

<table>
<tr><th>Specification</th><th colspan="3">Values</th><th>Comments</th></tr>
<tr><td>Trigger types</td><td colspan="3">1. Start trigger
2. Pause trigger
3. Script trigger (generation sessions only)
4. Reference trigger (acquisition sessions only)
5. Advance trigger (acquisition sessions only)</td><td>—</td></tr>
<tr><td>Sources</td><td colspan="3">1. PFI 0 (SMB jack connector)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)
4. PXI_STAR (PXI backplane—PXI only)
5. Pattern match (acquisition sessions only)
6. Software (user function call)
7. Disabled (do not wait for a trigger)</td><td>—</td></tr>
<tr><td>Trigger detection</td><td colspan="3">1. Start trigger (edge detection: rising or falling)
2. Pause trigger (level detection: high or low)
3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low)
4. Reference trigger (edge detection: rising or falling)
5. Advance trigger (edge detection: rising or falling)</td><td>—</td></tr>
<tr><td rowspan="2">Minimum required trigger pulse width</td><td colspan="2">Generation Triggers</td><td>Acquisition Triggers</td><td rowspan="2">—</td></tr>
<tr><td colspan="2">30 ns</td><td>Acquisition triggers must meet set-up and hold time requirements.</td></tr>
<tr><td rowspan="2">Trigger rearm time</td><td>Start to Reference Trigger</td><td>Start to Advance Trigger</td><td>Reference to Reference Trigger</td><td rowspan="2">—</td></tr>
<tr><td>57 S, typical;
64 S maximum</td><td>138 S, typical;
143 S, maximum</td><td>132 S, typical;
153 S, maximum</td></tr>
</table>

<table>
<tr><th>Specification</th><th colspan="2">Values</th><th>Comments</th></tr>
<tr><td>Destinations</td><td colspan="2">1. PFI 0 (SMB jack connectors)
2. PFI <1..3> (DDC connector)
3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)</td><td>Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.</td></tr>
<tr><td rowspan="2">Delay from Pause trigger to Paused state</td><td>Generation Sessions</td><td>Acquisition Sessions</td><td>—</td></tr>
<tr><td>32 Sample clock periods + 150 ns</td><td>Synchronous to the data</td><td>Use the Data Active event during generation to determine when the NI 6551/6552 enters the Pause state.</td></tr>
<tr><td>Delay from trigger to digital data output</td><td colspan="2">32 Sample clock periods + 160 ns</td><td>—</td></tr>
</table>

Events (Output from the NI 6551/6552)

Specification	Value	Comments
Event type	1. Marker <0..3> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event 4. Ready for Advance event (acquisition sessions only) 5. End of Record event (acquisition sessions only) 6. Sample Error event (hardware comparison sessions only) 7. Delayed Data Active event (hardware comparison sessions only)	—
Destinations	1. PFI 0 (SMB jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI backplane—PXI only)/ RTSI <0..7> (RTSI bus—PCI only)	Each event, except the Data Active event, can be routed to any destination. The Data Active event can only be routed to PFI channels.
Marker time resolution (placement)	Markers must be placed at an integer multiple of 2 S	—

Calibration

Specification	Value	Comments
Interval for external calibration	2 years	—
Warm-up time	15 minutes	—
Onboard calibration voltage reference		
Temperature coefficient	±5 ppm/°C	—
Long-term stability	90 ppm/$\sqrt{\text{kHr}}$	Typical
On Board Clock characteristics (only valid when PLL reference source is set to None)		
Frequency accuracy	±100 ppm	Typical
Temperature stability	±30 ppm	Typical
Aging	±5 ppm first year	Typical

Power

Specification	Value			Comments
	Typical	Maximum		
		PXI	PCI	
+3.3 VDC	2.0 A	2.0 A	2.0 A	—
+5 VDC	1.8 A	2.3 A	2.4 A	—
+12 VDC	0.3 A	0.5 A	0.5 A	—
–12 VDC	0.2 A	0.2 A	0.2 A	—
Total power	21.6 W	26.5 W	27.0 W	—

Software Specifications

Specification	Value	Comments
Driver software	NI-HSDIO driver software. NI-HSDIO allows you to configure, control, and calibrate the NI 6551/6552. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI API guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments (ADEs): • National Instruments LabVIEW • National Instruments LabWindows™/CVI™ • Microsoft Visual C/C++	Refer to the *NI-HSDIO Instrument Driver Readme* for more information about supported ADE versions.
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6551/6552. MAX is included on the NI-HSDIO driver DVD.	—

Environment

Note To ensure that the NI 6551/6552 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the device. The NI 6551/6552 is intended for indoor use only.

Specification	Value		Comments
Operating temperature	**PXI**	**PCI**	
	0 ºC to +55 ºC in all NI PXI chassis except the following: 0 ºC to +45 ºC when installed in an NI PXI-1000/B and NI PXI-101*x* chassis (Meets IEC-60068-2-1 and IEC-60068-2-2.)	0 ºC to +45 ºC	—
Storage temperature	–20 °C to 70 °C		—

Specification	Value	Comments
Operating relative humidity	10% to 90% relative humidly, noncondensing (Meets IEC-60068-2-56.)	—
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC-60068-2-56.)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	PXI only
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	PXI only
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC-60068-2-64.)	PXI only
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	PXI only
Altitude	0 m to 2,000 m above sea level (at 25 ºC ambient temperature)	—
Pollution Degree	2	—

Specification	Value	Comments
Safety	The NI 6551/6552 meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use: • IEC 61010-1, EN 61010-1 • UL 61010-1, CSA 61010-1	For UL and other safety certifications, refer to the product label or visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the *Certification* column.
Electromagnetic Compatibility	The NI 6551/6552 meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use: • EN 61326-1 (IEC 61326-1): Class A emissions, Basic immunity • EN 55011 (CISPR 11): Group 1, Class A emissions • AS/NZS CISPR 11: Group 1, Class A emissions • FCC 47 CFR Part 15B: Class A emissions • ICES-001: Class A emissions For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section of this document. To meet EMC compliance the following cautions apply: **Caution** The SHC68-C68-D4 or SHC68-C68-D2 shielded cables must be used when operating the NI 6551/6552. **Caution** EMI filler panels (NI P/N 778700-01) must be installed in all empty slots of the NI 6551/6552.	

CE Compliance	This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows: • 2006/95/EC; Low-Voltage Directive (safety) • 2004/108/EC; Electromagnetic Compatibility Directive (EMC)	CE
Online Product Certification	Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the *Certification* column.	—
Environmental Management	NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers. For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document	—
Waste Electrical and Electronic Equipment (WEEE)	**EU Customers**: At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit `ni.com/environment/weee`.	

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。
关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。
(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Physical Specifications

Specification	Value		Comments
Dimensions	**PXI**	**PCI**	
	18.6 cm × 13.1 cm (7.32 in. × 5.16 in.) Single 3U CompactPCI slot; PXI compatible	12.6 cm × 35.5 cm (4.95 in. × 13.9 in.)	—
Weight	375 g (13.2 oz)		—
Front Panel Connectors			
Label	**Function(s)**	**Connector Type**	—
CLK IN	External Sample clock, external PLL reference input	SMB jack connector	—
PFI 0	Events, triggers	SMB jack connector	—
CLK OUT	Exported Sample clock, exported Reference clock	SMB jack connector	—
DIGITAL DATA & CONTROL	Digital data channels, exported Sample clock, STROBE, events, triggers	68-pin VHDCI connector	—