PCI-6551

SPECIFICATIONS

PCI-6551

50 MHz, 20-Channel Digital Waveform Device

These specifications apply to the PCI-6551 with 1 MBit, 8 MBit, and 64 MBit of memory per channel.

Hot Surface If the PCI-6551 has been in use, it may exceed safe handling temperatures and cause burns. Allow the PCI-6551 to cool before removing it from the chassis.

Note All values were obtained using a 1 m cable (SHC68-C68-D4 recommended). Performance specifications are not guaranteed when using longer cables.

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

The following characteristic specifications describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Conditions

Typical values are representative of an average unit operating at room temperature.

Channels

Data	
Number of channels	20
Direction control	Per channel Per cycle Bidirectional
Programmable Function Interface (PFI)	
Number of channels	4
Direction control	Per channel
Clock terminals	
Input	3
Output	2

Generation Channels

Channels	Data DDC CLK OUT PFI <0..3>
Signal type	Single-ended
Total programmable voltage levels[1]	1 voltage low level 1 voltage high level
Generation voltage features (into 1 MΩ)	
Range	-2.0 V to 5.5 V
Range restrictions[2]	-0.5 V to 5.5 V -2.0 V to 3.7 V
Swing	400 mV to 6 V (up to 50 MHz clock rate)
Level resolution	10 mV
DC generation accuracy	±20 mV (does not include system crosstalk)
Output impedance	
Magnitude	50 Ω (at 25 °C), nominal
Temperature coefficient	0.2 Ω/°C, typical
Maximum DC drive strength	
Per channel	±50 mA
All data, clock, and PFI channels	±600 mA
Data channel driver enable/disable control	Per channel Per cycle
Channel power-on state[3]	Drivers disabled, 50 kΩ input impedance
Output protection	
Range	-2.0 V to 5.5 V
Duration	Indefinite

1 For all data, CLK OUT (Sample clock only), and PFI channels: while you can only set one voltage low level and one voltage high level for all generation channels, you can set a different low voltage low level and voltage high level for all acquisition channels. You can also set the channels to the high-impedance state (tristate).
2 Up to 50 MHz clock rate.
3 For module assemblies C and later. Module assemblies A and B have an input impedance of 10 kΩ.

Acquisition Channels

Channels	Data STROBE PFI <0..3>
Voltage comparators per channel	2
Total programmable thresholds[4]	1 voltage low threshold 1 voltage high threshold
Voltage range	-2.0 V to 5.5 V
Voltage characteristics (10 kΩ input impedance)	
Minimum detectable swing[5]	50 mV
Threshold resolution	10 mV
DC threshold accuracy[6]	±30 mV
Input impedance[7]	50 Ω nominal or 50 kΩ (default)
Input protection range[8]	-2.3 V to 6.8 V

Hardware Comparison

Error FIFO depth	4,094
Number of repeated errors	255
Speed	50 MHz, maximum

Timing

Sample Clock

Sources	1. On Board clock (internal voltage-controlled crystal oscillator [VCXO] with divider) 2. CLK IN (SMB jack connector) 3. STROBE (DDC connector; acquisition only)

[4] While you can set only one voltage low level and one voltage high level for all acquisition channels, you can set a different voltage low level and voltage high level for all generation channels. You can also set the channels to a high-impedance state (tristate).
[5] Measured with 50% duty cycle input signal.
[6] Does not include system crosstalk.
[7] Software-selectable per channel when powered on and within valid range. For module assembly revisions C and later. Module assemblies A and B have an input impedance of 50 Ω nominal or or 10 kΩ (default).
[8] Diode clamps in the design may provide additional protection outside the specified range.

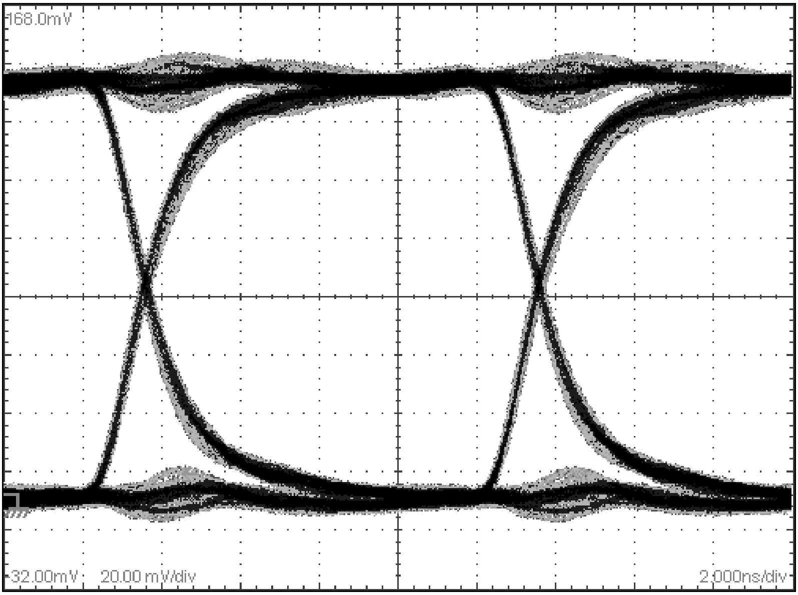
Frequency range	
On Board clock	48 Hz to 50 MHz, Configurable to 200 MHz/N; where $4 \leq N \leq 4{,}194{,}304$
CLK IN	20 kHz to 50 MHz
STROBE	48 Hz to 50 MHz
Relative delay adjustment[9]	
Range	0.0 to 1.0 Sample clock periods
Resolution	10 ps
Exported Sample clock	
Destinations[10]	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMB jack connector)
Delay (δ_C), for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period
Jitter, using On Board clock	
Period	20 ps_{rms}, typical
Cycle-to-cycle	35 ps_{rms}, typical

Generation Timing

Channels	Data DDC CLK OUT PFI <0..3>
Data channel-to-channel skew	±300 ps, typical ±900 ps, maximum
Maximum data channel toggle rate	25 MHz
Data format	Non-return to zero (NRZ)
Data position modes	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge
Generation data delay (δ_G), for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period

9 You can apply a delay or phase adjustment to the On Board clock to align multiple devices.
10 Sample clocks with sources other than STROBE can be exported.

Figure 1. Eye Diagram

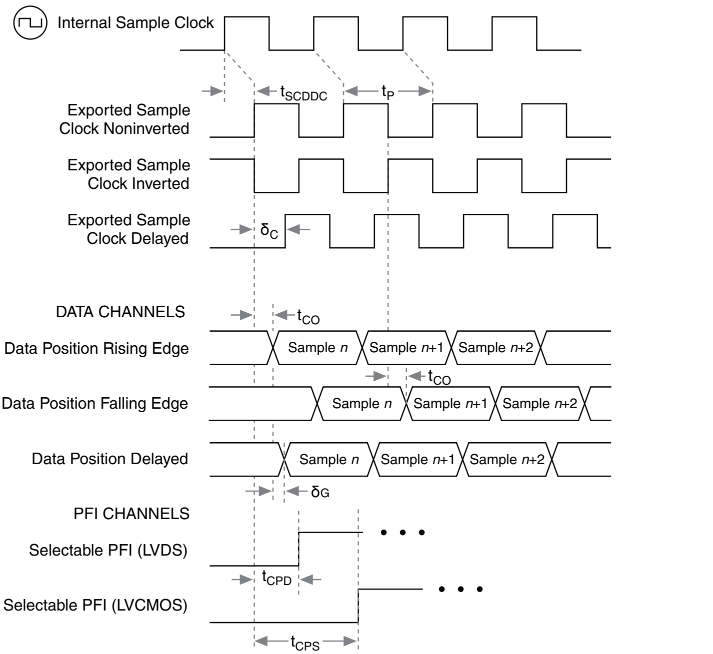


Note This eye diagram was captured on DIO 0 (100 MHz clock rate) at 3.3 V at room temperature into 50 Ω termination.

Rise and fall times, 0 V to 3.3 V swing[11]	
Into 50 Ω	
Rise time	2.25 ns
Fall time	2.25 ns
Into 1 MΩ and 475 pF test system capacitance	
Rise time	2.75 ns
Fall time	2.75 ns
Exported Sample clock offset (t_{CO})	Software-selectable: 0 ns or 2.5 ns (default)
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	32.5 ns, typical

[11] 20% to 80%, typical.

Figure 2. Generation Timing Diagram



t_{SCDDC} = Time Delay from Sample Clock (Internal) to DDC Connector Exported Sample Clock

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (Fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{CO} = Exported Sample Clock Offset

t_{CPD} = Exported Sample Clock to Selectable PFI Offset (LVDS)

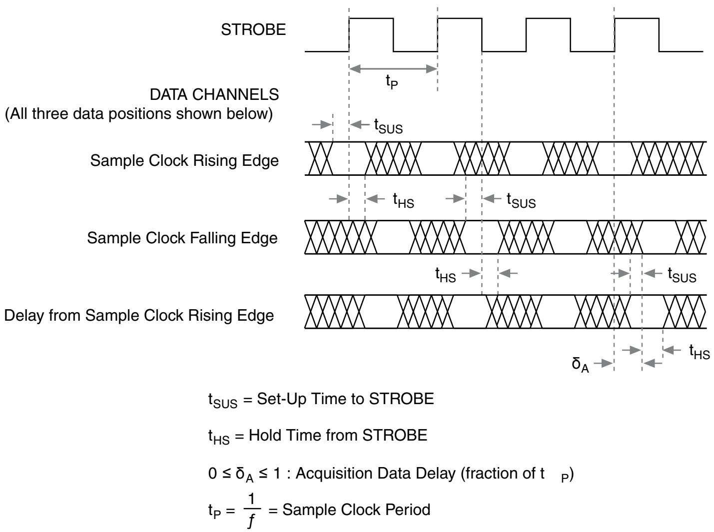
t_{CPS} = Exported Sample Clock to Selectable PFI Offset (LVCMOS)

Acquisition Timing

Channels	Data STROBE PFI <0..3>
Channel-to-channel skew	±400 ps, typical ±900 ps, maximum
Data position modes, per channel	Sample clock rising edge Sample clock falling edge Delay from Sample clock rising edge

Minimum detectable pulse width[12]	4 ns
Setup and hold times	
To STROBE[13]	
Setup time (t_{SUS})	2.3 ns, maximum
Hold time (t_{HS})	1.9 ns, maximum
To Sample clock[14]	
Setup time (t_{SUSC})	0.4 ns
Hold time (t_{HSC})	0 ns
Time delay from DDC connector data to internal Sample clock (t_{DDCSC})	27.5 ns, typical
Acquisition data delay (δ_A), for clock frequencies ≥25 MHz	
Range	0.0 to 1.0 Sample clock periods
Resolution	1/256 of Sample clock period

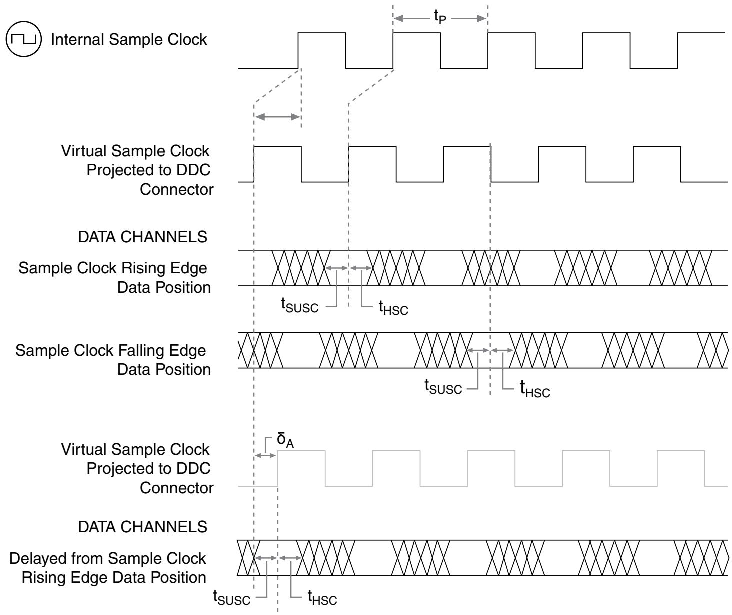
Figure 3. Acquisition Timing Diagram Using STROBE as the Sample Clock



Note Provided setup and hold times account for maximum channel-to-channel skew and jitter.

[12] Required at both acquisition voltage thresholds.
[13] Includes maximum data channel-to-channel skew.
[14] Does not include data channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}.

Figure 4. Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \leq \delta_A \leq 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

CLK IN

Connector	SMB jack
Direction	Input
Destinations	1. Reference clock for the phase-locked loop (PLL) 2. Sample clock
Input coupling	AC
Input protection	±10 VDC
Input impedance	Software-selectable: 50 Ω (default) or 1 kΩ

Minimum detectable pulse width[15]	4 ns
Clock requirements	Free-running (continuous) clock

As Sample Clock

Table 1. External Sample Clock Range

Voltage Range ($V_{pk\text{-}pk}$)	Sine Wave	Square Wave	
	Frequency Range	Frequency Range	Duty Cycle
0.65 to 5.0	5.5 MHz to 50 MHz	20 kHz to 50 MHz	25% to 75%
1.0 to 5.0	3.5 MHz to 50 MHz	—	—
2.0 to 5.0	1.8 MHz to 50 MHz	—	—

As Reference Clock

Frequency range	10 MHz ±50 ppm
Voltage range	0.65 $V_{pk\text{-}pk}$ to 5.0 $V_{pk\text{-}pk}$
Duty cycle	25% to 75%

STROBE

Connector	DDC
Direction	Input
Destinations	Sample clock (acquisition only)
Frequency range	48 Hz to 50 MHz
Duty cycle range[16]	25% to 75%
Minimum detectable pulse width[17]	4 ns
Voltage thresholds	Refer to *Acquisition Timing* in the *Timing* section.
Clock requirements	Free-running (continuous) clock
Input impedance[18]	Software-selectable: 50 Ω or 50 kΩ (default)

15 Required at V_{rms} mean.
16 At the programmed thresholds.
17 Required at both acquisition voltage thresholds.
18 For module assemblies C and later. Module assemblies A and B have an input impedance of 50 Ω or 10 kΩ (default).

CLK OUT

Connector	SMB jack
Direction	Output
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)
Output impedance	50 Ω, nominal
As Sample clock	
Electrical characteristics	Refer to *Generation Channels* in the *Channels* section.
As Reference clock	
Maximum drive current	24 mA
Logic type	3.3 V CMOS

DDC CLK OUT

Connector	DDC
Direction	Output
Source[19]	Sample clock
Electrical characteristics	Refer to *Generation Timing* in the *Timing* section.

Reference Clock (PLL)

Sources[20]	1. RTSI 7 2. CLK IN (SMB jack connector) 3. None (On Board clock not locked to a reference)
Destination	CLK OUT (SMB jack connector)
Lock time	400 ms, typical
Frequencies	10 MHz ±50 ppm
Duty cycle range	25% to 75%

19 STROBE cannot be routed to DDC CLK OUT.
20 The source provides the reference frequency for the PLL.

Waveform

Memory and Scripting

Memory architecture	The PCI-6551 uses Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user defined.
Onboard memory size[21]	
1 Mbit/channel	
Acquisition	1 Mbit/channel (4 MBytes total)
Generation	1 Mbit/channel (4 MBytes total)
8 Mbit/channel	
Acquisition	8 Mbit/channel (32 MBytes total)
Generation	8 Mbit/channel (32 MBytes total)
64 Mbit/channel	
Acquisition	64 Mbit/channel (256 MBytes total)
Generation	64 Mbit/channel (256 MBytes total)
Generation	
Single waveform mode	Generates a single waveform once, *n* times, or continuously.
Scripted mode[22]	Generates a simple or complex sequences of waveforms.
Finite repeat count	1 to 16,777,216
Waveform quantum[23]	Waveform must be an integer multiple of 2 S (samples).

21 Maximum limit for generation sessions assumes no scripting instructions.
22 Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.
23 Regardless of waveform size, NI-HSDIO allocates waveforms into block sizes of 32 S of physical memory.

Table 2. Generation Minimum Waveform Size, Samples (S)[24]

Configuration	Sample Rate
	50 MHz
Single waveform	2 S
Continuous waveform	16 S
Stepped sequence	64 S
Burst sequence	256 S

Acquisition	
Minimum record size[25]	1 S
Record quantum	1 S
Total records	2,147,483,647, maximum
Total pre-Reference trigger samples	0 up to full record
Total post-Reference trigger samples	0 up to full record

Triggers

Trigger Types	Sessions	Edge Detection	Level Detection
1. Start	Acquisition and generation	Rising or Falling	—
2. Pause	Acquisition and generation	—	High or Low
3. Script <0..3>	Generation	Rising or Falling	High or Low

[24] Sample rate dependent. Increasing sample rate increases minimum waveform size.
[25] Regardless of waveform size, NI-HSDIO allocates at least 128 bytes for a record.

Trigger Types	Sessions	Edge Detection	Level Detection
4. Reference	Acquisition	Rising or Falling	—
5. Advance	Acquisition	Rising or Falling	—

Sources	PFI 0 (SMB jack connector) PFI <1..3> (DDC Connector) RTSI <0..7> (RTSI bus) Pattern match (acquisition sessions only) Software (user function call) Disabled (do not wait for a trigger)
Destinations[26]	PFI 0 (SMB jack connectors) PFI <1..3> (DDC connector) RTSI <0..6> (RTSI bus)
Minimum required trigger pulse width	
Generation	30 ns
Acquisition	Acquisition triggers must meet setup and hold time requirements.

Table 3. Trigger Rearm Time

Trigger Operation	Samples, Typical	Sample, Maximum
Start to Reference	57 S	64 S
Start to Advance	138 S	143 S
Reference to Reference	132 S	153 S

Delay from Pause trigger to Pause state[27]	
Generation sessions	32 Sample clock periods + 150 ns
Acquisition sessions	Data synchronous
Delay from trigger to digital data output	32 Sample clock periods + 160 ns

[26] Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported for acquisition sessions.

[27] Use the Data Active event during generation to determine when the PCI-6551 enters the Pause state.

Events

Types	Sessions
1. Marker <0..3>	Generation
2. Data Active	Generation
3. Ready for Start	Acquisition and generation
4. Ready for Advance	Acquisition
5. End of Record	Acquisition
6. Sample Error	Hardware comparison
7. Delayed Data Active	Hardware comparison

Destinations[28]	1. PFI 0 (SMB jack connector) 2. PFI <1..3> (DDC connector) 3. RTSI <0..7> (RTSI bus)
Marker time resolution (placement)	Markers must be placed at an integer multiple of 2 S (samples).

Calibration

Interval for external calibration	2 years
Warm-up time	15 minutes
Onboard calibration voltage reference	
Temperature coefficient	±5 ppm/°C
Long-term stability	90 ppm/$\sqrt{kHr}$, typical
On Board clock characteristics (valid only when PLL reference source is set to None)	
Frequency accuracy	±100 ppm, typical
Temperature stability	±30 ppm, typical
Aging	±5 ppm first year, typical

28 Except for the Data Active event, each event can be routed to any destination. The Data Active event can be routed only to the PFI channels.

Software

Driver Software

Driver support for this device was first available in NI-HSDIO 1.0.

NI-HSDIO is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-6551. NI-HSDIO provides application programming interfaces for many development environments.

Application Software

NI-HSDIO provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

NI Measurement Automation Explorer

NI Measurement Automation Explorer (MAX) provides interactive configuration and test tools for the PCI-6551. MAX is included on the NI-HSDIO media.

Power

VDC	Current Draw, Typical	Current Draw, Maximum
+3.3 V	2.0 A	2.0 A
+5 V	1.8 A	2.4 A
+12 V	0.3 A	0.5 A
-12 V	0.2 A	0.2 A

Total power	21.6 W, typical 27 W, maximum

Physical Specifications

Dimensions	12.6 cm × 35.5 cm (4.95 in × 13.9 in)
Weight	375 g (13.2 oz)

I/O Connectors

Label	Connector Type	Description
CLK IN	SMB jack	External Sample clock, external PLL reference input
PFI 0		Events, triggers
CLK OUT		Exported Sample clock, exported Reference clock
DIGITAL DATA & CONTROL	68-pin VHDCI connector	Digital data channels, exported Sample clock, STROBE, events, triggers

Environment

Note To ensure that the PCI-6551 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the PCI-6551 or available at *ni.com/manuals*. The PCI-6551 is intended for indoor use only.

Operating temperature	0 °C to 45 °C
Operating relative humidity	10 to 90% relative humidity, noncondensing (meets IEC 60068-2-56)
Storage temperature	-20 °C to 70 °C (meets IEC 60068-2-2)
Storage relative humidity	5 to 95% relative humidity, noncondensing (meets IEC 60068-2-56)
Altitude	0 to 2,000 m above sea level (at 25 °C ambient temperature)
Pollution degree	2

Compliance and Certifications

Safety

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations, certifications, and additional information, refer to the *Online Product Certification* section.

To meet EMC compliance, the following cautions apply:

Caution The SHC68-C68-D4 shielded cables must be used when operating the PCI-6551.

Caution EMC filler panels must be installed in all empty chassis slots.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit *ni.com/certification*, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

373309F-01 November 3, 2017