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NI PXI-5441 Specifications

16-Bit 100 MS/s Arbitrary Waveform Generator with Onboard Signal Processing (OSP)

このドキュメントには、日本語ページも含まれています。

This document lists specifications for the NI PXI-5441 arbitrary waveform generator. Unless otherwise noted, the following conditions were used for each specification:

- Analog filter enabled.
- DAC interpolation set to maximum allowed factor for a given sample rate.
- Signals terminated with 50 Ω.
- Direct path set to 1 V_{pk-pk}, Low-Gain Amplifier path set to 2 V_{pk-pk}, and High-Gain Amplifier path set to 12 V_{pk-pk}.
- Sample clock set to 100 mega samples per second (MS/s).

Specifications describe the warranted, traceable product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under Specifications or Typical values. Nominal values are not covered by warranty.

Specifications are subject to change without notice. For the most recent NI 5441 specifications, visit `ni.com/manuals`. To access all the NI 5441 documentation, navigate to **Start»All Programs»National Instruments»NI-FGEN»Documentation**.

NATIONAL INSTRUMENTS

Hot Surface If the NI 5441 has been in use, it may exceed safe handling temperatures and cause burns. Allow the NI 5441 to cool before removing it from the chassis.

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) as stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in its intended operational electromagnetic environment.

This product is intended for use in industrial locations. There is no guarantee that harmful interference will not occur in a particular installation, when the product is connected to a test object, or if the product is used in residential areas. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with the instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Caution When operating this product, use shielded cables and accessories.

Contents

CH 0
(Channel 0 Analog Output, Front Panel Connector)

Specification	Value	Comments
Number of Channels	1	—
Connector	SMB (jack)	—
Output Voltage Characteristics		
Output Paths	1. The software-selectable Main Output path setting provides full-scale voltages from 12.00 V_{pk-pk} to 5.64 mV_{pk-pk} into a 50 Ω load. NI-FGEN uses either the Low-Gain Amplifier or the High-Gain Amplifier when the Main Output path is selected, depending on the Gain attribute. 2. The software-selectable Direct path is optimized for intermediate frequency (IF) applications and provides full-scale voltages from 0.707 to 1.000 V_{pk-pk}.	—
DAC Resolution	16 bits	—

Specification	Value				Comments
Amplitude and Offset					
Amplitude Range	Path	Load	Amplitude (V_{pk-pk})		Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used. NI-FGEN compensates for user-specified resistive loads.
			Minimum Value	Maximum Value	
	Direct	50 Ω	0.707	1.00	
		1 kΩ	1.35	1.91	
		Open	1.41	2.00	
	Low-Gain Amplifier	50 Ω	0.00564	2.00	
		1 kΩ	0.0107	3.81	
		Open	0.0113	4.00	
	High-Gain Amplifier	50 Ω	0.0338	12.0	
		1 kΩ	0.0644	22.9	
		Open	0.0676	24.0	
Amplitude Resolution	<0.06% (0.004 dB) of amplitude range				—
Offset Range	Span of ±25% of the amplitude range with increments <0.0014% of amplitude range				Not available on the Direct path.
Maximum Output Voltage					
Maximum Output Voltage	Path	Load	Maximum Output Voltage (V_{pk})		The maximum output voltage of the NI 5441 is determined by the amplitude range and the offset range.
	Direct	50 Ω	±0.500		
		1 kΩ	±0.953		
		Open	±1.000		
	Low-Gain Amplifier	50 Ω	±1.000		
		1 kΩ	±1.905		
		Open	±2.000		
	High-Gain Amplifier	50 Ω	±6.000		
		1 kΩ	±11.43		
		Open	±12.00		

Specification	Value	Comments
Accuracy		
DC Accuracy	**For the Low-Gain or High-Gain Amplifier path**: ±0.2% of amplitude range ±0.05% of offset ±500 µV (within ±10 °C of self-calibration temperature) ±0.4% of amplitude range ±0.05% of offset ±1 mV (0 to 55 °C) **For the Direct path**: Gain accuracy: ±0.2% amplitude range (within ±10 °C of self-calibration temperature) Gain accuracy: ±0.4% amplitude range (0 to 55 °C) DC error: ±30 mV (0 to 55 °C) **Note**: For DC accuracy, "amplitude range" is defined as 2× the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, its DC accuracy is calculated by the following equation: ±0.2%×(16 V) ±0.05%×(1.5 V) ±500 µV = ±33.25 mV	All paths are calibrated for amplitude and gain errors. The Low-Gain and High-Gain Amplifier paths also are calibrated for offset errors.
AC Amplitude Accuracy	(+2.0% + 1 mV), (–1.0% – 1 mV) (+0.8% + 0.5 mV), (–0.2% – 0.5 mV), typical	50 kHz sine wave.
Output Characteristics		
Output Impedance	50 Ω nominal or 75 Ω nominal, software-selectable	—
Load Impedance Compensation	Output amplitude is compensated for user-specified load impedances.	—
Output Coupling	DC	—
Output Enable	Software-selectable. When disabled, CH 0 output is terminated with a 1 W resistor with a value equal to the selected output impedance.	—
Maximum Output Overload	The CH 0 output terminal can be connected to a 50 Ω, ±12 V (±8 V for the Direct path) source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.	—

<table>
<tr><th>Specification</th><th>Value</th><th>Comments</th></tr>
<tr><td colspan="3">Output Characteristics (Continued)</td></tr>
<tr><td>Waveform Summing</td><td>The CH 0 output supports waveform summing among similar paths—specifically, the output terminals of multiple NI 5441 signal generators can be connected together.</td><td>—</td></tr>
<tr><td colspan="3">Frequency and Transient Response</td></tr>
<tr><td>Bandwidth</td><td>43 MHz</td><td>Measured at –3 dB.</td></tr>
<tr><td>DAC Digital Interpolation Filter</td><td>Software-selectable finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.</td><td>The digital filter is not available for use for Sample clock rates below 10 MS/s.

Refer to the DAC Effective Sample Rate section for more information about the effect of DAC interpolation on sample rates.

Refer to the Onboard Signal Processing section for OSP Interpolation.</td></tr>
<tr><td>Analog Filter</td><td>Software-selectable 7-pole elliptical filter for image suppression.</td><td>Available only on Low-Gain amplifier and High-Gain amplifier Paths.</td></tr>
<tr><td rowspan="3">Passband Flatness</td><td colspan="3">Path</td><td rowspan="3">With respect to 50 kHz.</td></tr>
<tr><td>Direct</td><td>Low-Gain Amplifier</td><td>High-Gain Amplifier</td></tr>
<tr><td>–0.4 to +0.6dB
100 Hz to
40 MHz</td><td>–1.0 dB to +0.5
100 Hz to 20 MHz</td><td>–1.2 to +0.5 dB
100 Hz to 20 MHz</td></tr>
</table>

Specification	Value			Comments
Frequency and Transient Response (Continued)				
Pulse Response	Path			Analog filter and DAC Interpolation filter disabled.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
Rise/Fall Time	<5 ns <4.5 ns, typical*	<8 ns <7 ns* <5.5 ns, typical*	<10 ns	
Aberration	<10%, typical	<5%, typical	<5%, typical	

* Specifications apply only to E-revision and later NI PXI-5441 devices (National Instruments part number 191789E-0*x*).

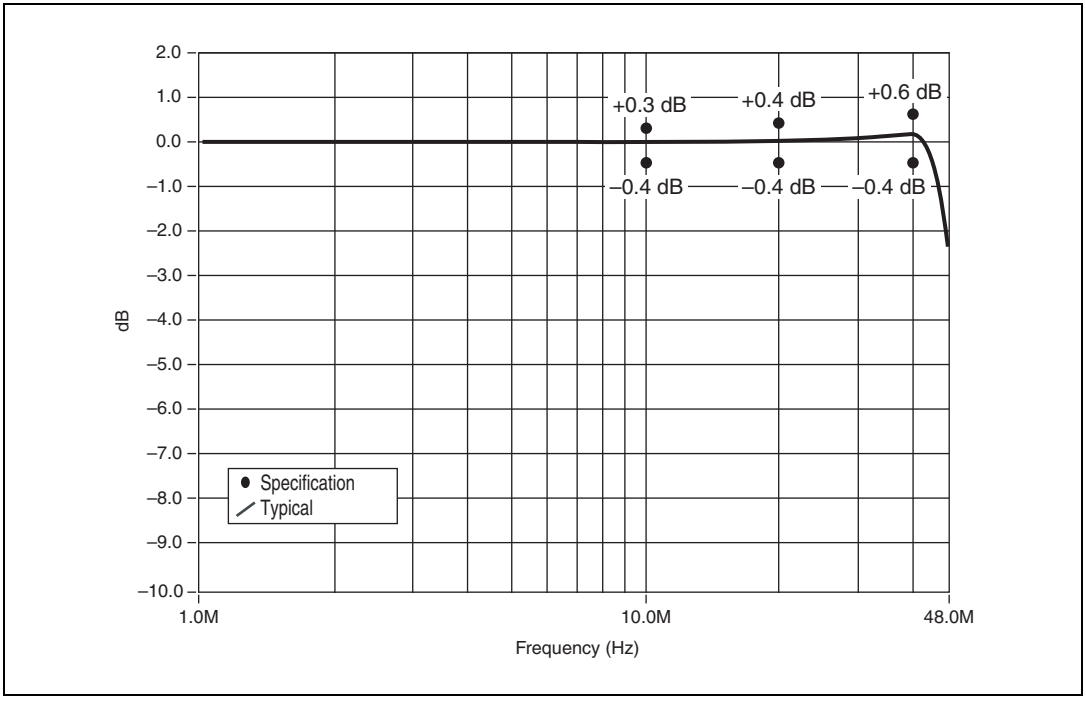

Figure 1. Normalized Passband Flatness, Direct Path

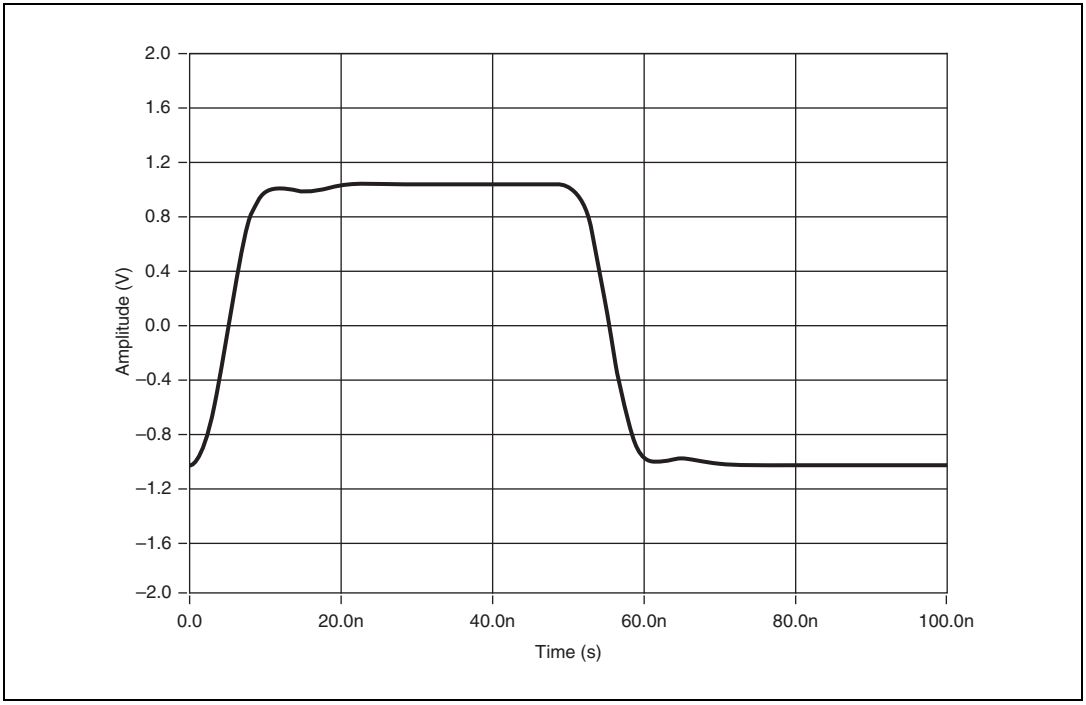

Figure 2. Pulse Response, Low-Gain Amplifier Path 50 Ω Load

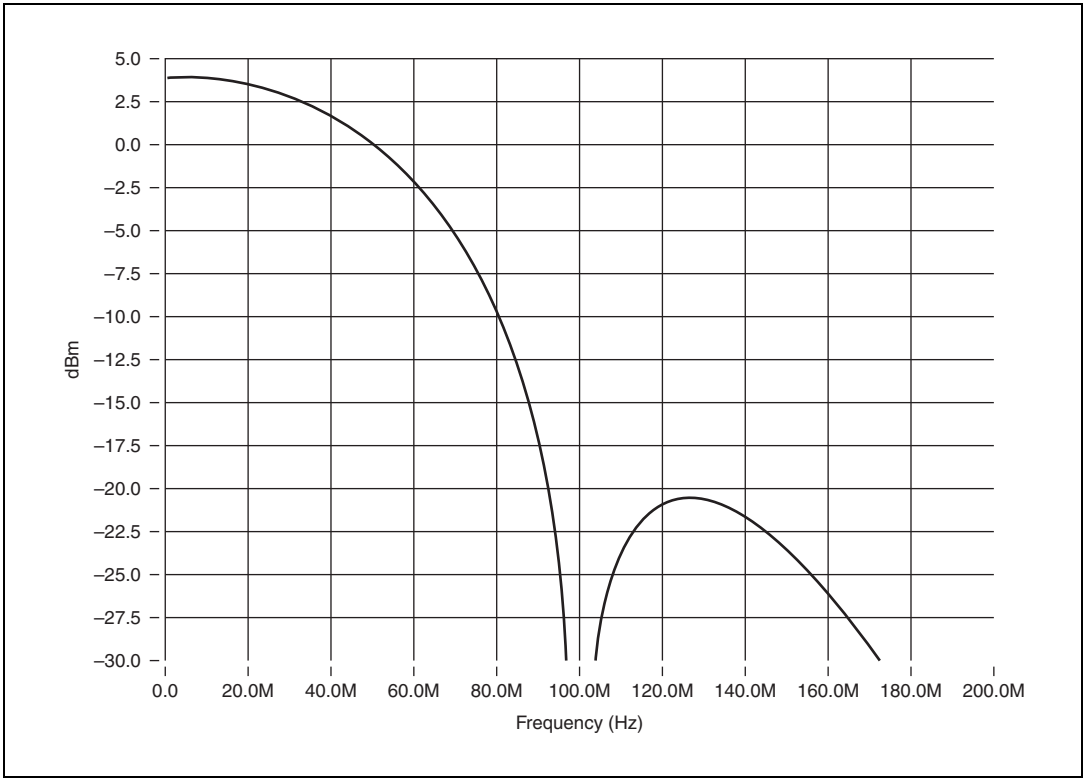

Figure 3. Frequency Response of Direct Path, 100 MS/s, 1x DAC Interpolation

Note Above 50 MHz, the response is the image response.

Specification	Value			Comments
Suggested Maximum Frequencies for Common Functions				
Function	Path			Disable the Analog filter and the DAC Interpolation filter for square, ramp, and triangle. The minimum frequency is 0 Hz.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
Sine	43 MHz	43 MHz	43 MHz	
Square	Not recommended*	25 MHz	12.5 MHz	
Ramp	Not recommended*	5 MHz	5 MHz	
Triangle	Not recommended*	5 MHz	5 MHz	
* Direct path is optimized for the frequency domain.				
Spectral Characteristics				
Signal to Noise and Distortion (SINAD)	Path			Amplitude –1 decibel full scale (dBFS). Measured from DC to 50 MHz. SINAD at low amplitudes is limited by a –148 dBm/Hz noise floor. All values are typical.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	64 dB	66 dB	63 dB	
10 MHz	61 dB	60 dB	47 dB	
20 MHz	57 dB	56 dB	42 dB	
30 MHz	60 dB	62 dB	62 dB	
40 MHz	60 dB	62 dB	62 dB	
43 MHz	58 dB	60 dB	55 dB	

Specification	Value			Comments
Spectral Characteristics (Continued)				
Spurious-Free Dynamic Range (SFDR)[1] with Harmonics	Path			Amplitude –1 dBFS. Measured from DC to 50 MHz. Also called harmonic distortion. SFDR with harmonics at low amplitudes is limited by a –148 dBm/Hz noise floor. All values are typical and include aliased harmonics.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	76 dB	71 dB	58 dB	
10 MHz	68 dB	64 dB	47 dB	
20 MHz	60 dB	57 dB	42 dB	
30 MHz	73 dB	73 dB	74 dB	
40 MHz	76 dB	73 dB	74 dB	
43 MHz	78 dB	75 dB	59 dB	
SFDR without Harmonics	Path			Amplitude –1 dBFS. Measured from DC to 50 MHz. SFDR without harmonics at low amplitudes is limited by a –148 dBm/Hz noise floor. All values are typical and include aliased harmonics.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	87 dB	90 dB	90 dB	
10 MHz	86 dB	88 dB	90 dB	
20 MHz	79dB	88 dB	88 dB	
30 MHz	72 dB	72 dB	73 dB	
40 MHz	75 dB	72 dB	73 dB	
43 MHz	77 dB	74 dB	59 dB	

[1] Dynamic range is defined as the difference between the carrier level and the largest spur.

Specification	Value			Comments
Spectral Characteristics (Continued)				
0 to 40 ºC Total Harmonic Distortion (THD)	Path			Amplitude –1 dBFS. Includes the 2nd through the 6th harmonic.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
20 kHz	–77 dBc, typical	–77 dBc, typical	–77 dBc, typical	
1 MHz	–75 dBc, typical	–70 dBc, typical	–62 dBc, typical	
5 MHz	–68 dBc	–68 dBc	–55 dBc	
10 MHz	–65 dBc –66 dBc, typical*	–61 dBc –66 dBc, typical*	–46 dBc	
20 MHz	–55 dBc –61 dBc, typical*	–53 dBc –61 dBc, typical*	–40 dBc	
30 MHz	–50 dBc –57 dBc, typical*	–48 dBc –57 dBc, typical*	–38 dBc	
40 MHz	–47 dBc –54 dBc, typical*	–46 dBc –54 dBc, typical*	–34 dBc	
43 MHz	–46 dBc –53 dBc, typical*	–45 dBc –53 dBc, typical*	–33 dBc	

* Specifications apply only to E-revision and later NI PXI-5441 devices (National Instruments part number 191789E-0*x*).

Specification	Value			Comments
Spectral Characteristics (Continued)				
0 to 55 ºC THD	Path			Amplitude –1 dBFS. Includes the 2nd through the 6th harmonic.
	Direct	Low-Gain Amplifier	High-Gain Amplifier	
20 kHz	–76 dBc, typical	–76 dBc, typical	–76 dBc, typical	
1 MHz	–74 dBc, typical	–69 dBc, typical	–61 dBc, typical	
5 MHz	–67 dBc	–67 dBc	–54 dBc	
10 MHz	–63 dBc	–60 dBc	–45 dBc	
20 MHz	–54 dBc –57 dBc*	–52 dBc –55 dBc*	–39 dBc	
30 MHz	–48 dBc –52 dBc*	–46 dBc –50 dBc*	–36 dBc	
40 MHz	–45 dBc –50 dBc*	–41 dBc –47 dBc*	–32 dBc	
43 MHz	–44 dBc –49 dBc*	–41 dBc –46 dBc*	–31 dBc	

* Specifications apply only to E-revision and later NI PXI-5441 devices (National Instruments part number 191789E-0*x*).

Specification	Value					Comments
Spectral Characteristics (Continued)						
Average Noise Density		Amplitude Range		Average Noise Density			Average Noise Density at small amplitudes is limited by a –148 dBm/Hz noise floor.
	Path	V_{pk-pk}	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/ Hz	
	Direct	1	4.0	18	–142	–146.0	
	Low Gain	0.06	–20.4	9	–148	–127.6	
	Low Gain	0.1	–16.0	9	–148	–132.0	
	Low Gain	0.4	–4.0	13	–145	–141.0	
	Low Gain	1	4.0	18	–142	–146.0	
	Low Gain	2	10.0	35	–136	–146.0	
	High Gain	4	16.0	71	–130	–146.0	
	High Gain	12	25.6	213	–120	–145.6	

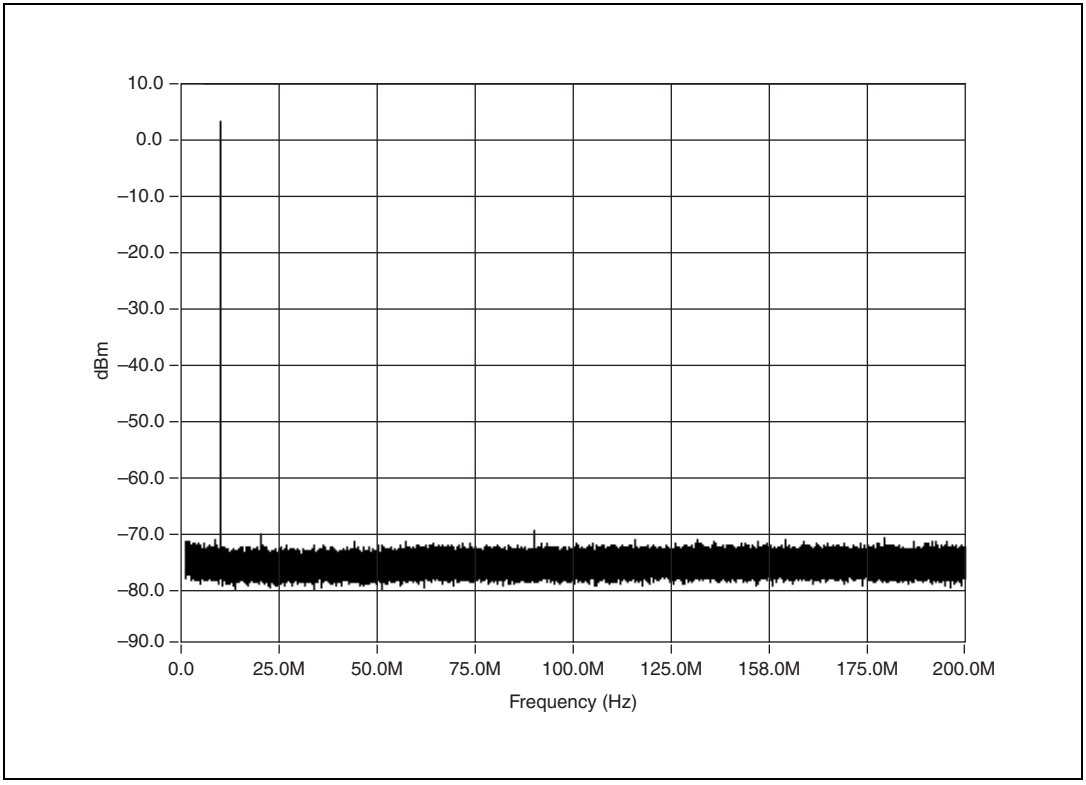

Figure 4. 10 MHz Single-Tone Spectrum, Direct Path, 100 MS/s, DAC Interpolation Factor Set to 4

Note The noise floor in Figure 4 is limited by the measurement device. Refer to the *Average Noise Density* specifications for more information about this limit.

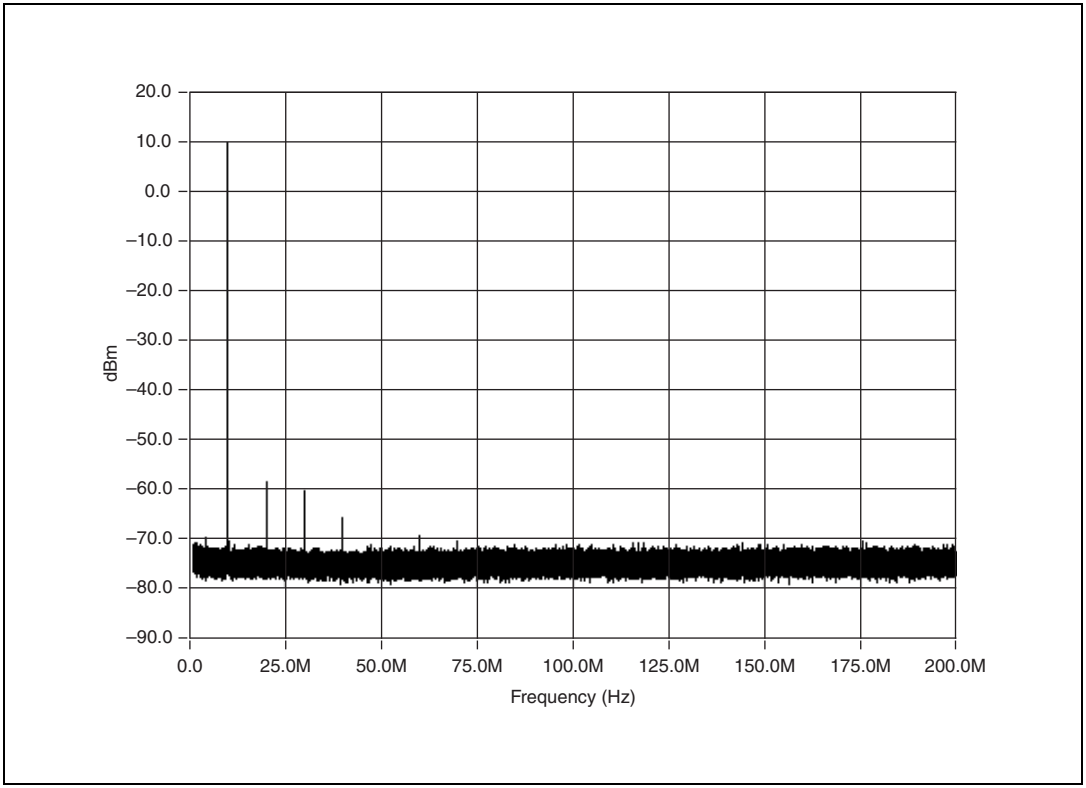

Figure 5. 10 MHz Single-Tone Spectrum, Low-Gain Amplifier Path, 100 MS/s, DAC Interpolation Factor Set to 4

Note The noise floor in Figure 5 is limited by the measurement device. Refer to the *Average Noise Density* specifications for more information about this limit.

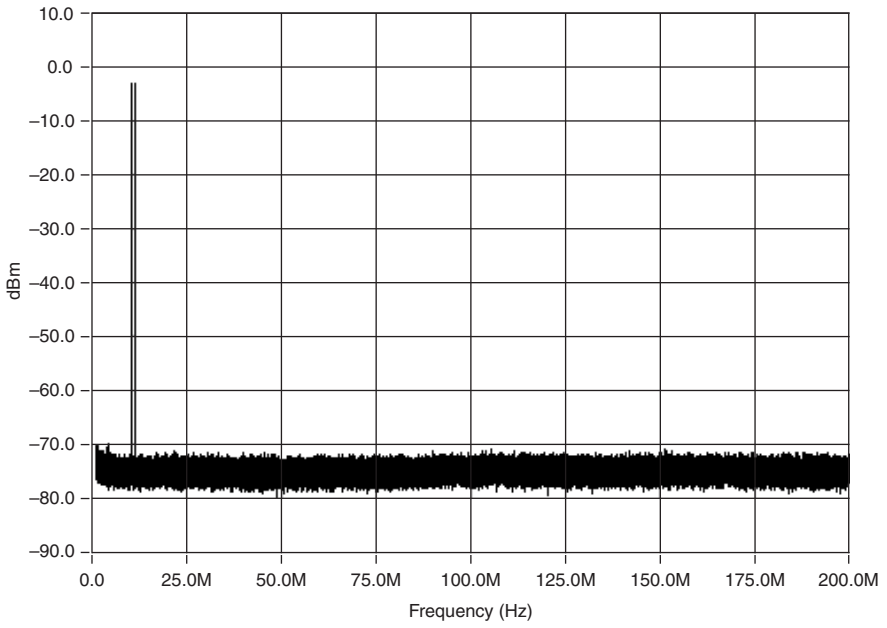

Figure 6. Direct Path, Two-Tone Spectrum (Typical)

Note The noise floor in Figure 6 is limited by the measurement device. Refer to the *Average Noise Density* specifications for more information about this limit.

Sample Clock

Specification	Value	Comments
Sample Clock Sources	1. Internal, Divide-by-*N* (*N* ≥ 1) 2. Internal, DDS-based, high-resolution 3. External, CLK IN (SMB front panel connector) 4. External, DDC CLK IN (DIGITAL DATA & CONTROL front panel connector) 5. External, PXI Star trigger (PXI backplane connector) 6. External, PXI_Trig<0..7> (PXI backplane connector)	Refer to the *Onboard Clock* section for more information about internal clock sources.

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td colspan="5">Sample Rate Range and Resolution</td></tr>
<tr><td>Sample Clock Source</td><td>Sample Rate Range</td><td colspan="2">Sample Rate Resolution</td><td rowspan="6">—</td></tr>
<tr><td>Divide-by-N</td><td>23.84 S/s to 100 MS/s</td><td colspan="2">Settable to (100 MS/s)/N (1 ≤ N ≤ 4,194,304)</td></tr>
<tr><td>High Resolution</td><td>10 S/s to 100 MS/s</td><td colspan="2">1.06 µHz</td></tr>
<tr><td>CLK IN</td><td>200 kS/s to 105 MS/s</td><td colspan="2" rowspan="3">Resolution determined by external clock source.
External sample clock duty cycle tolerance 40 to 60%.</td></tr>
<tr><td>DDC CLK IN</td><td>10 S/s to 105 MS/s</td></tr>
<tr><td>PXI Star Trigger</td><td>10 S/s to 105 MS/s</td></tr>
<tr><td>PXI_Trig<0..7></td><td>10 S/s to 20 MS/s</td><td colspan="2">10 S/s to 20 MS/s</td></tr>
<tr><td colspan="5">DAC Effective Sample Rate</td></tr>
<tr><td rowspan="5"></td><td>Sample Rate (MS/s)</td><td>DAC Interpolation Factor</td><td>Effective Sample Rate</td><td rowspan="5">DAC Effective Sample Rate = (DAC Interpolation factor) × (sample rate)
Refer to the Onboard Signal Processing section for OSP interpolation.</td></tr>
<tr><td>10 S/s to 105 MS/s</td><td>1 (Off)</td><td>10 S/s to 105 MS/s</td></tr>
<tr><td>12.5 MS/s to 105 MS/s</td><td>2</td><td>25 MS/s to 210 MS/s</td></tr>
<tr><td>10 MS/s to 100 MS/s</td><td>4</td><td>40 MS/s to 400 MS/s</td></tr>
<tr><td>10 MS/s to 50 MS/s</td><td>8</td><td>80 MS/s to 400 MS/s</td></tr>
<tr><td colspan="5">Sample Clock Delay Range and Resolution</td></tr>
<tr><td>Sample Clock Source</td><td>Delay Adjustment Range</td><td colspan="2">Delay Adjustment Resolution</td><td rowspan="3">—</td></tr>
<tr><td>Divide-by-N</td><td>±1 Sample clock period</td><td colspan="2"><10 ps</td></tr>
<tr><td>High-Resolution</td><td>±1 Sample clock period</td><td colspan="2">Sample clock period/16,384</td></tr>
<tr><td>External (all)</td><td>0 to 7.6 ns</td><td colspan="2"><15 ps</td></tr>
</table>

Specification	Value				Comments
System Phase Noise and Jitter (10 MHz Carrier)					
Sample Clock Source	System Phase Noise Density (dBc/Hz) Offset			System Output Jitter (Integrated from 100 Hz to 100 kHz)	Specified at 2× DAC oversampling.
	100 Hz	1 kHz	10 kHz		
Divide-by-*N*	–110	–131	–137	<1.0 ps rms	
High-Resolution*	–114	–126	–126	<4.0 ps rms	
CLK IN	–113	–132	–135	<1.1 ps rms	
PXI Star Trigger†	–115	–118	–130	<3.0 ps rms	
* High-Resolution specifications increase as the sample rate is decreased. † PXI star trigger specification is valid when the sample clock source is locked to PXI_CLK10.					
External Sample Clock Input Jitter Tolerance	Cycle-cycle jitter ±300 ps Period Jitter ±1 ns				—
Sample Clock Exporting					
Exported Sample Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. DDC CLK OUT (DIGITAL DATA & CONTROL front panel connector) 3. PXI_Trig<0..6> (PXI backplane connector)				Exported sample clocks can be divided by integer *K* ($1 \le K \le 4{,}194{,}304$).
Exported Sample Clock Destinations	Maximum Frequency	Jitter (Typical)		Duty Cycle	—
PFI<0..1>	105 MHz	PFI 0: 6 ps rms PFI 1: 12 ps rms		25 to 65%	
DDC CLK OUT	105 MHz	40 ps rms		40 to 60%	
PXI_Trig<0..6>	20 MHz	—		—	

Note Sample clock purity can significantly affect the performance of an NI PXI-5441. High amounts of jitter or phase noise in the sample clock can create spurs in the signal generator's spectrum that are not present when using a pure sample clock. For example, if

the Clock Mode property is set to Automatic, NI-FGEN often selects High-Resolution clocking to achieve a specific IQ rate. High-Resolution clocking has more jitter than Divide-By-*N* clocking and may create extra spurs in the signal generator output spectrum (refer to Figures 8 through 15 for examples of this phenomenon). To remove extra spurs without using software resampling, you can use a pure external clock. The NI PXI-5650/5651/5652 frequency source, with low jitter and <1 Hz frequency resolution, is an excellent option.

Onboard Clock
(Internal VCXO)

Specification	Value	Comments
Clock Source	Internal sample clocks can either be locked to a reference clock using a phase-locked loop or be derived from the onboard VCXO frequency reference.	—
Frequency Accuracy	±25 ppm	—

Phase-Locked Loop (PLL) Reference Clock

Specification	Value	Comments
Reference Clock Sources	1. PXI_CLK10 (PXI backplane connector) 2. CLK IN (SMB front panel connector)	The PLL reference clock provides the reference frequency for the PLL.
Frequency Accuracy	When using the PLL, the frequency accuracy of the NI 5441 is solely dependent on the frequency accuracy of the PLL reference clock source.	—
Lock Time	Typical: 70 ms Maximum: 200 ms	—
Frequency Range	5 to 20 MHz in increments of 1 MHz Default of 10 MHz The PLL reference clock frequency must be accurate to ±50 ppm.	—

Specification	Value	Comments
Duty Cycle Range	40 to 60%	—
Exported PLL Reference Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. PXI_Trig<0..6> (PXI backplane connector)	—

CLK IN
(Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Connector	SMB (jack)	—
Direction	Input	—
Destinations	1. Sample clock 2. PLL reference clock	—
Frequency Range	1 to 105 MHz (sample clock destination and sine waves) 200 kHz to 105 MHz (sample clock destination and square waves) 5 to 20 MHz (PLL reference clock destination)	—
Input Voltage Range	Sine wave: 0.65 to 2.8 V_{pk-pk} into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 to 2.8 V_{pk-pk} into 50 Ω	—
Maximum Input Overload	±10 V	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

TClk Specifications

National Instruments TClk synchronization method and the NI-TClk instrument driver are used to align the Sample clocks on any number of SMC-based modules in a chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI Signal Generators Help*.

- Specifications are valid for any number of PXI modules installed in one NI PXI-1042 chassis.
- All parameters set to identical values for each SMC-based module.
- Sample Clock set to 100 MS/s, Divide-by-*N*, and all filters are disabled.
- For other configurations, including multichassis systems, contact NI Technical Support at `ni.com/support`.

Note Although you can use NI-TClk to synchronize nonidentical modules, these specifications apply only to synchronizing identical modules.

Specification	Value	Comments
Intermodule SMC Synchronization Using NI-TClk for Identical Modules (Typical)		
Skew	500 ps	Caused by clock and analog path delay differences. No manual adjustment performed.
Average Skew After Manual Adjustment	<10 ps	For information about manual adjustment, refer to the *Synchronization Repeatability Optimization* topic in the *NI-TClk Synchronization Help*. For additional help with the adjustment process, contact NI Technical Support at `ni.com/support`.
Sample Clock Delay/Adjustment Resolution	≤10 ps	—

PFI 0 and PFI 1
(Programmable Function Interface, Front Panel Connectors)

Specification	Value	Comments
Connectors	Two SMB (jacks)	—
Direction	Bidirectional	—
Frequency Range	DC to 105 MHz	—
As an Input (Trigger)		
Destinations	Start trigger	—
Maximum Input Overload	–2 to +7 V	—
V_{IH}	2.0 V	—
V_{IL}	0.8 V	—
Input Impedance	1 kΩ	—
As an Output (Event)		
Sources	1. Sample clock divided by integer K ($1 \le K \le 4{,}194{,}304$) 2. Sample clock timebase (100 MHz) divided by integer M ($2 \le M \le 4{,}194{,}304$) 3. PLL reference clock 4. Marker 5. Exported start trigger (Out Start trigger)	—
Output Impedance	50 Ω	—
Maximum Output Overload	–2 to +7 V	—
V_{OH}	Minimum: 2.9 V (open load), 1.4 V (50 Ω load)	Output drivers are +3.3 V TTL compatible.
V_{OL}	Maximum: 0.2 V (open load), 0.2 V (50 Ω load)	
Rise/Fall Time	≤2.0 ns	Load of 10 pF.

DIGITAL DATA & CONTROL (DDC)
Optional Front Panel Connector

Specification	Value			Comments
Connector Type	68-pin VHDCI female receptacle			—
Number of Data Output Signals	16			—
Control Signals	1. DDC CLK OUT (clock output) 2. DDC CLK IN (clock input) 3. PFI 2 (input) 4. PFI 3 (input) 5. PFI 4 (output) 6. PFI 5 (output)			—
Ground	23 pins			—
Output Signal Characteristics (Includes Data Outputs, DDC CLK OUT, and PFI<4..5>)				
Signal Type	LVDS (Low-Voltage Differential Signal)			—
Signal Characteristics	Minimum	Typical	Maximum	Tested with 100 Ω differential load. Measured at the device front panel. Load capacitance <15 pF. Driver and receiver comply with ANSI/TIA/EIA-644.
V_{OH}	—	1.3 V	1.7 V	
V_{OL}	0.8 V	1.0 V	—	
Differential Output Voltage	0.25 V	—	0.45 V	
Output Common-Mode Voltage	1.125 V	—	1.375 V	
Differential Pulse Skew (skew within a differential pair)	—	—	0.6 ns	
Rise/Fall Time	—	0.5 ns	1.6 ns	

Specification	Value		Comments
Output Signal Characteristics (Continued)			
Output Skew	Typical: 1 ns; maximum 2 ns. Skew between any two output terminals on the DIGITAL DATA & CONTROL front panel connector.		—
Output Enable/Disable	Controlled through the software on all data output signals and control signals collectively. When disabled, the output terminals go to a high-impedance state.		—
Maximum Output Overload	–0.3 to +3.9 V		—
Input Signal Characteristics (Includes DDC CLK IN and PFI<2..3>)			
Signal Type	LVDS (Low-Voltage Differential Signal)		—
Input Differential Impedance	100 Ω		—
Maximum Output Overload	–0.3 to +3.9 V		—
Signal Characteristics	Minimum	Maximum	—
Differential Input Voltage	0.1 V	0.5 V	
Input Common Mode Voltage	0.2 V	2.2 V	
DDC CLK OUT			
Clocking Format	Data outputs and markers change on the falling edge of DDC CLK OUT.		—
Frequency Range	Refer to the *Sample Clock* section for more information.		—
Duty Cycle	40 to 60%		—
Jitter	40 ps rms		—

Specification	Value	Comments
DDC CLK IN		
Clocking Format	DDC data output signals change on the rising edge of DDC CLK IN.	—
Frequency Range	10 Hz to 105 MHz	—
Input Duty Cycle Tolerance	40 to 60%	—
Input Jitter Tolerances	300 ps pk-pk of cycle-cycle jitter, and 1 ns rms of period jitter.	—

Start Trigger

Specification	Value	Comments
Sources	1. PFI<0..1> (SMB front panel connectors) 2. PFI<2..3> (DIGITAL DATA & CONTROL front panel connector) 3. PXI_Trig<0..7> (backplane connector) 4. PXI Star trigger (backplane connector) 5. Software (use function call) 6. Immediate (does not wait for a trigger). Default.	—
Modes	1. Single 2. Continuous 3. Stepped 4. Burst	—
Edge Detection	Rising	—

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Minimum Pulse Width</td><td colspan="2">25 ns</td><td>Refer to the t_{s1} documentation in the NI Signal Generators Help by navigating to NI Signal Generators Help»Devices» NI 5441» Triggering» Trigger Timing.</td></tr>
<tr><td rowspan="5">Delay from Start Trigger to CH 0 Analog Output with OSP Disabled.</td><td>DAC Interpolation Factor</td><td>Typical Delay</td><td rowspan="5">Refer to the t_{s2} documentation in the NI Signal Generators Help by navigating to NI Signal Generators Help»Devices» NI 5441» Triggering» Trigger Timing.</td></tr>
<tr><td>Digital interpolation filter disabled.</td><td>44 Sample clock periods + 110 ns</td></tr>
<tr><td>2</td><td>58 Sample clock periods + 110 ns</td></tr>
<tr><td>4</td><td>64 Sample clock periods + 110 ns</td></tr>
<tr><td>8</td><td>65 Sample clock periods + 110 ns</td></tr>
<tr><td>Delay from Start Trigger to Digital Data Output with OSP Disabled.</td><td colspan="2">40 Sample clock periods + 110 ns</td><td>—</td></tr>
<tr><td>Additional Delay for Function Generator Mode.</td><td colspan="2">Add 33 Sample clock periods.
(Applicable to delay from Start trigger to CH0 analog output and delay from Start trigger to digital data output)</td><td>—</td></tr>
<tr><td>Additional Delay with OSP Enabled.</td><td colspan="2">Add 70 Sample clock periods for real data processing mode.
Add 73 Sample clock periods for complex data processing mode.
(Applicable to delay from Start trigger to CH0 analog output and delay from Start trigger to digital data output)</td><td>FIR and CIC filters enabled.</td></tr>
</table>

Specification	Value	Comments
Trigger Exporting		
Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the *Destinations* specification in the *Markers* section.	—
Exported Trigger Delay	65 ns (typical)	Refer to the t_{s3} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices» NI 5441» Triggering» Trigger Timing**.
Exported Trigger Pulse Width	>150 ns	Refer to the t_{s4} documentation in the *NI Signal Generators Help* by navigating to **NI Signal Generators Help»Devices» NI 5441» Triggering» Trigger Timing**.

Markers

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Destinations</td><td colspan="3">1. PFI<0..1> (SMB front panel connectors)
2. PFI<4..5> (DIGITAL DATA & CONTROL front panel connector)
3. PXI_Trig<0..6> (backplane connector)</td><td>—</td></tr>
<tr><td>Quantity</td><td colspan="3">One marker per segment</td><td>—</td></tr>
<tr><td>Quantum</td><td colspan="3">Marker position must be placed at an integer multiple of four samples (two samples for Complex (IQ) data).</td><td>—</td></tr>
<tr><td>Width</td><td colspan="3">>150 ns</td><td>Refer to the t_{m2} documentation in the NI Signal Generators Help by navigating to NI Signal Generators Help» Fundamentals» Waveform Fundamentals» Events» Marker Events.</td></tr>
<tr><td rowspan="4">Skew</td><td>Destination</td><td>With Respect to Analog Output</td><td>With Respect to Digital Data Output</td><td rowspan="4">Refer to the t_{m1} documentation in the NI Signal Generators Help by navigating to NI Signal Generators Help» Fundamentals» Waveform Fundamentals» Events» Marker Events.</td></tr>
<tr><td>PFI<0..1></td><td>±2 Sample Clock Periods</td><td>N/A</td></tr>
<tr><td>PFI<4..5></td><td>N/A</td><td><2 ns</td></tr>
<tr><td>PXI_Trig<0..6></td><td>±2 Sample Clock Periods</td><td>N/A</td></tr>
<tr><td>Jitter</td><td colspan="3">20 ps rms</td><td>—</td></tr>
</table>

Arbitrary Waveform Generation Mode

Specification	Value			Comments
Memory Usage	The NI 5441 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.			For more information, refer to the *NI-TClk Synchronization Help* by navigating to **NI Signal Generators Help» Programming» NI-TClk Synchronization Help**.
Onboard Memory Size	32 MB option: 33,554,432 bytes	256 MB option: 268,435,456 bytes	512 MB option: 536,870,912 bytes	—
Output Modes	Arbitrary Waveform mode and Arbitrary Sequence mode			—
Arbitrary Waveform Mode	In Arbitrary Waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.			—
Arbitrary Sequence Mode	In Arbitrary Sequence mode, a sequence directs the NI 5441 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as *segments*. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.			—

Specification	Value			Comments
Minimum Waveform Size (Samples)	Trigger Mode	Arbitrary Waveform Mode	Arbitrary Sequence Mode	The minimum waveform size is sample rate dependent in Arbitrary Sequence mode. For complex (IQ) data minimum waveform size is halved.
	Single	16	16	
	Continuous	16	96 at >50 MS/s	
			32 at ≤50 MS/s	
	Stepped	32	96 at >50 MS/s	
			32 at ≤50 MS/s	
	Burst	16	512 at >50 MS/s	
			256 at ≤50 MS/s	
Loop Count	1 to 16,777,215 Burst trigger: Unlimited			—
Quantum	Waveform size must be an integer multiple of four samples (two samples for complex (IQ) data).			—
Memory Limits				
	32 MB Option	256 MB Option	512 MB Option	All trigger modes except where noted. For complex (IQ) data maximum waveform memory is halved.
Arbitrary Waveform Mode, Maximum Waveform Memory	16,777,088 samples	134,217,600 samples	268,435,328 samples	
Arbitrary Sequence Mode, Maximum Waveform Memory	16,777,008 samples	134,217,520 samples	268,435,200 samples	Condition: One or two segments in a sequence. For complex (IQ) data maximum waveform memory is halved.

Specification	Value			Comments
Memory Limits (Continued)				
Arbitrary Sequence Mode, Maximum Waveforms	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	4,194,000 Burst trigger: 524,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Segments in a Sequence	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	6,708,000 Burst trigger: 4,180,000	Condition: Waveform memory is <4,000 samples. (<2,000 samples for complex (IQ) data.)
Waveform Play Times				
	32 MB	256 MB	512 MB	
Maximum Play Time, Sample Rate = 100 MS/s, OSP Disabled	0.16 seconds	1.34 seconds	2.68 seconds	Single Trigger mode. Play times can be significantly extended by using Continuous, Stepped, or Burst Trigger modes. For Complex (IQ) mode the play times are halved.
Maximum Play Time, IQ Rate = 1 MS/s, Real Mode, OSP Enabled	16 seconds	2 minutes and 14 seconds	4 minutes and 28 seconds	
Maximum Play Time, IQ Rate = 100 kS/s, Real Mode, OSP Enabled	2 minutes and 47 seconds	22 minutes and 22 seconds	44 minutes and 43 seconds	

Function Generation Mode

Specification	Value		Comments
Standard Waveforms and Maximum Frequencies	Waveform	Maximum Frequency	—
	Sine	43 MHz	
	Square	25 MHz	
	Triangle	5 MHz	
	Ramp Up	5 MHz	
	Ramp Down	5 MHz	
	DC	—	
	Noise (Pseudo-Random)	5 MHz	
	User Defined	43 MHz	
Memory Size	65,536 samples for 1/4 symmetric waveforms (Example: Sine) 16, 384 samples for non-1/4 symmetric waveforms (Example: Ramp)		16-bit samples. User Defined Waveforms must be exactly 16,384 samples.
Frequency Resolution	355 nHz		—
Phase Resolution	0.0055°		—

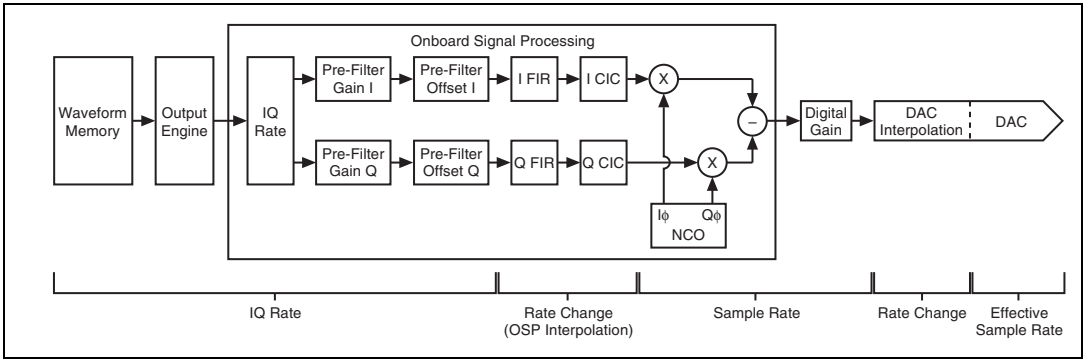

Figure 7. Onboard Signal Processing Block Diagram

Specification	Value	Comments
IQ Rate		
OSP Interpolation Range	12 to 512 (multiples of 2) 512 to 1,024 (multiples of 4) 1,024 to 2,048 (multiples of 8) (OSP Interpolation = FIR Interpolation × CIC Interpolation)	Total NI PXI-5441 Interpolation = OSP Interpolation × DAC Interpolation.
IQ Rate	Sample Rate/OSP Interpolation (Lower IQ Rates are possible by either lowering the sample rate or doing software interpolation)	Example: For a sample rate of 100 MS/s, IQ rate range = 48.8 kS/s to 8.3 MS/s
Data Processing Modes	1. Real (I path only) 2. Complex (IQ)	—

Specification	Value	Comments
Pre-Filter Gain and Offset		
Pre-Filter Gain and Offset Resolution	18 Bits	—
Pre-Filter Gain Range	–2.0 to +2.0 (Values <|1| attenuate User Data)	Unitless
Pre-Filter Offset Range	–1.0 to +1.0	Applied after pre-Filter gain
Output	Output = (User data × pre-Filter gain) + pre-Filter offset (–1 ≤ Output ≤ +1)	Pre-Filter output
FIR (Finite Impulse Response) Filter		
Filter Length	95 Taps	The FIR filter is used to pulse shape the IQ data and to compensate for the CIC filter roll-off.
Coefficient Width	17 bits (–1 to +1)	
Filter Symmetry	Symmetric	
Interpolation Range	2, 4, or 8	
Coefficients	Automatically generated by NI-FGEN (refer to *FIR Filter Types*) or Custom Coefficients provided by the user	

Specification	Value			Comments
FIR Filter Types				
Filter Type	Parameter	Minimum	Maximum	—
Custom	—	—	—	Coefficients are provided by the user.
Flat	Passband	0.1	0.43	Lowpass Filter that minimizes ripple to the following relation: IQ Rate × Passband.
Gaussian	BT	0.1	0.9	—
Raised Cosine	Alpha	0.1	0.9	
Root Raised Cosine	Alpha	0.1	0.9	
CIC (Cascaded Integrator-Comb) Filter				
Size	6 Stages			The CIC Filter does the majority of the interpolation in the OSP.
Interpolation Range	6 ≤ Interpolation ≤ 256 (integers)			
NCO (Numerically Controlled Oscillator)				
Frequency Range	1 mHz to (0.43 × Sample Rate)			—
Frequency Resolution	Sample Rate / 2^{48}			Example: 355 nHz with a Sample Rate of 100 MS/s
I and Q Phase Resolution	0.0055°			—
Phase Quantization	16 bits			Look-up table address width
Tuning Speed	1 ms			—

Specification	Value				Comments
Modulation Performance (Typical)					
Modulation Configuration	Measurement Type	FIR Interpolation			—
		2	4	8	
GSM Physical Layer*	MER (Modulation Error Ratio)	46 dB	47 dB	42 dB	Direct path (4 dBmPeak), 25 MHz carrier
	EVM (Error Vector Magnitude)	<0.5 % rms	<0.5 % rms	<0.8 % rms	
W-CDMA Physical Layer†	MER	46 dB	39 dB	—	Direct path (4 dBmPeak), 25 MHz carrier, ACPR Measurement BW = 4 MHz and Channel Spacing = 5 MHz
	EVM	<7 0.5 % rms	<1.0 % rms	—	
	ACPR (Adjacent Channel Power Ratio) (External Sample Clock)	65 dBc	68 dBc	—	
	ACPR (High-Resolution Sample Clock)	61 dBc	61 dBc	—	
DVB Physical Layer‡	MER	43 dB	—	—	Direct Path (4 dBmPeak), 25 MHz Carrier, ACPR Measurement BW = 7.96 MHz and Channel Spacing = 8 MHz
	EVM	<0.6 % rms	—	—	
	ACPR (External Sample Clock)	48 dBc	—	—	
	ACPR (High-Resolution Sample Clock)	47 dBc	—	—	

* OSP Enabled. IQ Rate = 1.083 MS/s, 4 Samples/Symbol. FIR Filter Type = Flat, Passband = 0.4. MSK modulation: Software Pulse Shaping and Phase Accumulation, 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 14.

† OSP Enabled. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root Raised Cosine, Alpha = 0.22. QPSK. PN Sequence Order = 15.

‡ OSP Enabled. IQ Rate = 6.92 MS/s, 1 Sample/Symbol. FIR Filter Type = Root Raised Cosine, Alpha = 0.15. 32 QAM Modulation. PN Sequence Order = 15.

Specification	Value			Comments
Digital Performance				
Maximum NCO Spur	<–90 dBc			Full-Scale Output
FIR Interpolation	IQ Rate Range (with 100 MS/s Sample Clock Rate)	OSP Out of Band Suppression	OSP Passband Ripple	—
2	195 kS/s to 8.33 MS/s	63 dB	0 to –0.08 dB	FIR Filter Type = Flat. Passband = 0.4. Ripple Measurement to 0.4 × IQ Rate. Stop Band Suppression from 0.6 × IQ Rate.
4	97.6 kS/s to 4.16 MS/s	74 dB	0 to –0.08 dB	
8	48.8 kS/s to 2.08 MS/s	40 dB	0 to –0.8 dB	

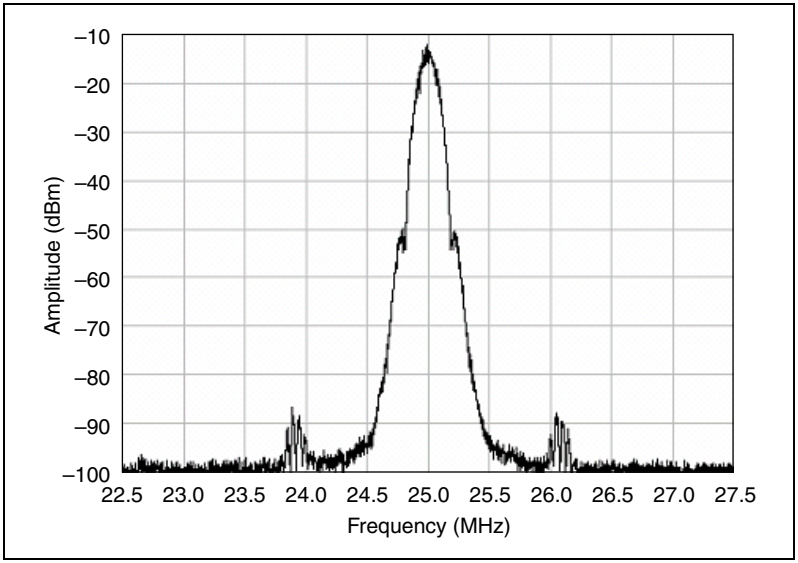

Figure 8. GSM Physical Layer[1,2]
External Sample Clocking = 99.665 MHz

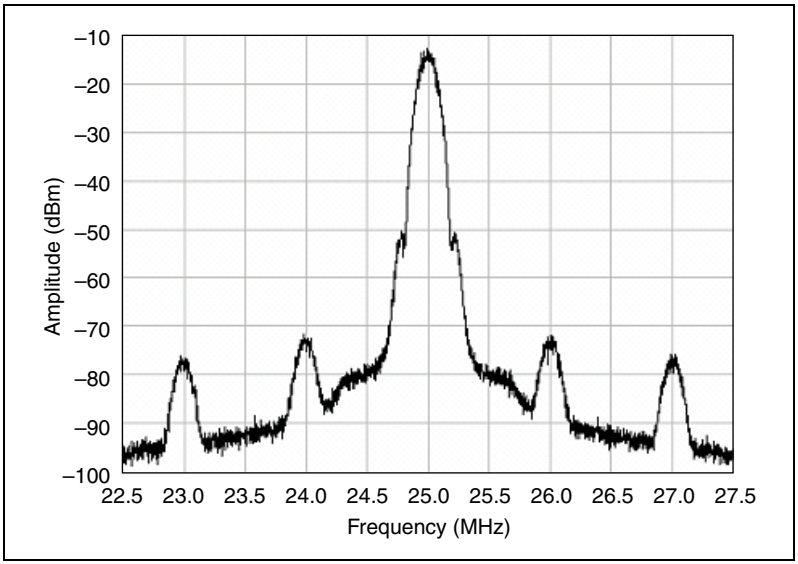

Figure 9. GSM Physical Layer [1,2]
Internal (High Resolution) Sample Clocking = 99.665 MHz
Additional artifacts are caused by High Resolution Clock spurs.

[1] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 1.083 MS/s, 4 Samples/Symbol. FIR Filter Type = Flat, Passband = 0.4. Software MSK modulation: 270.833 kS/s, Gaussian, BT = 0.3. PN Sequence Order = 14.

[2] For more information on eliminating spurs, refer to the *DAC Effective Sample Rate* in the *Sample Clock* section.

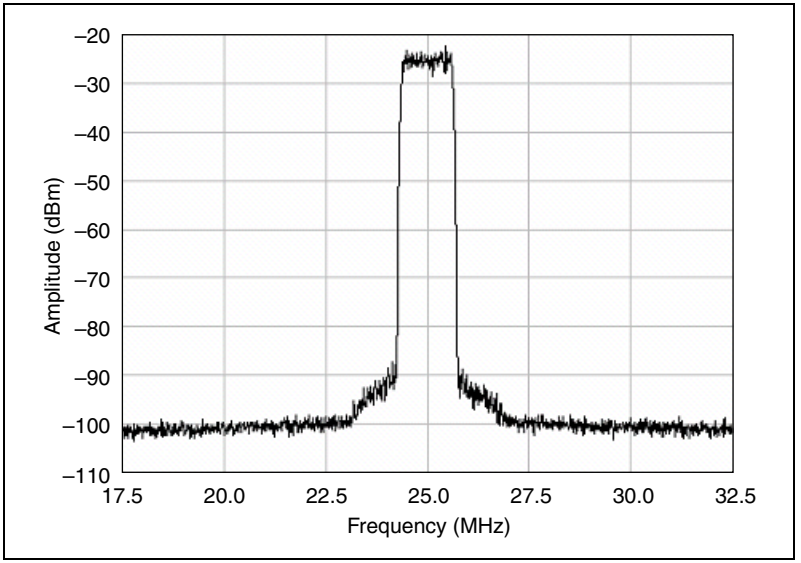

Figure 10. CDMA 2000 Physical Layer[1,2]
External Sample Clocking = 98.304 MHz

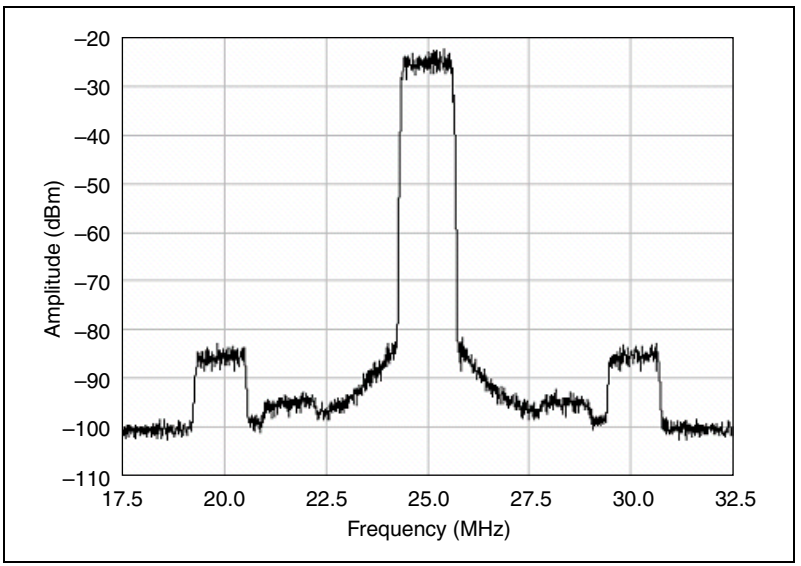

Figure 11. CDMA 2000 Physical Layer[1,2]
Internal (High Resolution) Sample Clocking = 98.304 MHz
Additional artifacts are caused by High Resolution Clock spurs.

[1] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 1.2288 MS/s, 1 Sample/Symbol. FIR Filter Type = Custom Flat Filter with Passband = 0.48. QPSK. PN Sequence Order = 15.

[2] For more information on eliminating spurs, refer to the *DAC Effective Sample Rate* in the *Sample Clock* section.

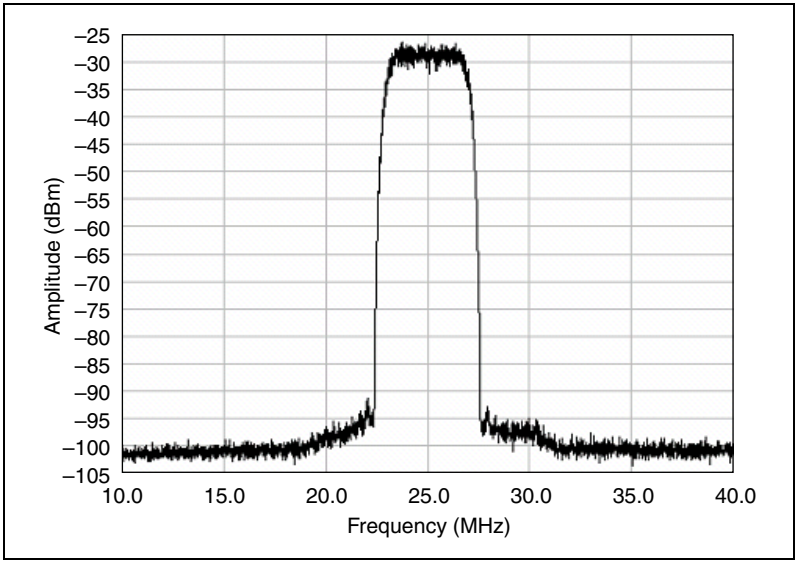

Figure 12. W-CDMA Physical Layer[1,2]
External Sample Clocking = 92.16 MHz

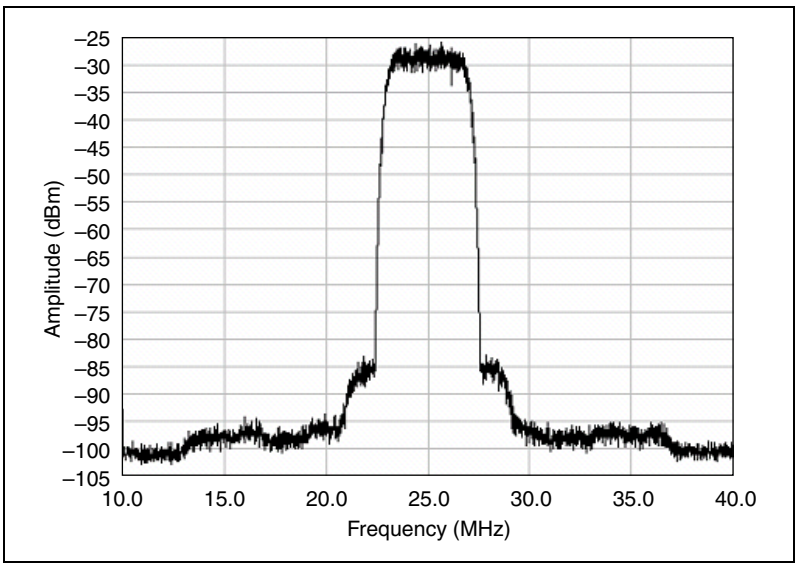

Figure 13. W-CDMA Physical Layer[1,2]
Internal (High Resolution) Sample Clocking = 92.16 MHz
Additional artifacts are caused by High Resolution Clock spurs.

[1] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 3.84 MS/s, 1 Sample/Symbol. FIR Filter Type = Root Raised Cosine, Alpha = 0.22. QPSK. PN Sequence Order = 15.

[2] For more information on eliminating spurs, refer to the *DAC Effective Sample Rate* in the *Sample Clock* section.

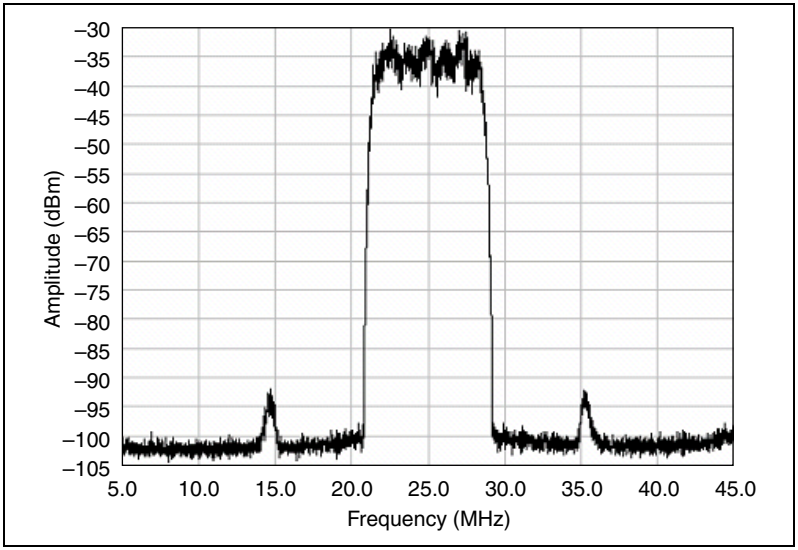

Figure 14. DVB Physical Layer[1,2]
External Sample Clocking = 96.88 MHz
Artifacts at 15 and 35 MHz are due to 2x FIR Interpolation aliasing.

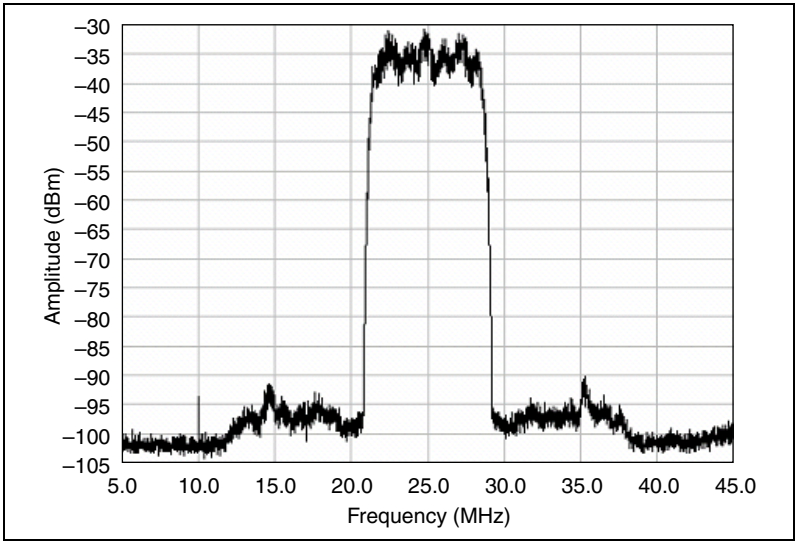

Figure 15. DVB Physical Layer[1,2]
Internal (High Resolution) Sample Clocking = 96.88 MHz
Artifact at 10 MHz is caused by CLK IN feed-through.
Additional artifacts are caused by High Resolution Clock spurs.

[1] OSP Enabled. Direct Path (4 dBm Peak). 25 MHz Carrier. IQ Rate = 6.92 MS/s, 1 Sample/Symbol. FIR Filter Type = Root Raised Cosine, Alpha = 0.15. 32 QAM Modulation. PN Sequence Order = 15.

[2] For more information on eliminating spurs, refer to the *DAC Effective Sample Rate* in the *Sample Clock* section.

Calibration

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.	—
External Calibration	The external calibration calibrates the VCXO, voltage reference, output impedance, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.	Also known as factory calibration.
Calibration Interval	Specifications valid within two years of external calibration.	—
Warm-up Time	15 minutes	—

Power

Specification	Typical Operation	Overload Operation	Comments
+3.3 VDC	1.9 A	2.7 A	Typical. Overload operation occurs when CH 0 is shorted to ground.
+5 VDC	2.2 A	2.4 A	
+12 VDC	0.46 A	0.5 A	
–12 VDC	0.01 A	0.01 A	
Total Power	22.9 W	27.0 W	

Software

Specification	Value	Comments
Driver Software	NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5441. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C++ .NET • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Interactive Control and Configuration Software	The FGEN Soft Front Panel supports interactive control of the NI 5441. The FGEN Soft Front Panel is included on the NI-FGEN driver DVD. Measurement & Automation Explorer (MAX) provides interactive configuration and test tools for the NI 5441. MAX is also included on the NI-FGEN DVD. You can use the NI 5441 with NI SignalExpress.	—

Environment

NI PXI-5441 Environment

Note To ensure that the NI PXI-5441 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5441 kit. The NI PXI-5441 is intended for indoor use only.

Specification	Value	Comments
Operating Temperature	0 to +55 ºC in all NI PXI chassis except the following: 0 to +45 ºC when installed in an NI PXI-101*x* or NI PXI-1000B chassis. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Storage Temperature	–25 to +85 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Operating Relative Humidity	10 to 90%, noncondensing. Meets IEC 60068-2-56.	—
Storage Relative Humidity	5 to 95%, noncondensing. Meets IEC 60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 to 500 Hz, 0.31 g_{rms}. Meets IEC 60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 to 500 Hz, 2.46 g_{rms}. Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 meter maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—

Compliance and Certifications

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations and certifications, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity (DoC) for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Physical

Specification	Value		Comments
Dimensions	3U, One Slot, PXI/cPCI Module 21.6 × 2.0 × 13.0 cm (8.5 × 0.8 × 5.1 in.)		—
Weight	345 g (12.1 oz)		—
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH 0	Analog output	SMB (jack)	
CLK IN	Sample clock input and PLL reference clock input.	SMB (jack)	
PFI 0	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
PFI 1	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
DIGITAL DATA & CONTROL	Digital data output, trigger input, exported trigger output, markers, external sample clock input, and sample clock output.	68-pin VHDCI female receptacle	
Front Panel LED Indicators			
Label	Function		For more information, refer to the *NI Signal Generators Help.*
ACCESS	The ACCESS LED indicates the status of the PCI bus and the interface from the NI 5441 to the controller.		
ACTIVE	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5441.		
Included Cable			
	1 (NI part number 763541-01), 50 Ω, BNC Male to SMB Plug, RG223/U, Double Shielded, 1 m cable.		—

Note NI PXI-5441 modules of revision B or later are equipped with a modified PXI Express-compatible backplane connector. This modified connector allows the NI PXI-5441 to be supported by hybrid slots in a PXI Express chassis. To determine the revision of an NI PXI-5441 module, read the label on the underside of the NI PXI-5441. The label will list an assembly number of the format 191789*x*-01, where *x* is the revision.

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at ni.com/support and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 662 457990-0,
Belgium 32 (0) 2 757 0020, Brazil 55 11 3262 3599,
Canada 800 433 3488, China 86 21 5050 9800,
Czech Republic 420 224 235 774, Denmark 45 45 76 26 00,
Finland 358 (0) 9 725 72511, France 01 57 66 24 24,
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