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PXI-5422

SPECIFICATIONS

PXI-5422

80 MHz Bandwidth, 16-Bit PXI Waveform Generator

These specifications apply to the 8 MB, 32 MB, 256 MB, and 512 MB PXI-5422.

Contents

Conditions

Specifications are valid under the following conditions unless otherwise noted:

- Analog filter enabled
- Signals terminated with 50 Ω
- Direct path set to 1 V pk-pk
- Low-gain amplifier path set to 2 V pk-pk
- High-gain amplifier path set to 12 V pk-pk
- Sample rate set to 200 MS/s
- Sample Clock source set to Divide-by-*N*

Typical specifications are representative of an average unit and valid under the following conditions unless otherwise noted:

- Ambient operating temperature range of 20 ±3 °C

CH 0 Analog Output

Number of channels	1
Connector type	SMB jack

Output Voltage

Full-scale voltage	
Main output path[1]	12.00 V pk-pk to 5.64 mV pk-pk into a 50 Ω load
Direct output path[2]	1.000 V pk-pk to 0.707 V pk-pk
DAC resolution	16 bits

1 When the main output path is selected, either the low-gain amplifier or the high-gain amplifier is used, depending on the value of the **Gain** property or `NIFGEN_ATTR_GAIN` attribute.
2 The direct path is optimized for intermediate frequency (IF) applications.

Amplitude and Offset

Table 1. Amplitude Range[3]

Path	Load	Amplitude (V pk-pk)	
		Minimum	Maximum
Direct	50 Ω	0.707	1.00
	1 kΩ	1.35	1.91
	Open	1.41	2.00
Low-gain amplifier	50 Ω	0.00564	2.00
	1 kΩ	0.0107	3.81
	Open	0.0113	4.00
High-gain amplifier	50 Ω	0.0338	12.0
	1 kΩ	0.0644	22.9
	Open	0.0676	24.0

Amplitude resolution	<0.06% (0.004 dB) of *Amplitude Range*
Offset range[4]	Span of ±50% of *Amplitude Range* with increments <0.0028% of *Amplitude Range*

Maximum Output Voltage

Table 2. Maximum Output Voltage[5]

Path	Load	Maximum Output Voltage (V)
Direct	50 Ω	±0.500
	1 kΩ	±0.953
	Open	±1.000

[3] Amplitude values assume the full scale of the DAC is utilized. If an amplitude smaller than the minimum value is desired, then waveforms less than full scale of the DAC can be used. NI-FGEN compensates for user-specified resistive loads.

[4] Offset range is not available on the direct path.

[5] The combination of amplitude and offset is limited by the maximum output voltage.

Table 2. Maximum Output Voltage[5] (Continued)

Path	Load	Maximum Output Voltage (V)
Low-gain amplifier	50 Ω	±1.000
	1 kΩ	±1.905
	Open	±2.000
High-gain amplifier	50 Ω	±6.000
	1 kΩ	±11.43
	Open	±12.00

Accuracy

Table 3. DC Accuracy[6]

Path	DC Accuracy	
	±10 °C of Self-Calibration Temperature	0 °C to 55 °C
Low-gain amplifier	±0.2% of *Amplitude Range* ± 0.05% of *Offset* ± 500 µV	±0.4% of *Amplitude Range* ± 0.05% of *Offset* ± 1 mV
High-gain amplifier		

5 The combination of amplitude and offset is limited by the maximum output voltage.

6 All paths are calibrated for amplitude and gain errors. The low-gain and high-gain amplifier paths are also calibrated for offset errors. DC accuracy is calibrated into a high-impedance load. *Amplitude Range* is defined as two times the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, DC accuracy is calculated by the following equation: ±0.2% * (16 V) ± 0.05% * (1.5 V) ± 500µV = ±33.25 mV

Table 3. DC Accuracy[6]

Path	Gain Accuracy	
	±10 °C of Self-Calibration Temperature	0 °C to 55 °C
Direct	±0.2% *Amplitude Range*	±0.4% *Amplitude Range*

DC offset error[7]	±30 mV
AC amplitude accuracy[8]	(+2.0% + 1 mV), (-1.0% - 1 mV) (+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical

Output

Output impedance	Software-selectable: 50 Ω or 75 Ω, nominal
Output coupling	DC
Output enable	Software-selectable[9]
Maximum output overload	CH 0 can be connected to a 50 Ω, ±12 V (±8 V for the direct path) source without sustaining any damage.[10]
Waveform summing	Supported[11]

Frequency and Transient Response

Analog filter[12]	Software-selectable: 7-pole elliptical filter for image suppression

6 All paths are calibrated for amplitude and gain errors. The low-gain and high-gain amplifier paths are also calibrated for offset errors. DC accuracy is calibrated into a high-impedance load. *Amplitude Range* is defined as two times the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, DC accuracy is calculated by the following equation: ±0.2% * (16 V) ± 0.05% * (1.5 V) ± 500µV = ±33.25 mV

7 Within 0 °C to 55 °C.

8 With a 50 kHz sine wave and terminated with high impedance.

9 When the output path is disabled, CH 0 is terminated to ground with a 1 W resistor with a value equal to the selected output impedance.

10 No damage occurs if CH 0 is shorted to ground indefinitely.

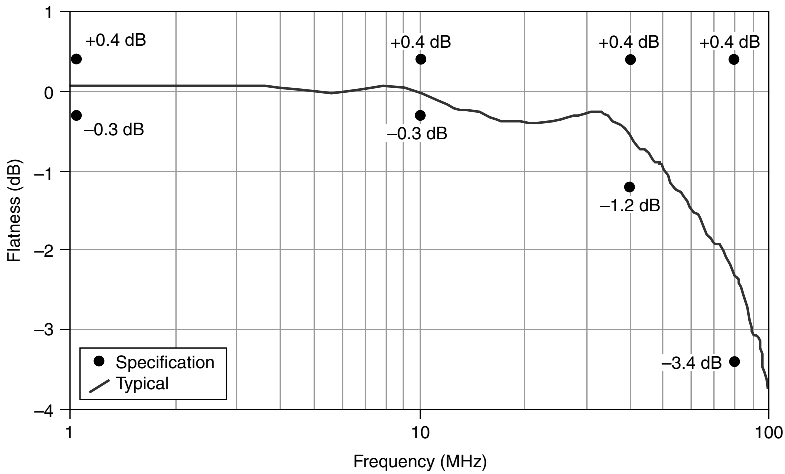
11 The output terminals of multiple PXI-5422 waveform generators can be connected directly together.

12 Available on low-gain amplifier and high-gain amplifier paths.

Table 4. Pulse Response[13]

Path	Rise/Fall Time (ns), Typical	Aberration (%), Typical
Direct	1.0	16
Low-gain amplifier	2.1	6
High-gain amplifier	4.8	8

Figure 1. Normalized Passband Flatness, Direct Path



[13] Analog filter disabled. Measured with a 1 m RG-223 cable.

Figure 2. Normalized Passband Flatness, Low-Gain Amplifier Path

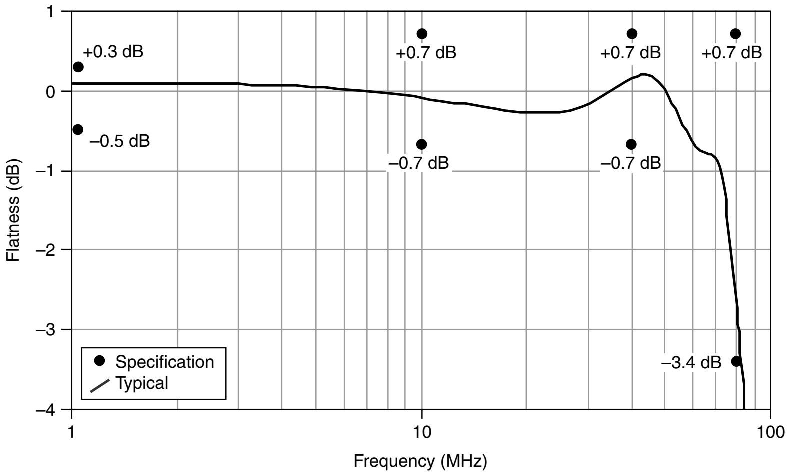


Figure 3. Normalized Passband Flatness, High-Gain Amplifier Path

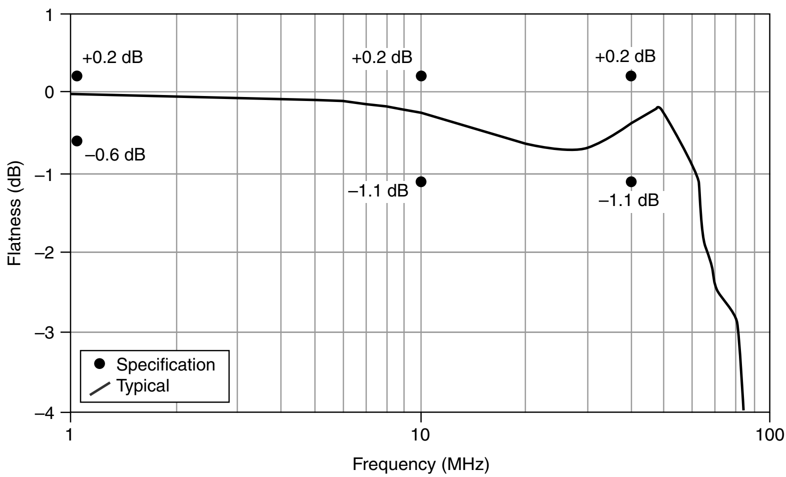
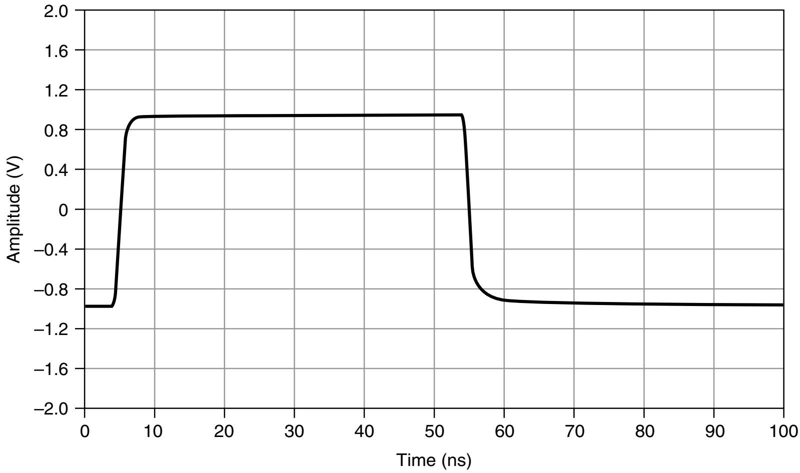


Figure 4. Pulse Response, Low-Gain Amplifier Path with a 50 Ω Load



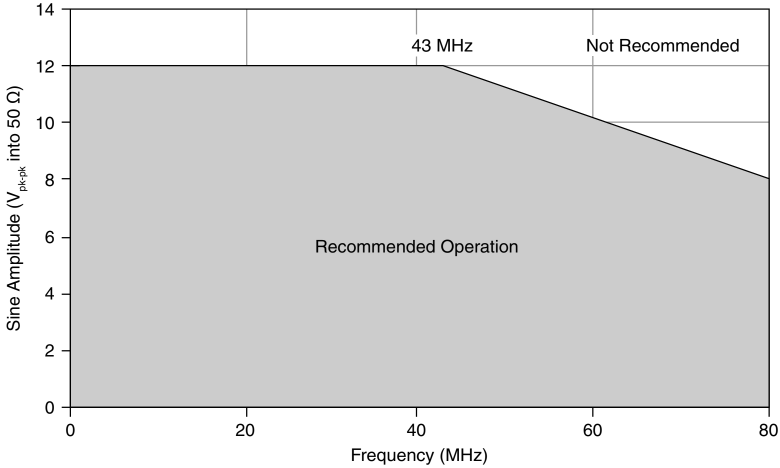
Suggested Maximum Frequencies

Table 5. Suggested Maximum Frequencies for Common Functions[14]

<table>
<tr><th rowspan="2">Path</th><th colspan="4">Frequency (MHz)</th></tr>
<tr><th>Sine</th><th>Square[15]</th><th>Ramp[15]</th><th>Triangle[15]</th></tr>
<tr><td>Direct</td><td rowspan="2">80</td><td colspan="3">Not recommended</td></tr>
<tr><td>Low-gain amplifier</td><td>50</td><td colspan="2" rowspan="2">10</td></tr>
<tr><td>High-gain amplifier</td><td>43</td><td>25</td></tr>
</table>

[14] The minimum frequency is <1 mHz. The value depends on memory size and module configuration.
[15] Disable the analog filter for square, ramp, and triangle functions.

Figure 5. Amplitude Versus Recommended Sine Wave Frequency



Spectral Characteristics

Table 6. Spurious-Free Dynamic Range (SFDR) with Harmonics[16]

Frequency	SFDR with Harmonics (dB), Typical		
	Direct Path	Low-Gain Amplifier Path	High-Gain Amplifier Path
1 MHz	70	65	66
5 MHz			58
10 MHz			52
20 MHz	63	64	49
30 MHz	57	60	43

16 At amplitude of -1 dBFS and measured from DC to 100 MHz. All values include aliased harmonics. Dynamic range is defined as the difference between the carrier level and the largest spur.

Table 6. Spurious-Free Dynamic Range (SFDR) with Harmonics[16] (Continued)

<table>
<tr><th rowspan="2">Frequency</th><th colspan="3">SFDR with Harmonics (dB), Typical</th></tr>
<tr><th>Direct Path</th><th>Low-Gain Amplifier Path</th><th>High-Gain Amplifier Path</th></tr>
<tr><td>40 MHz</td><td rowspan="2">48</td><td rowspan="2">53</td><td>39</td></tr>
<tr><td>50 MHz</td><td rowspan="4">—</td></tr>
<tr><td>60 MHz</td><td rowspan="2">47</td><td rowspan="3">52</td></tr>
<tr><td>70 MHz</td></tr>
<tr><td>80 MHz</td><td>41</td></tr>
</table>

Table 7. Spurious-Free Dynamic Range (SFDR) without Harmonics[16]

<table>
<tr><th rowspan="2">Frequency</th><th colspan="3">SFDR without Harmonics (dB), Typical</th></tr>
<tr><th>Direct Path</th><th>Low-Gain Amplifier Path</th><th>High-Gain Amplifier Path</th></tr>
<tr><td>1 MHz</td><td rowspan="2">84</td><td rowspan="4">79</td><td rowspan="4">76</td></tr>
<tr><td>5 MHz</td></tr>
<tr><td>10 MHz</td><td rowspan="2">79</td></tr>
<tr><td>20 MHz</td></tr>
<tr><td>30 MHz</td><td>72</td><td>70</td><td>67</td></tr>
<tr><td>40 MHz</td><td rowspan="2">47</td><td>57</td><td>54</td></tr>
<tr><td>50 MHz</td><td>52</td><td rowspan="4">—</td></tr>
<tr><td>60 MHz</td><td rowspan="2">46</td><td rowspan="3">51</td></tr>
<tr><td>70 MHz</td></tr>
<tr><td>80 MHz</td><td>40</td></tr>
</table>

16 At amplitude of -1 dBFS and measured from DC to 100 MHz. All values include aliased harmonics. Dynamic range is defined as the difference between the carrier level and the largest spur.

Table 8. Average Noise Density[17], Direct Path

Amplitude Range		Average Noise Density, Typical		
		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	**dBm/Hz**	**dBFS/Hz**
1.00 V pk-pk	4.0 dBm	19.9	-141	-145

Table 9. Average Noise Density[17], Low-Gain Amplifier Path

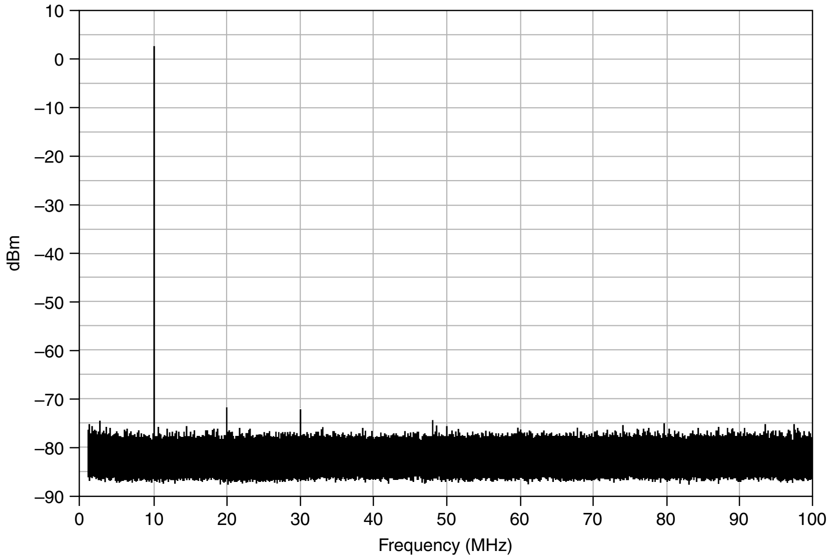
Amplitude Range		Average Noise Density, Typical		
		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	**dBm/Hz**	**dBFS/Hz**
0.06 V pk-pk	-20.5 dBm	1.3	-148	-144
0.10 V pk-pk	-16.0 dBm	2.2		
0.40 V pk-pk	-4.0 dBm	8.9		
1.00 V pk-pk	4.0 dBm	22.3	-140	
2.00 V pk-pk	10.0 dBm	44.6	-134	

Table 10. Average Noise Density[17], High-Gain Amplifier Path

Amplitude Range		Average Noise Density, Typical		
		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	**dBm/Hz**	**dBFS/Hz**
4.00 V pk-pk	16.0 dBm	93.8	-128	-144
12.00 V pk-pk	25.6 dBm	281.5	-118	

[17] Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor.

Figure 6. 10 MHz Single-Tone Spectrum[18], Direct Path, 200 MS/s, Typical



[18] The noise floor in this figure is limited by the measurement device. Refer to *Table 8.* on page 11 for more information about this limit.

Figure 7. 10.00001 MHz Single-Tone Spectrum[18], Low-Gain Amplifier Path, 200 MS/s, Typical

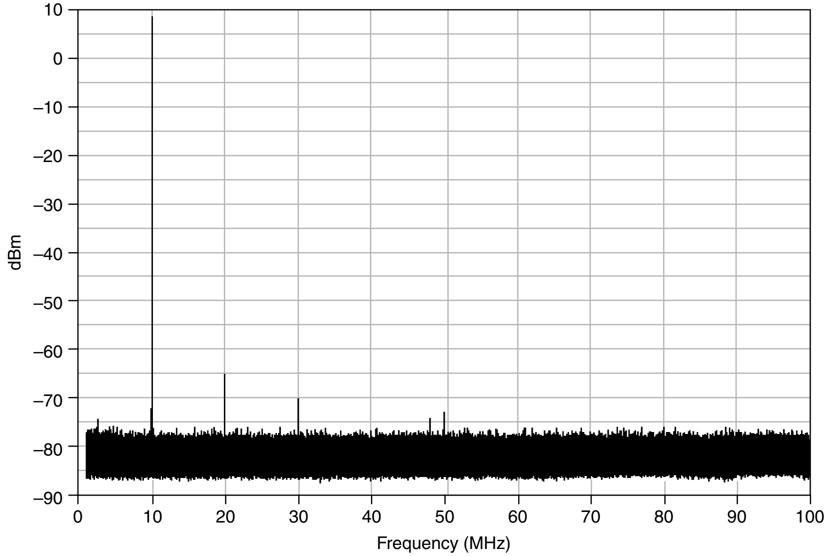


Figure 8. Total Harmonic Distortion, Direct Path, Typical

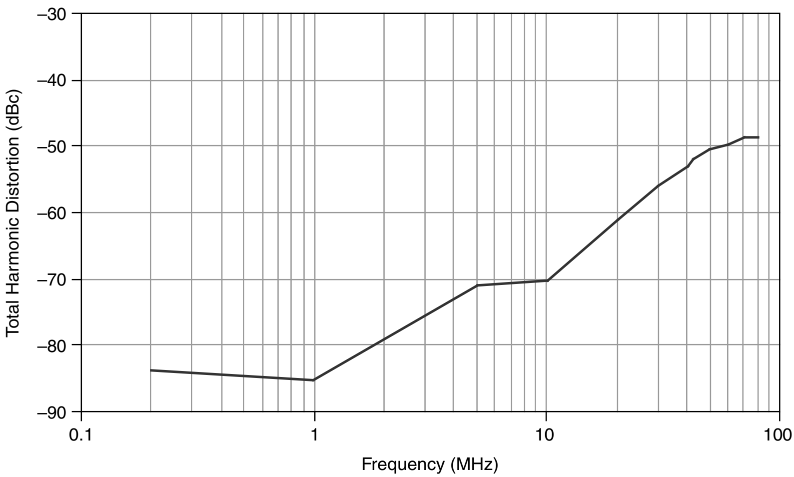


Figure 9. Total Harmonic Distortion, Low-Gain Amplifier Path, Typical

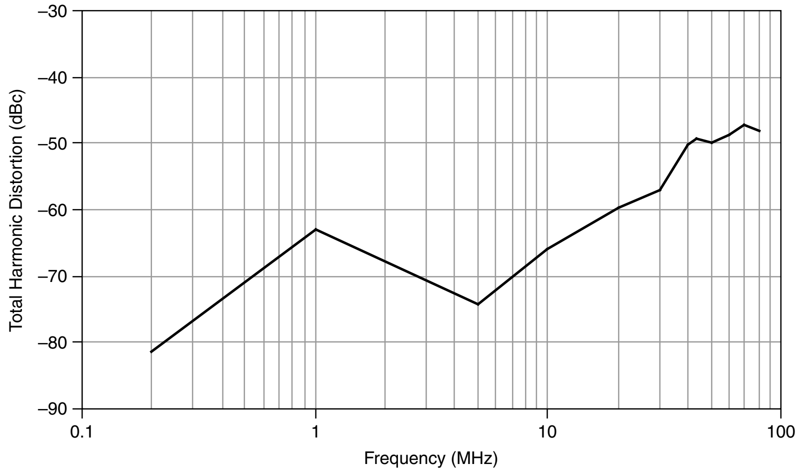


Figure 10. Total Harmonic Distortion, High-Gain Amplifier Path, Typical

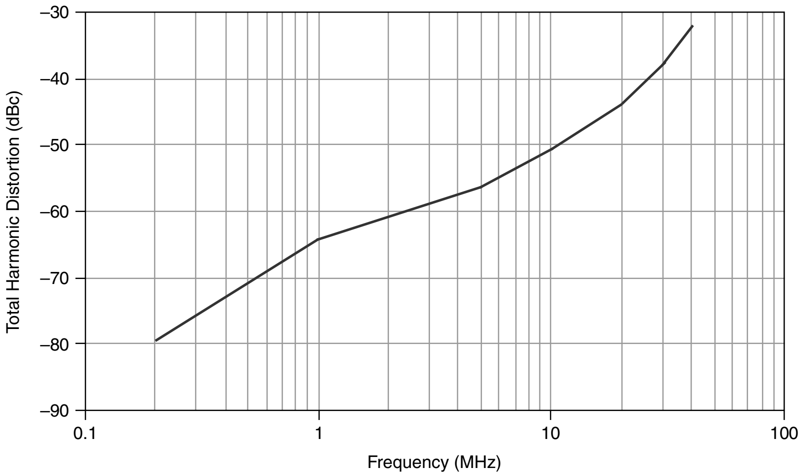


Figure 11. Intermodulation Distortion, 200 kHz Separation, Typical

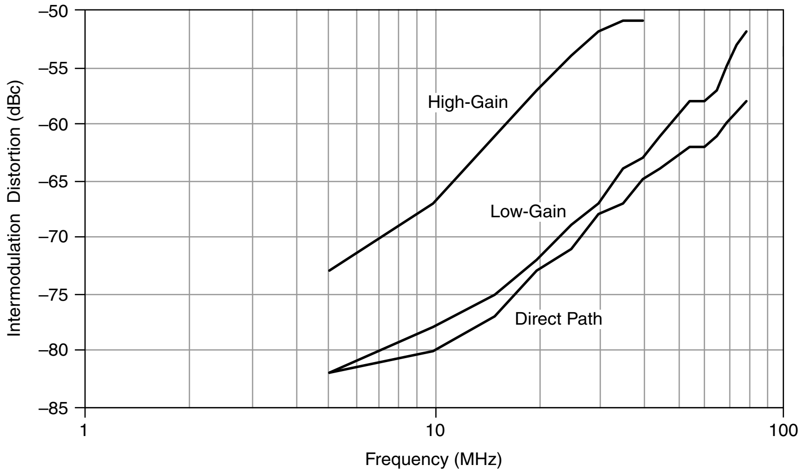
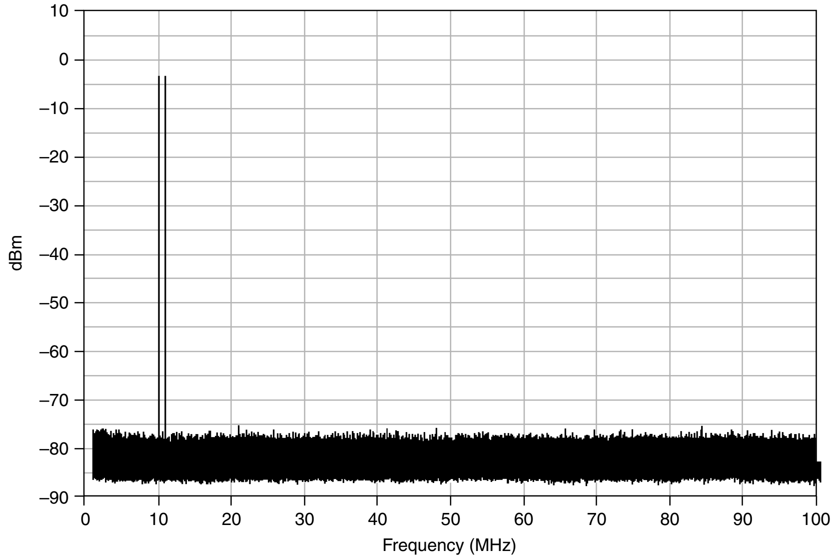


Figure 12. Direct Path, Two-Tone Spectrum[18], Typical



Sample Clock

Sources[19]

Internal	Divide-by-N ($N \geq 1$) DDS-based, High-Resolution
External	CLK IN (SMB front panel connector) DDC CLK IN (DIGITAL DATA & CONTROL front panel connector) PXI Star Trigger (backplane connector) PXI_Trig <0..7> (backplane connector)

Sample Rate Range and Resolution

Table 11. Sample Rate Range

Sample Clock Source	Sample Rate Range (MS/s)
Divide-by-N	5 to 200
High-Resolution	5 to 100
	>100 to 200
CLK IN	5 to 200
DDC CLK IN	
PXI Star Trigger	5 to 105
PXI_Trig <0..7>	5 to 20

Table 12. Sample Rate Resolution

Sample Clock Source	Sample Rate Resolution
Divide-by-N	Configurable to (200 MS/s)/N ($1 \leq N \leq 40$)
High-Resolution	1.06 µHz
	4.24 µHz

[19] Refer to the *Onboard Clock* section for more information about internal clock sources.

Table 12. Sample Rate Resolution (Continued)

Sample Clock Source	Sample Rate Resolution
CLK IN	Resolution determined by external clock source. External Sample Clock duty cycle tolerance 40% to 60%.
DDC CLK IN	
PXI Star Trigger	
PXI_Trig <0..7>	

Sample Clock Delay Range and Resolution

Table 13. Delay Adjustment Range

Sample Clock Source	Delay Adjustment Range
Divide-by-*N*	±1 Sample Clock period
High-Resolution	
CLK IN	0 ns to 7.6 ns
DDC CLK IN	
PXI Star Trigger	
PXI_Trig <0..7>	

Table 14. Delay Adjustment Resolution

Sample Clock Source	Delay Adjustment Resolution
Divide-by-*N*	<5 ps
High-Resolution ≤100 MHz	Sample Clock period/16,384
High-Resolution >100 MHz	Sample Clock period/4,096
CLK IN	<15 ps
DDC CLK IN	
PXI Star Trigger	
PXI_Trig <0..7>	

System Phase Noise and Jitter (10 MHz Carrier)

Table 15. System Phase Noise Density Offset[20]

<table>
<tr><th rowspan="2">Sample Clock Source</th><th colspan="3">System Phase Noise Density Offset (dBc/Hz), Typical</th></tr>
<tr><th>100 Hz</th><th>1 kHz</th><th>10 kHz</th></tr>
<tr><td>Divide-by-N</td><td>-110</td><td>-122</td><td>-138</td></tr>
<tr><td>High-Resolution[21] 100 MS/s</td><td>-109</td><td rowspan="2">-120</td><td>-120</td></tr>
<tr><td>High-Resolution[21] 200 MS/s</td><td>-108</td><td>-122</td></tr>
<tr><td>CLK IN</td><td>-116</td><td>-130</td><td>-143</td></tr>
<tr><td>PXI Star Trigger[22]</td><td>-111</td><td>-128</td><td>-136</td></tr>
</table>

Table 16. System Output Jitter [23]

Sample Clock Source	System Output Jitter (ps rms), Typical
Divide-by-*N*	1.5
High-Resolution[21] 100 MS/s	4.0
High-Resolution[21] 200 MS/s	4.2
CLK IN	1.1
PXI Star Trigger[22]	2.1

External Sample Clock input jitter tolerance

Cycle-cycle jitter	±150 ps, typical
Period jitter	±1 ns, typical

Sample Clock Exporting

Destinations[24]	PFI <0..1> (SMB front panel connectors) DDC CLK OUT (DIGITAL DATA & CONTROL front panel connector) PXI_Trig <0..6> (backplane connector)

20 Specified at two times DAC oversampling.
21 High-Resolution specifications vary with sample rate.
22 PXI Star Trigger specification is valid when the Sample Clock source is locked to PXI_CLK10.
23 Specified at two times DAC oversampling. Integrated from 100 Hz to 100 kHz.
24 Exported Sample Clocks can be divided by integer K ($1 \leq K \leq 4,194,304$).

Maximum frequency	
PFI <0..1>	200 MHz
DDC CLK OUT	200 MHz
PXI_Trig <0..6>	20 MHz
Jitter	
PFI 0	6 ps rms, typical
PFI 1	12 ps rms, typical
DDC CLK OUT	60 ps rms, typical
Duty cycle	
PFI <0..1>	25% to 65%
DDC CLK OUT	35% to 65%

Onboard Clock (Internal VCXO)

Source	Internal Sample Clocks can either be locked to a Reference Clock using a phase-locked loop or derived from the onboard VCXO frequency reference.
Frequency accuracy	±25 ppm

Phase-Locked Loop (PLL) Reference Clock

Sources[25]	PXI_CLK10 (backplane connector) CLK IN (SMB front panel connector)
Frequency accuracy	When using the PLL, the frequency accuracy of the PXI-5422 is solely dependent on the frequency accuracy of the PLL Reference Clock source.
Lock time	≤200 ms, typical
Frequency range[26]	5 MHz to 20 MHz in increments of 1 MHz[27]
Duty cycle range	40% to 60%
Destinations	PFI <0..1> (SMB front panel connectors) PXI_Trig <0..6> (backplane connector)

25 The PLL Reference Clock provides the reference frequency for the PLL.
26 The PLL Reference Clock frequency must be accurate to ±50 ppm.
27 The default is 10 MHz.

CLK IN

Connector type	SMB jack
Direction	Input
Destinations	Sample Clock PLL Reference Clock
Frequency range	
Sample Clock destination	5 MHz to 200 MHz
PLL Reference Clock destination	5 MHz to 20 MHz
Input voltage range into 50 Ω	
Sine wave	0.65 V pk-pk to 2.8 V pk-pk (0 dBm to +13 dBm)
Square wave	0.2 V pk-pk to 2.8 V pk-pk
Maximum input overload	±10 V
Input impedance	50 Ω
Input coupling	AC

PFI 0 and PFI 1

Connector type	SMB jack (x2)
Direction	Bidirectional
Frequency range	DC to 200 MHz
As an input (trigger)	
Destinations	Start Trigger
Maximum input overload	-2 V to +7 V
V IH	2.0 V
V IL	0.8 V
Input impedance	1 kΩ

As an output (event)	
Sources	Sample Clock divided by integer *K* ($1 \leq K \leq 4{,}194{,}304$) Sample Clock Timebase (200 MHz) divided by integer *M* ($4 \leq M \leq 4{,}194{,}304$) PLL Reference Clock Marker Exported Start Trigger (Out Start Trigger)
Output impedance	50 Ω
Maximum output overload	-2 V to +7 V
Minimum V OH[28]	
Open load	2.7 V
50 Ω load	1.3 V
Maximum V OL[28]	
Open load	0.6 V
50 Ω load	0.2 V
Rise/fall time (20% to 80%)[29]	≤2.0 ns

DIGITAL DATA & CONTROL (DDC)

Connector type	68-pin VHDCI female receptacle
Number of data output signals	16
Control signals	DDC CLK OUT (clock output) DDC CLK IN (clock input) PFI 2 (input) PFI 3 (input) PFI 4 (output) PFI 5 (output)
Ground	23 pins

[28] Output drivers are +3.3 V TTL compatible.
[29] Load of 10 pF.

Output Signals (Data Outputs, DDC CLK OUT, and PFI <4..5>)

Low-voltage differential signal (LVDS)[30]	
V OH	1.3 V, typical 1.7 V, maximum
V OL	0.8 V, minimum 1.0 V, typical
Differential output voltage	0.25 V, minimum 0.45 V, maximum
Output common-mode voltage	1.125 V, minimum 1.375 V, maximum
Rise/fall time (20% to 80%)	0.8 ns, typical 1.6 ns, maximum
Output skew[31]	1 ns, typical 2 ns, maximum
Output enable/disable	Controlled through the software on all data output signals and control signals collectively. When disabled, the output signals go to a high-impedance state.
Maximum output overload	-0.3 V to +3.9 V

Input Signals (DDC CLK IN and PFI <2..3>)

Signal type	Low-voltage differential signal (LVDS)
Input differential impedance	100 Ω
Maximum output overload	-0.3 V to +3.9 V
Differential input voltage	0.1 V, minimum 0.5 V, maximum
Input common mode voltage	0.2 V, minimum 2.2 V, maximum

[30] Tested with a 100 Ω differential load, measured with an SHC68-C68-D3 LVDS cable (188143B-01), and driver and receiver comply with ANSI/TIA/EIA-644.

[31] Skew between any two output signals on the DIGITAL DATA & CONTROL (DDC) front panel connector.

DDC CLK OUT

Clocking format	Data outputs and markers change on the falling edge of DDC CLK OUT.
Frequency range	Refer to the *Sample Clock* section for more information.
Duty cycle	35% to 65%
Jitter	60 ps rms, typical

DDC CLK IN

Clocking format	DDC data output signals change on the rising edge of DDC CLK IN.
Frequency range	10 Hz to 200 MHz
Input duty cycle tolerance	40% to 60%

Start Trigger

Sources	PFI <0..1> (SMB front panel connectors) PFI <2..3> (DIGITAL DATA & CONTROL front panel connector) PXI_Trig <0..7> (backplane connector) PXI Star Trigger (backplane connector) Software (use node or function call) Immediate (does not wait for a trigger)[32]
Trigger modes	Single Continuous Stepped Burst
Edge detection	Rising
Minimum pulse width	25 ns
Delay from Start Trigger to CH 0 analog output	65 Sample Clock periods + 110 ns
Delay from Start Trigger to digital data output	41 Sample Clock periods + 110 ns

32 The default is Immediate.

Destinations	A signal used as a trigger can be routed out to any destination listed in the *Destinations* specification of the *Markers* section.
Exported trigger delay	65 ns, typical
Exported trigger pulse width	>150 ns

Related Information

For information about trigger timing, visit ni.com/info and enter the Info Code pxi-5422-trigger-timing.

Markers

Destinations	PFI <0..1> (SMB front panel connectors) PFI <4..5> (DIGITAL DATA & CONTROL front panel connector) PXI_Trig <0..6> (backpane connector)
Quantity	One marker per segment
Quantum	Marker position must be placed at an integer multiple of four samples.
Width	>150 ns
Skew with respect to analog output	
PFI <0..1>	±2 Sample Clock periods
PXI_Trig <0..6>	±2 Sample Clock periods
Skew with respect to digital data output	
PFI <4..5>	<2 ns
Jitter	40 ps rms, typical

Related Information

For information about marker events, visit ni.com/info and enter the Info Code marker-events.

Arbitrary Waveform Generation Mode

Memory usage	The PXI-5422 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters—such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage—are flexible and user-defined.
Onboard memory size	
8 MB standard	8,388,608 bytes
32 MB option	33,554,432 bytes
256 MB option	268,435,456 bytes
512 MB option	536,870,912 bytes
Output modes	Arbitrary waveform[33] Arbitrary sequence[34]

33 In arbitrary waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.

34 In arbitrary sequence mode, a sequence directs the PXI-5422 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as *segments*. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.

Table 17. Minimum Waveform Size

Trigger Mode	Minimum Waveform Size (Samples)		
	Arbitrary Waveform Mode	Arbitrary Sequence Mode[35]	
		At >50 MS/s	At ≤50 MS/s
Single	16		
Continuous	32	192	96
Stepped			
Burst			

Loop count	1 to 16,777,215 Burst trigger: Unlimited
Quantum	Waveform size must be an integer multiple of four samples.

Memory Limits[36]

Table 18. Maximum Waveform Memory

Onboard Memory	Maximum Waveform Memory (Samples)	
	Arbitrary Waveform Mode	Arbitrary Sequence Mode[37]
8 MB standard	4,194,176	4,194,048
32 MB option	16,777,088	16,776,960
256 MB option	134,217,600	134,217,472
512 MB option	268,435,328	268,435,200

Table 19. Maximum Waveforms in Arbitrary Sequence Mode[37]

Onboard Memory	Maximum Waveforms
8 MB standard	65,000
	Burst trigger: 8,000

[35] The minimum waveform size is sample rate dependent in arbitrary sequence mode.
[36] All trigger modes except where noted.
[37] One or two segments in a sequence.

Table 19. Maximum Waveforms in Arbitrary Sequence Mode[37] (Continued)

Onboard Memory	Maximum Waveforms
32 MB option	262,000
	Burst trigger: 32,000
256 MB option	2,097,000
	Burst trigger: 262,000
512 MB option	4,194,000
	Burst trigger: 524,000

Table 20. Maximum Segments in a Sequence in Arbitrary Sequence Mode[38]

Onboard Memory	Maximum Segments in a Sequence
8 MB standard	104,000
	Burst trigger: 65,000
32 MB option	418,000
	Burst trigger: 262,000
256 MB option	3,354,000
	Burst trigger: 2,090,000
512 MB option	6,708,000
	Burst trigger: 4,180,000

[38] Waveform memory is <4,000 samples.

Calibration

Self-calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 90 seconds to complete.
External calibration	External calibration calibrates the VCXO, voltage reference, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.
Calibration interval	Specifications valid within two years of external calibration.
Warm-up time	15 minutes

Power

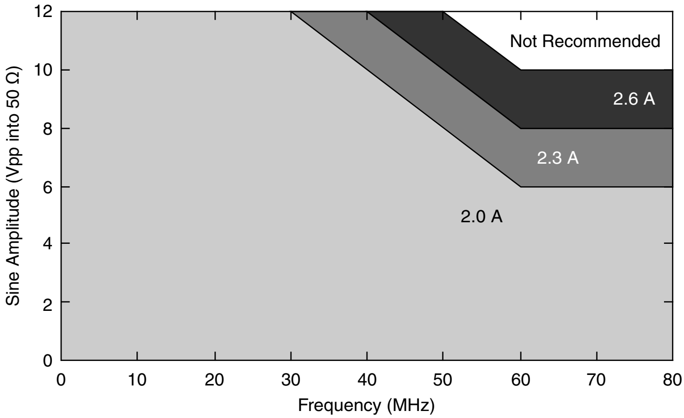
Table 21. Power

	Power	
	Typical Operation[39]	Overload Operation[40]
+3.3 V DC	2 A	
+5 V DC	Refer to *Figure 13.* on page 29.	2.7 A
+12 V DC	0.46 A	
-12 V DC	0.01 A	
Total	12.2 W + 5 V × 5 V current	25.7 W

39 Typical operation includes the following conditions:
- Sine output
- Analog filter enabled
- 50 Ω termination
- 200 MS/s High-Resolution Sample Clock
- Digital pattern enabled and terminated
- Sample Clock routed to PFI 0 and terminated

40 Occurs when CH 0 is shorted to ground.

Figure 13. 5 V Current Versus Frequency and Amplitude



Physical

Dimensions	3U, one-slot, PXI/cPCI module[41] 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)
Weight	352 g (12.4 oz)

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

[41] PXI-5422 modules of revision B or later are equipped with a modified PXI Express-compatible backplane connector. This modified connector allows the PXI-5422 to be supported by hybrid slots in a PXI Express chassis. To determine the revision of a PXI-5422, read the label on the underside of the PXI-5422 module. The label will list an assembly number of the format 191946*x*-01, where *x* is the revision.

Operating Environment

Ambient temperature range	0 °C to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) 0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) when installed in a PXI-101*x* or PXI-1000B chassis
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-25 °C to 85 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Shock	
Operating[42]	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Storage	50 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random vibration	
Operating[42]	5 Hz to 500 Hz, 0.31 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.46 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

[42] Spectral and jitter specifications could degrade.

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Product Certifications and Declarations* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit *ni.com/*

certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

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