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NI PXI/PCI-5412 Specifications

14-Bit 100 MS/s Arbitrary Waveform Generator

このドキュメントには、日本語ページも含まれています。

This document lists specifications for the NI PXI/PCI-5412 arbitrary waveform generator. Unless otherwise noted, the following conditions were used for each specification:

- Interpolation set to maximum allowed factor for a given sample rate.
- Signals terminated with 50 Ω.
- Low-gain amplifier path set to 2 Vpk-pk, and high-gain amplifier path set to 12 Vpk-pk.
- Sample clock set to 100 megasamples per second (MS/s).

Specifications describe the warranted, traceable product performance over ambient temperature ranges of 0 °C to 55 °C, unless otherwise noted.

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under specifications or typical values. Nominal values are not covered by warranty.

Specifications are subject to change without notice. For the most recent NI 5412 specifications, visit `ni.com/manuals`.

To access all the NI 5412 documentation, navigate to **Start»All Programs»National Instruments»NI-FGEN»Documentation**.

Caution The protection provided by this product may be impaired if it used in a manner not specified in this document.

Hot Surface If the NI 5412 has been in use, it may exceed safe handling temperatures and cause burns. Allow the NI 5412 to cool before removing it from the chassis.

NATIONAL INSTRUMENTS

Contents

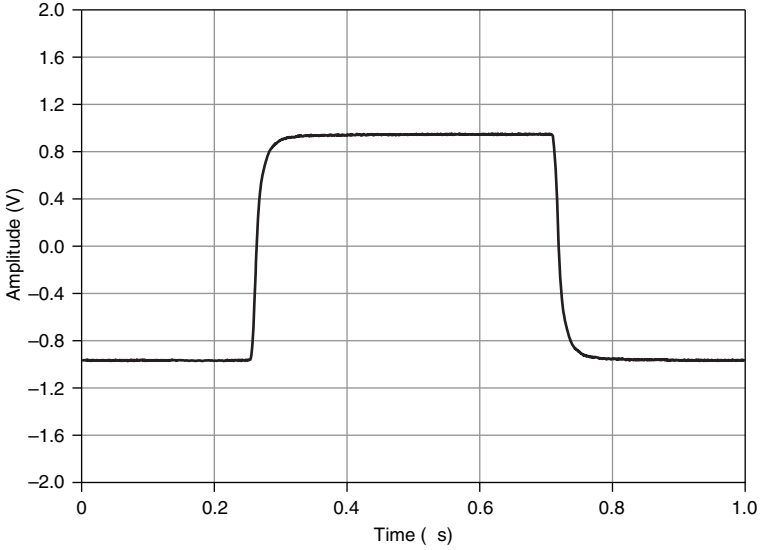
CH 0
(Channel 0 Analog Output, Front Panel Connector)

Specification	Value				Comments
Number of Channels	1				—
Connector	SMB (jack)				—
Output Voltage Characteristics					
Output Paths	The software-selectable main output path setting provides full-scale voltages from 12.00 Vpk-pk to 5.64 mVpk-pk into a 50 Ω load. NI-FGEN uses either the low-gain amplifier or the high-gain amplifier when the main output path is selected, depending on the value of the Gain property or `NIFGEN_ATTR_GAIN` attribute.				—
DAC Resolution	14 bits				—
Amplitude and Offset					
Amplitude Range	Path	Load	Amplitude (Vpk-pk)		Amplitude values assume the full scale of the DAC is utilized. Create amplitudes smaller than the minimum value by using less than the full scale of the DAC. NI-FGEN compensates for user-specified resistive loads.
			Minimum Value	Maximum Value	
	Low-Gain Amplifier	50 Ω	0.00564	2.00	
		1 kΩ	0.0107	3.81	
		Open	0.0113	4.00	
	High-Gain Amplifier	50 Ω	0.0338	12.0	
		1 kΩ	0.0644	22.9	
		Open	0.0676	24.0	
Amplitude Resolution	<0.06% (0.004 dB) of amplitude range				—
Offset Range	Span of ±25% of amplitude range with increments <0.0014% of amplitude range.				—

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td colspan="5">Maximum Output Voltage</td></tr>
<tr><td rowspan="7">Maximum Output Voltage</td><td>Path</td><td>Load</td><td>Maximum Output Voltage (V_{pk})</td><td rowspan="7">The maximum output voltage of the NI 5412 is determined by the amplitude range and the offset range.</td></tr>
<tr><td rowspan="3">Low-Gain Amplifier</td><td>50 Ω</td><td>±1.000</td></tr>
<tr><td>1 kΩ</td><td>±1.905</td></tr>
<tr><td>Open</td><td>±2.000</td></tr>
<tr><td rowspan="3">High-Gain Amplifier</td><td>50 Ω</td><td>±6.000</td></tr>
<tr><td>1 kΩ</td><td>±11.43</td></tr>
<tr><td>Open</td><td>±12.00</td></tr>
<tr><td colspan="5">Accuracy</td></tr>
<tr><td>DC Accuracy</td><td colspan="3">±0.2% of amplitude range ± 0.05% of offset ± 500 µV (within ±10 °C of self-calibration temperature)
±0.4% of amplitude range ± 0.05% of offset ± 1 mV (0 °C to 55 °C)
Note: For DC accuracy, amplitude range is defined as 2× the gain setting. For example, a DC signal with a gain of 8 has an amplitude range of 16 V. If this signal has an offset of 1.5, its DC accuracy is calculated by the following equation:
±0.2% × (16 V) ± 0.05% × (1.5 V) ± 500 µV = ±33.25 mV</td><td>Calibrated for high-impedance load.</td></tr>
<tr><td>AC Amplitude Accuracy</td><td colspan="3">(+2.0% + 1 mV), (-1.0% - 1 mV)
(+0.8% + 0.5 mV), (-0.2% - 0.5 mV), typical</td><td>50 kHz sine wave. Signals terminated with high impedance.</td></tr>
<tr><td colspan="5">Output Characteristics</td></tr>
<tr><td>Output Impedance</td><td colspan="3">50 Ω or 75 Ω nominal, software-selectable.</td><td>—</td></tr>
<tr><td>Output Coupling</td><td colspan="3">DC</td><td>—</td></tr>
</table>

Specification	Value		Comments
Output Enable	Software-selectable. When the output path is disabled, the CH 0 output is terminated to ground with a 1 W resistor equal to the selected output impedance.		—
Maximum Output Overload	The CH 0 output can be connected to a 50 Ω, ±12 V source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.		—
Waveform Summing	The CH 0 output supports waveform summing among similar paths—specifically, the output terminals of multiple NI 5412 signal generators can be connected directly together.		—
Frequency and Transient Response			
Bandwidth	20 MHz		-3 dB
Digital Interpolation Filter	Software-selectable finite impulse response (FIR) filter. Available interpolation factors are 2, 4, or 8.		The digital filter is not available for use for Sample clock rates below 10 MS/s. Refer to the *Effective Sample Rate* section of the *Sample Clock* section for more information about the effect of interpolation on sample rates.
Passband Flatness	Low-Gain and High-Gain Amplifier Paths		With respect to 50 kHz.
	±1.0 dB from DC to 6 MHz		
Pulse Response	Path		All values are typical. Measured with a 1 m RG-223 cable.
	Low-Gain Amplifier	High-Gain Amplifier	
Rise/Fall Time	<20 ns	<20 ns	
Aberration	<5%	<5%	

Figure 1. Pulse Response, Low-Gain Amplifier Path 50 Ω Load



Specification	Value		Comments
Suggested Maximum Frequencies for Common Functions			
Function	Path		The minimum frequency is <1 mHz. The value depends on memory size and device configuration.
	Low-Gain Amplifier	High-Gain Amplifier	
Sine	20 MHz	20 MHz	
Square	5 MHz	5 MHz	
Ramp	1 MHz	1 MHz	
Triangle	1 MHz	1 MHz	
Spectral Characteristics			
Spurious-Free Dynamic Range (SFDR)* without Harmonics	Path		Amplitude -1 decibel full scale (dBFS). Measured from DC to 50 MHz. All values are typical.
	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	70 dB	70 dB	
10 MHz	65 dB	65 dB	
20 MHz	60 dB	60 dB	
Total Harmonic Distortion (THD), 0 ºC to 40 ºC	Path		Amplitude -1 dBFS. Includes the 2nd through the 6th harmonic. All values are typical.
	Low-Gain Amplifier	High-Gain Amplifier	
1 MHz	-59 dBc	-51 dBc	
10 MHz	-52 dBc	-40 dBc	
20 MHz	-45 dBc	-37 dBc	

* Dynamic range is defined as the difference between the carrier level and the largest spur.

Specification	Value					Comments
Spectral Characteristics (Continued)						
Average Noise Density	Path	Amplitude Range		Average Noise Density		Average noise density at small amplitudes is limited by a -148 dBm/Hz noise floor. All values are typical.
		Vpk-pk	dBm	$\frac{nV}{\sqrt{Hz}}$	dBm/Hz	dBFS/Hz
	Low-Gain	2	10	45	-134	-144
	High-Gain	12	25.6	251	-119	-145

Sample Clock

Specification	Value	Comments
Sample Clock Sources	1. Internal, Divide-by-N ($N \geq 1$) 2. Internal, DDS-based, High-Resolution 3. External, CLK IN (SMB front panel connector) 4. **NI PXI-5412**: External, PXI star trigger (PXI backplane connector) 5. **NI PXI-5412**: External, PXI_Trig<0..7> (PXI backplane connector) **NI PCI-5412**: External, RTSI<0..7>	Refer to the *Onboard Clock* section for more information about internal clock sources.

Specification	Value			Comments
Sample Rate Range and Resolution				
Sample Clock Source	Sample Rate Range		Sample Rate Resolution	—
Divide-by-*N*	23.84 S/s to 100 MS/s		Settable to (100 MS/s)/*N* ($1 \leq N \leq 4{,}194{,}304$)	
High-Resolution	10 S/s to 100 MS/s		1.06 µHz	
CLK IN	200 kS/s to 105 MS/s		Resolution determined by external clock source. External Sample clock duty cycle tolerance 40% to 60%.	
NI PXI-5412 PXI Star Trigger	10 S/s to 105 MS/s			
NI PXI-5412 PXI_Trig<0..7>	10 S/s to 20 MS/s			
NI PCI-5412 RTSI<0..7>	10 S/s to 20 MS/s			
Effective Sample Rate				
	Sample Rate (MS/s)	Interpolation Factor	Effective Sample Rate	Effective Sample Rate = (*Interpolation Factor*) × (*Sample Rate*)
	10 S/s to 105 MS/s	1 (Off)	10 S/s to 105 MS/s	
	12.5 MS/s to 105 MS/s	2	25 MS/s to 210 MS/s	
	10 MS/s to 100 MS/s	4	40 MS/s to 400 MS/s	
	10 MS/s to 50 MS/s	8	80 MS/s to 400 MS/s	
Sample Clock Delay Range and Resolution				
Sample Clock Source	Delay Adjustment Range		Delay Adjustment Resolution	—
Divide-by-*N*	±1 Sample clock period		<10 ps	
High-Resolution	±1 Sample clock period		Sample clock period/16,384	

<table>
<tr><th>Specification</th><th colspan="4">Value</th><th>Comments</th></tr>
<tr><td colspan="6">System Phase Noise and Jitter (10 MHz Carrier)</td></tr>
<tr><td rowspan="2">Device (Sample Clock Source)</td><td colspan="3">System Phase Noise Density (dBc/Hz) Offset</td><td rowspan="2">System Output Jitter (Integrated from 100 Hz to 100 kHz)</td><td rowspan="3">Specified at 2 × DAC oversampling. High-resolution specifications vary with sample rate. All values are typical.</td></tr>
<tr><td>100 Hz</td><td>1 kHz</td><td>10 kHz</td></tr>
<tr><td>NI PXI-5412</td><td>-100</td><td>-118</td><td>-120</td><td><6 ps rms</td></tr>
<tr><td>NI PCI-5412</td><td>-90</td><td>-110</td><td>-120</td><td><7 ps rms</td><td></td></tr>
<tr><td>External Sample Clock Input Jitter Tolerance</td><td colspan="4">Cycle-cycle jitter ±300 ps
Period jitter ±1 ns</td><td>All values are typical.</td></tr>
<tr><td colspan="6">Exported Sample Clock Destination Characteristics</td></tr>
<tr><td rowspan="2">Exported Sample Clock Destinations</td><td colspan="4">1. PFI<0..1> (SMB front panel connectors)
2. NI PXI-5412: PXI_Trig<0..6> (PXI backplane connector)
NI PCI-5412: RTSI<0..6></td><td rowspan="4">Exported Sample clocks can be divided by integer K (1 ≤ K ≤ 4,194,304).</td></tr>
<tr><td colspan="2">Maximum Frequency</td><td colspan="2">Duty Cycle</td></tr>
<tr><td>PFI<0..1></td><td colspan="2">105 MHz</td><td colspan="2">25% to 65%</td></tr>
<tr><td>NI PXI-5412
PXI_Trig<0..6></td><td colspan="2">20 MHz</td><td colspan="2">—</td></tr>
<tr><td>NI PCI-5412
RTSI<0..6></td><td colspan="2">20 MHz</td><td colspan="2">—</td><td></td></tr>
</table>

Onboard Clock
(Internal VCXO)

Specification	Value	Comments
Clock Source	Internal sample clocks can either be locked to a Reference clock using a phase-locked loop or be derived from the onboard VCXO frequency reference.	—
Frequency Accuracy	±25 ppm	—

Phase-Locked Loop (PLL) Reference Clock

Specification	Value	Comments
Sources	1. **NI PXI-5412**—PXI_CLK10 (PXI backplane connector) **NI PCI-5412**—RTSI_7 (RTSI_CLK) 2. CLK IN (SMB front panel connector)	The PLL Reference clock provides the reference frequency for the PLL.
Frequency Accuracy	When using the PLL, the frequency accuracy of the NI 5412 is solely dependent on the frequency accuracy of the PLL Reference clock source.	—
Lock Time	≤200 ms	—
Frequency Range	5 MHz to 20 MHz in increments of 1 MHz. Default of 10 MHz. The PLL reference clock frequency must be accurate to ±50 ppm.	—
Duty Cycle Range	40% to 60%	—
Exported PLL Reference Clock Destinations	1. PFI<0..1> (SMB front panel connectors) 2. **NI PXI-5412**—PXI_Trig<0..6> (backplane connector) **NI PCI-5412**—RTSI<0..6>	—

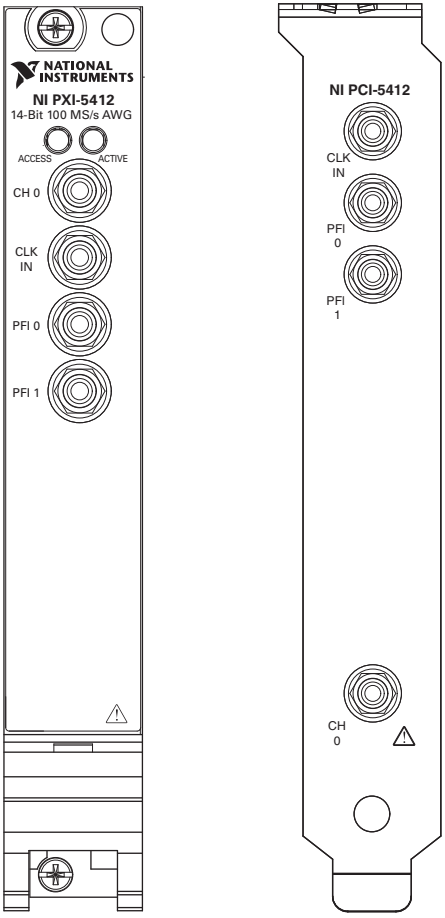
Physical

Specification	Value		Comments
	NI PXI-5412	NI PCI-5412	
Dimensions	3U, One Slot, PXI/cPCI Module 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)	34.1 × 2.0 × 10.7 cm (13.4 × 0.8 × 4.2 in.)	—
Weight	340 g (11 oz)	480 g (17 oz)	—
Front Panel Connectors			
Label	Function(s)	Connector Type	—
CH 0	Analog output	SMB (jack)	
CLK IN	Sample clock input and PLL reference clock input.	SMB (jack)	
PFI 0	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
PFI 1	Marker output, trigger input, sample clock output, exported trigger output, and PLL reference clock output.	SMB (jack)	
NI PXI-5412 Only—Front Panel LED Indicators			
Label	Function		For more information, refer to the *NI Signal Generators Help*.
ACCESS	The ACCESS LED indicates the status of the PCI bus and the interface from the NI 5412 to the controller.		
ACTIVE	The ACTIVE LED indicates the status of the onboard generation hardware of the NI 5412.		
Included Cable			
1 (NI part number 763541-01), 50 Ω, BNC Male to SMB Plug, RG223/U, Double Shielded, 1 m cable.			—

Note NI PXI-5412 modules of revision B or later are equipped with a modified PXI Express-compatible backplane connector. This modified connector allows the NI PXI-5412 to be installed in hybrid slots in a PXI Express chassis. To determine the revision of an NI PXI-5412 module, read the label on the underside of the NI PXI-5412. The label lists an assembly number of the format 192274x-01, where *x* is the revision.

Front Panel

Figure 2. NI PXI-5412 and NI PCI-5412 Front Panel



CLK IN
(Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value	Comments
Connector	SMB (jack)	—
Direction	Input	—
Destinations	1. Sample clock 2. PLL reference clock	—
Frequency Range	1 MHz to 105 MHz (Sample clock destination and sine waves) 200 kHz to 105 MHz (Sample clock destination and square waves) 5 MHz to 20 MHz (PLL Reference clock destination)	—
Input Voltage Range	Sine wave: 0.65 Vpk-pk to 2.8 Vpk-pk into 50 Ω (0 dBm to +13 dBm) Square wave: 0.2 Vpk-pk to 2.8 Vpk-pk into 50 Ω	—
Maximum Input Overload	±10 V	—
Input Impedance	50 Ω	—
Input Coupling	AC	—

PFI 0 and PFI 1
(Programmable Function Interface, Front Panel Connectors)

Specification	Value	Comments
Connectors	Two SMB (jack)	—
Direction	Bidirectional	—
Frequency Range	DC to 105 MHz	—

Specification	Value	Comments
As an Input (Trigger)		
Destinations	Start trigger	—
Maximum Input Overload	-2 V to +7 V	—
V_{IH}	2.0 V	
V_{IL}	0.8 V	
Input Impedance	1 kΩ	
As an Output (Event)		
Sources	1. Sample clock divided by integer K ($1 \leq K \leq 4{,}194{,}304$) 2. Sample clock timebase (100 MHz) divided by integer M ($2 \leq M \leq 4{,}194{,}304$) 3. PLL Reference clock 4. Marker 5. Exported Start trigger (Out Start Trigger)	—
Output Impedance	50 Ω	—
Maximum Output Overload	-2 V to +7 V	—
V_{OH}	Minimum: 2.9 V (open load), 1.4 V (50 Ω load)	Output drivers are +3.3 V TTL compatible.
V_{OL}	Maximum: 0.2 V (open load), 0.2 V (50 Ω load)	
Rise/Fall Time (20% to 80%)	≤2.0 ns	Load of 10 pF.

TClk Specifications

National Instruments TClk synchronization method and the NI-TClk instrument driver are used to align the Sample clocks on any number of SMC-based modules in a chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI Signal Generators Help*.

- Specifications are valid for any number of PXI modules installed in one NI PXI-1042 chassis.
- All parameters set to identical values for each SMC-based module.
- Sample Clock set to 100 MS/s, Divide-by-*N*, and all filters are disabled.
- For other configurations, including multichassis systems, contact NI Technical Support at `ni.com/support`.

Note Although you can use NI-TClk to synchronize nonidentical modules, these specifications apply only to synchronizing identical modules.

Specification	Value	Comments
Intermodule SMC Synchronization Using NI-TClk for Identical Modules (Typical)		
Skew	500 ps	Caused by clock and analog path delay differences. No manual adjustment performed.
Average Skew After Manual Adjustment	<10 ps	For information about manual adjustment, refer to the *Synchronization Repeatability Optimization topic* in the *NI-TClk Synchronization Help*. For additional help with the adjustment process, contact NI Technical Support at `ni.com/support`.
Sample Clock Delay/Adjustment Resolution	≤10 ps	—

Start Trigger

<table>
<tr><th>Specification</th><th colspan="2">Value</th><th>Comments</th></tr>
<tr><td>Sources</td><td colspan="2">1. PFI<0..1> (SMB front panel connectors)
2. NI PXI-5412—PXI_Trig<0..7> (PXI backplane connector)
NI PCI-5412—RTSI<0..7>
3. NI PXI-5412—PXI Star trigger (PXI backplane connector)
4. Software (use VI or function call)
5. Immediate (does not wait for a trigger). Default.</td><td>—</td></tr>
<tr><td>Modes</td><td colspan="2">1. Single
2. Continuous
3. Stepped
4. Burst</td><td>—</td></tr>
<tr><td>Edge Detection</td><td colspan="2">Rising</td><td>—</td></tr>
<tr><td>Minimum Pulse Width</td><td colspan="2">25 ns</td><td>Refer to t_{s1} at NI Signal Generators Help»Devices» NI 5412» Triggering» Trigger Timing.</td></tr>
<tr><td rowspan="5">Delay from Start Trigger to CH 0 Analog Output</td><td>Interpolation Factor</td><td>Typical Delay</td><td rowspan="5">Refer to t_{s2} at NI Signal Generators Help»Devices» NI 5412» Triggering» Trigger Timing. All values are typical.</td></tr>
<tr><td>Digital Interpolation Filter disabled.</td><td>43 Sample clock periods +110 ns</td></tr>
<tr><td>2</td><td>57 Sample clock periods +110 ns</td></tr>
<tr><td>4</td><td>63 Sample clock periods +110 ns</td></tr>
<tr><td>8</td><td>64 Sample clock periods +110 ns</td></tr>
</table>

Specification	Value	Comments
Trigger Exporting		
Exported Trigger Destinations	A signal used as a trigger can be routed out to any destination listed in the *Destinations* specification of the *Markers* section.	—
Exported Trigger Delay	65 ns (typical).	Refer to t_{s3} at **NI Signal Generators Help»Devices» NI 5412» Triggering» Trigger Timing**. All values are typical.
Exported Trigger Pulse Width	>150 ns	Refer to t_{s4} at **NI Signal Generators Help»Devices» NI 5412» Triggering» Trigger Timing**.

Markers

Specification	Value	Comments
Destinations	1. PFI<0..1> (SMB front panel connectors) 2. **NI PXI-5412**—PXI_Trig<0..6> (PXI backplane connector) **NI PCI-5412**—RTSI<0..6>	—
Quantity	One marker per segment.	—
Quantum	Marker position must be placed at an integer multiple of four samples.	—

Specification	Value		Comments
Width	>150 ns		Refer to t_{m2} at **NI Signal Generators Help» Fundamentals» Waveform Fundamentals» Events»Marker Events**.
Skew	Destination	With Respect to Analog Output	Refer to t_{m1} at **NI Signal Generators Help» Fundamentals» Waveform Fundamentals» Events»Marker Events**.
	PFI<0..1>	±2 Sample clock periods	
	NI PXI-5412 PXI_Trig<0..6> **NI PCI-5412** RTSI<0..6>	±2 Sample clock periods	

Arbitrary Waveform Generation Mode

Specification	Value			Comments
Memory Usage	The NI 5412 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters, such as number of segments in sequence list, maximum number of waveforms in memory, and number of samples available for waveform storage, are flexible and user defined.			—
Onboard Memory Size	8 MB standard: 8,388,608 bytes	32 MB option: 33,554,432 bytes	256 MB option: 268,435,456 bytes	—
Output Modes	Arbitrary waveform mode and arbitrary sequence mode			—
Arbitrary Waveform Mode	In arbitrary waveform mode, a single waveform is selected from the set of waveforms stored in onboard memory and generated.			—

<table>
<tr><th>Specification</th><th colspan="3">Value</th><th>Comments</th></tr>
<tr><td>Arbitrary Sequence Mode</td><td colspan="3">In arbitrary sequence mode, a sequence directs the NI 5412 to generate a set of waveforms in a specific order. Elements of the sequence are referred to as segments. Each segment is associated with a set of instructions. The instructions identify which waveform is selected from the set of waveforms in memory, how many loops (iterations) of the waveform are generated, and at which sample in the waveform a marker output signal is sent.</td><td>—</td></tr>
<tr><td rowspan="8">Minimum Waveform Size (Samples)</td><td>Trigger Mode</td><td>Arbitrary Waveform Mode</td><td>Arbitrary Sequence Mode</td><td rowspan="8">The Minimum Waveform Size is sample rate dependent in arbitrary sequence mode.</td></tr>
<tr><td>Single</td><td>16</td><td>16</td></tr>
<tr><td rowspan="2">Continuous</td><td rowspan="2">16</td><td>96 at >50 MS/s</td></tr>
<tr><td>32 at ≤50 MS/s</td></tr>
<tr><td rowspan="2">Stepped</td><td rowspan="2">32</td><td>96 at >50 MS/s</td></tr>
<tr><td>32 at ≤50 MS/s</td></tr>
<tr><td rowspan="2">Burst</td><td rowspan="2">16</td><td>512 at >50 MS/s</td></tr>
<tr><td>256 at ≤50 MS/s</td></tr>
<tr><td>Loop Count</td><td colspan="3">1 to 16,777,215
Burst trigger: Unlimited</td><td>—</td></tr>
<tr><td>Quantum</td><td colspan="3">Waveform size must be an integer multiple of four samples.</td><td>—</td></tr>
</table>

Specification	Value			Comments
Memory Limits				
	8 MB Standard	32 MB Option	256 MB Option	All trigger modes except where noted.
Arbitrary Waveform Mode, Maximum Waveform Memory	4,194,176 samples	16,777,088 samples	134,217,600 samples	
Arbitrary Sequence Mode, Maximum Waveform Memory	4,194,120 samples	16,777,008 samples	134,217,520 samples	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Waveforms	65,000 Burst trigger: 8,000	262,000 Burst trigger: 32,000	2,097,000 Burst trigger: 262,000	Condition: One or two segments in a sequence.
Arbitrary Sequence Mode, Maximum Segments in a Sequence	104,000 Burst trigger: 65,000	418,000 Burst trigger: 262,000	3,354,000 Burst trigger: 2,090,000	Condition: Waveform memory is <4,000 samples.

Calibration

Specification	Value	Comments
Self-Calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the DC gain and offset. The self-calibration is initiated by the user through the software and takes approximately 75 seconds to complete.	—
External Calibration	External calibration calibrates the VCXO, voltage reference, DC gain, and offset. Appropriate constants are stored in nonvolatile memory.	Also known as factory calibration.
Calibration Interval	Specifications valid within two years of external calibration.	—
Warm-up Time	15 minutes	—

Power

Specification	Normal Operation	Overload Operation	Comments
Total Power	22 W	26 W	All values are typical. Overload operation occurs when CH 0 is shorted to ground.

Software

Specification	Value	Comments
Driver Software	NI-FGEN is an IVI-compliant driver that allows you to configure, control, and calibrate the NI 5412. NI-FGEN provides application programming interfaces for many development environments.	—
Application Software	NI-FGEN provides programming interfaces for the following application development environments: • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C++ .NET • Microsoft Visual C/C++ • Microsoft Visual Basic	—
Interactive Control and Configuration Software	The FGEN Soft Front Panel supports interactive control of the NI 5412. The FGEN Soft Front Panel is included on the NI-FGEN driver DVD. Measurement & Automation Explorer (MAX) provides interactive configuration and test tools for the NI 5412. MAX is also included on the NI-FGEN DVD. You can use the NI 5412 with NI SignalExpress.	—

Environment

NI PXI-5412 Environment

Note To ensure that the NI PXI-5412 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5412 kit.

Specifications	Value	Comments
Operating Temperature	0 ºC to +55 ºC in all NI PXI chassis except the following: 0 ºC to +45 ºC when installed in an NI PXI-101x or NI PXI-1000B chassis. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Storage Temperature	-25 ºC to +85 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC 60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC 60068-2-56.	—
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	Spectral and jitter specifications could degrade.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Operating Vibration	5 Hz to 500 Hz, 0.31 g_{rms}. Meets IEC 60068-2-64.	Spectral and jitter specifications could degrade.
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—
Indoor use only.		

NI PCI-5412 Environment

Note To ensure that the NI PCI-5412 cools effectively, follow the guidelines in the *Maintain Forced-Air Cooling Note to Users* included in the NI 5412 kit. Also, to maximize airflow and extend the life of the device, leave any adjacent PCI slots empty.

Specifications	Value	Comments
Operating Temperature	0 ºC to +45 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Storage Temperature	-25 ºC to +85 ºC. Meets IEC 60068-2-1 and IEC 60068-2-2.	—
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC 60068-2-56.	—
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC 60068-2-56.	—
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.	—
Storage Vibration	5 Hz to 500 Hz, 2.46 g_{rms}. Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.	—
Altitude	2,000 m maximum (at 25 °C ambient temperature)	—
Pollution Degree	2	—
Indoor use only.		

Compliance and Certifications

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility (EMC)

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions, Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。 (For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

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Visit ni.com/register to register your National Instruments product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

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