SC Express

NI PXIe-4300 User Manual

8 Ch, 250 kS/s, 300 V Ch-Ch Isolated Analog Input Module

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Getting Started

The NI PXIe-4300 provides eight, simultaneous sampled, analog input channels, each with channel-to-channel and channel-to-earth isolation. The PXIe-4300 has a 10 V maximum measurement range that can be expanded to 300 V when using a TB-4300B. The PXIe-4300 can be used to measure current when using a TB-4300C, which provides 50 Ω resistors between the AI+ and AI- terminals to convert current to voltage for current measurements. Each channel of the NI PXIe-4300 has a 16-bit ADC with three programmable filter settings and four gain settings. Two input PFI lines are available on the module for triggering.

Installation

Refer to the *NI PXIe-4300 and TB-4300/B/C User Guide and Terminal Block Specifications* for step-by-step software and hardware installation instructions.

Module Specifications

Refer to the *NI PXIe-4300 Device Specifications* document for module specifications.

Module Accessories and Cables

Refer to the *NI PXIe-4300 and TB-4300/B/C User Guide and Terminal Block Specifications* for information about supported accessories and cables.

Module Self-Calibration

Self-calibration measures the onboard reference voltage of the module and adjusts the self-calibration constants to account for any errors caused by short-term fluctuations in the environment.

NI recommends that you self-calibrate the NI PXIe-4300 module after installation and whenever the ambient temperature changes. Self-calibration should be performed after the module has warmed up for the recommended time period. Refer to the *NI PXIe-4300 Device Specifications* for the module warm-up time and self-calibration conditions.

You can initiate self-calibration using Measurement & Automation Explorer (MAX), by completing the following steps.

1. Launch MAX.

2. Select **My System»Devices and Interfaces»*your module***.

3. Initiate self-calibration using one of the following methods:

    •   Click **Self-Calibrate** in the upper right corner of MAX.

    •   Right-click the name of the module in the MAX configuration tree and select **Self-Calibrate** from the drop-down menu.

Note   You can also programmatically self-calibrate the module with NI-DAQmx, as described in *Device Calibration* in the *NI-DAQmx Help* or the *LabVIEW Help*.

2

Using the NI PXIe-4300

This chapter describes how to connect AI inputs to the NI PXIe-4300 module. It also provides the front signal pin assignments of the module.

Connecting Signals

Figure 2-1 shows correct and incorrect AI source grounding.

Figure 2-1. NI PXIe-4300 AI Source Grounding Diagram
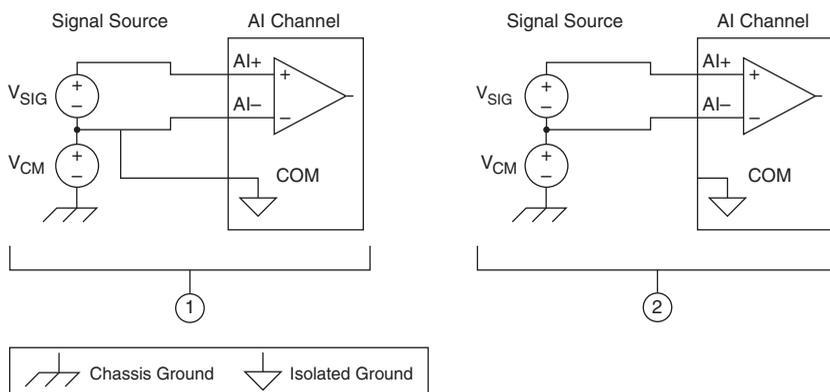
| 1 | Correct AI Source Grounding | 2 | Incorrect AI Source Grounding |

The COM terminal for each channel must be connected to the reference ground of the AI source. Failure to connect COM results in inaccurate measurements. You can connect the COM terminal directly to the negative terminal of the source as shown in Figure 2-1 or to an isolated ground of the source as long as the working voltage specification of the NI PXIe-4300 is not violated.

For best results, wire the AI+ and AI- signals as twisted pairs and use the COM as a shield. The COM connection should be made as close to the source as possible to take advantage of the differential nature of this device.

Refer to the *NI PXIe-4300 and TB-4300/B/C User Guide and Terminal Block Specifications* for details about signal terminal locations.

Device Pinout

Table 2-1 shows the pinout of the front connector of the NI PXIe-4300. Refer to the *I/O Connector Signal Description* section for definitions of each signal. Refer to the *NI PXIe-4300 and TB-4300/B/C User Guide and Terminal Block Specifications* for signal locations on the terminal block.

Table 2-1. Front Signal Pin Assignments

Front Connector Diagram	Pin Number	Column A	Column B	Column C	Channel
	32	COM 0	—	AI 0+	
	31	—	—	AI 0-	0
	30	—	—	—	
	29	COM 1	—	AI 1+	
	28	—	—	AI 1-	1
	27	—	—	—	
	26	COM 2	—	AI 2+	
	25	—	—	AI 2-	2
	24	—	—	—	
	23	COM 3	—	AI 3+	
	22	—	—	AI 3-	3
	21	—	—	—	
	20	COM 4	—	AI 4+	
	19	—	—	AI 4-	4
	18	—	—	—	
	17	COM 5	—	AI 5+	
	16	—	—	AI 5-	5
	15	—	—	—	
	14	COM 6	—	AI 6+	
	13	—	—	AI 6-	6
	12	—	—	—	
	11	COM 7	—	AI 7+	
	10	—	—	AI 7-	7
	9	—	—	—	
	8	COM 7	COM 7	COM 7	
	7	—	PFI 0	PFI 1	
	6	—	—	—	
	5	—	—	—	No Channel
	4	—	—	—	
	3	—	—	—	
	2	RSVD	COM 7	RSVD	
	1	RSVD	RSVD	RSVD	

Front Connector Diagram:

Column
A B C

32 ○ ○ ○
31 ○ ○ ○
30 ○ ○ ○
29 ○ ○ ○
28 ○ ○ ○
27 ○ ○ ○
26 ○ ○ ○
25 ○ ○ ○
24 ○ ○ ○
23 ○ ○ ○
22 ○ ○ ○
21 ○ ○ ○
20 ○ ○ ○
19 ○ ○ ○
18 ○ ○ ○
17 ○ ○ ○
16 ○ ○ ○
15 ○ ○ ○
14 ○ ○ ○
13 ○ ○ ○
12 ○ ○ ○
11 ○ ○ ○
10 ○ ○ ○
9 ○ ○ ○
8 ○ ○ ○
7 ○ ○ ○
6 ○ ○ ○
5 ○ ○ ○
4 ○ ○ ○
3 ○ ○ ○
2 ○ ○ ○
1 ○ ○ ○

— is no connection,
isolation barrier,
RSVD is reserved

I/O Connector Signal Description

Table 2-2 describes the signals found on the I/O connectors.

Table 2-2. I/O Connector Signal Descriptions

Signal Names	Reference	Direction	Description
COM <0..7>	—	—	Analog Input Isolated Common Ground—These terminals are the reference point for differential analog input measurements.
AI <0..7>+, AI <0..7>-	COM <0..7>	Input	Analog Input Channels 0 to 7—AI+ and AI- are the positive and negative inputs of differential analog input.
PFI <0,1>	COM 7	Input	Programmable Function Interface Channels 0 to 1—Each of these terminals can be individually configured as PFI terminals. They can be used to supply a start, reference, or pause trigger, or be used as an external timing source for AI. **Note**: These channels may only be referenced to channel 7 in order to maintain safety isolation.
RSVD	COM 7	Bi-Directional	These pins are reserved for communication with the accessory.

NI PXIe-4300 Block Diagram

Figure 2-2 shows the block diagram of the NI PXIe-4300 module.

Figure 2-2. NI PXIe-4300 Block Diagram
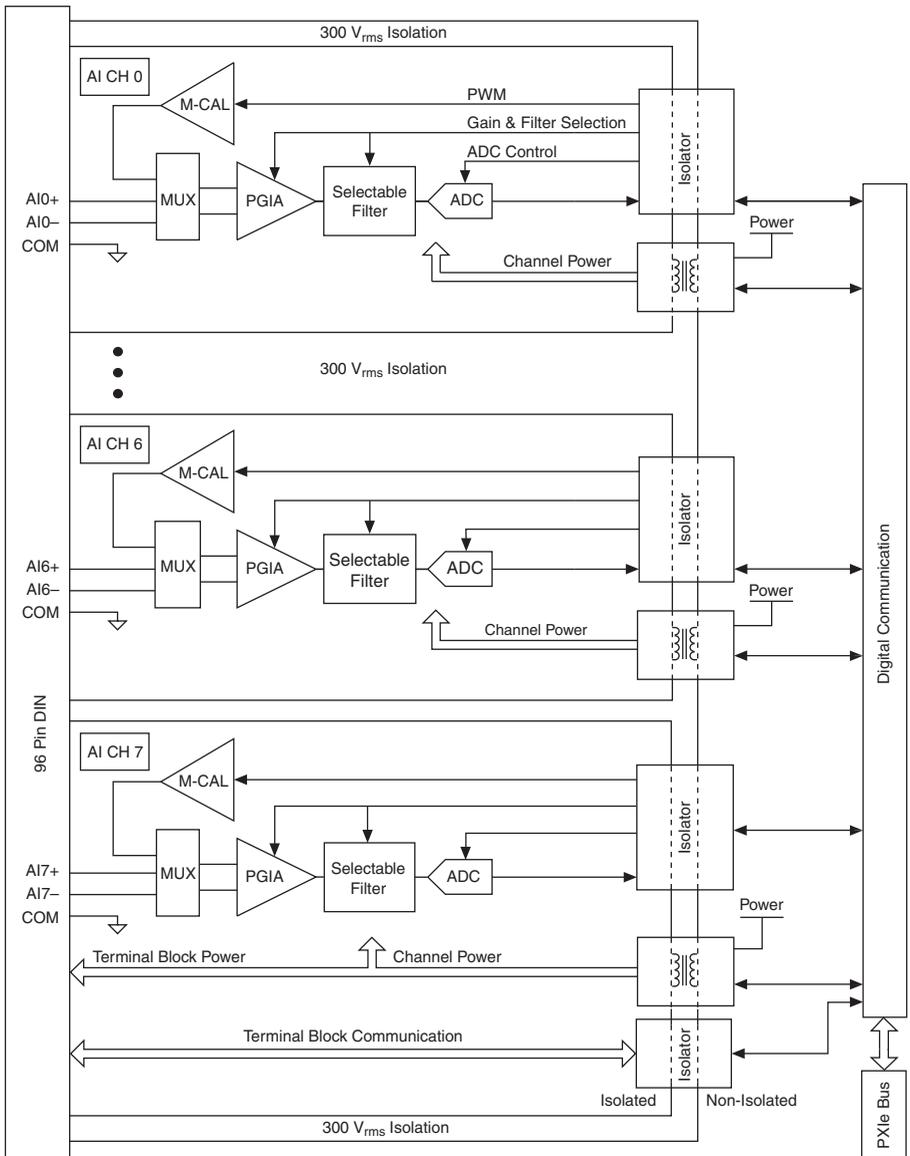
Signal Acquisition Considerations

This section contains information about signal acquisition concepts including timing, triggering, and synchronization.

Input Ranges

Input range refers to the set of input voltages that an analog input channel can digitize with the specified accuracy. The programmable gain instrumentation amplifier (PGIA) amplifies or attenuates the AI signal depending on the input range. You can individually program the input range of each AI channel on your NI PXIe-4300 module.

The input range affects the resolution of the NI PXIe-4300 module for an AI channel. Resolution refers to the voltage of one ADC code. For example, a 16-bit ADC converts analog inputs into one of $65{,}536\ (= 2^{16})$ codes—that is, one of 65,536 possible digital values. These values are spread fairly evenly across the input range. So, for an input range of -10 V to 10 V, the voltage of each code of a 16-bit ADC is:

$$\frac{10\ V - (-10\ V)}{2^{16}} \;=\; 305\ \mu V$$

Choose an input range that matches the expected input range of your signal. A large input range can accommodate a large signal variation, but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution, but may result in the input signal going out of range.

Note   The NI PXIe-4300 module uses a calibration method that requires codes (typically about 5% of the codes) outside of the specified range. This calibration method improves absolute accuracy, but it decreases the nominal resolution of input ranges by about 5% over what the formula shown above would indicate.

Table 2-3 shows the input ranges and resolutions supported by the NI PXIe-4300 module.

Table 2-3. NI PXIe-4300 Input Range and Nominal Resolution

Input Range	Nominal Resolution Assuming 5% Over Range
-10 V to 10 V	320 μV
-5 V to 5 V	160 μV
-2 V to 2 V	64 μV
-1 V to 1 V	32 μV

ADC

The analog-to-digital converter (ADC) digitizes the AI signal by converting the analog voltage into a digital number. The NI PXIe-4300 module has eight ADCs. Multiplexers (mux) are used to select filter settings and to select external or internal sources for calibration.

Settling time refers to the time it takes the PGIA to amplify the input signal to the desired accuracy before it is sampled by the ADC.

The PGIA can amplify or attenuate an AI signal to ensure that you use the maximum resolution of the ADC.

Analog Input Data Acquisition Methods

When performing analog input measurements, you can either perform software-timed or hardware-timed acquisitions.

Software-Timed Acquisitions

With a software-timed acquisition, software controls the rate of the acquisition. Software sends a separate command to the hardware to initiate each ADC conversion. In NI-DAQmx, software-timed acquisitions are referred to as having on-demand timing. Software-timed acquisitions are also referred to as immediate or static acquisitions and are typically used for reading a single sample of data.

Hardware-Timed Acquisitions

With hardware-timed acquisitions, a digital hardware signal (AI Sample Clock) controls the rate of the acquisition. This signal can be generated internally on your device or provided externally.

Hardware-timed acquisitions have several advantages over software-timed acquisitions:

* The time between samples can be much shorter.
* The timing between samples is deterministic.
* Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or hardware-timed single point (HWTSP). A buffer is a temporary storage in computer memory for to-be-transferred samples.

* Buffered—In a buffered acquisition, data is moved from the onboard FIFO memory of the DAQ device to a PC buffer using DMA before it is transferred to application memory. Buffered acquisitions typically allow for much faster transfer rates than HWTSP acquisitions because data is moved in large blocks, rather than one point at a time.

    One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous:

    – Finite sample mode acquisition refers to the acquisition of a specific, predetermined number of data samples. Once the specified number of samples has been read in, the acquisition stops. If you use a reference trigger, you must use finite sample mode.

– Continuous acquisition refers to the acquisition of an unspecified number of samples. Instead of acquiring a set number of data samples and stopping, a continuous acquisition continues until you stop the operation. Continuous acquisition is also referred to as double-buffered or circular-buffered acquisition.

If data cannot be transferred across the bus fast enough, the FIFO becomes full. New acquisitions overwrite data in the FIFO before it can be transferred to host memory. The device generates an error in this case. With continuous operations, if the application program does not read data out of the PC buffer fast enough to keep up with the data transfer, the buffer could reach an overflow condition, causing an error to be generated.

• Hardware-timed single point (HWTSP)—Typically, HWTSP operations are used to read single samples at known time intervals. While buffered operations are optimized for high throughput, HWTSP operations are optimized for low latency and low jitter. In addition, HWTSP can notify software if it falls behind hardware. These features make HWTSP ideal for real-time control applications. HWTSP operations, in conjunction with the wait for next sample clock function, provide tight synchronization between the software layer and the hardware layer. Refer to the whitepaper *NI-DAQmx Hardware-Timed Single Point Lateness Checking* for more information. To access this document, go to ni.com/info and enter the Info Code daqhwtsp.

Analog Input Filter

The NI PXIe-4300 has selectable filter settings per channel. Each channel can independently be set to one of the three available lowpass filter settings: 10 kHz, 100 kHz, and Disable. The 10 kHz and 100 kHz filters are 2-pole Butterworth filters, and their designation refers to the -3 dB cut-off frequency. The *Disable* setting bypasses the filters and allows measurements in the full bandwidth of the NI PXIe-4300.

Gain

The NI PXIe-4300 module implements the different analog input COM-reference settings by routing different signals to the PGIA. The PGIA is a differential amplifier so it amplifies (or attenuates) the difference in voltage between its two inputs. The PGIA drives the ADC with this amplified voltage. The amount of amplification (the gain), is determined by the analog input range, as shown in Figure 2-3.

Note   Time and temperature can introduce gain and offset AI errors at runtime. You can minimize these errors by self-calibrating the module.

Figure 2-3. NI PXIe-4300 PGIA

$$V_m = [V_{in+} - V_{in-}] \times Gain$$
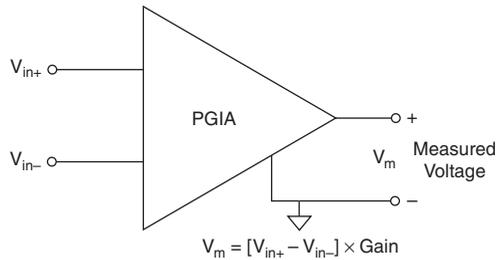
Analog Input Timing Signals

In order to provide all of the timing functionality described throughout this section, NI PXIe-4300 modules have a flexible timing engine.

NI PXIe-4300 modules use AI Sample Clock (ai/SampleClock) to perform simultaneous sampling on all active analog channels. Since there is one ADC per channel, AI Sample Clock controls the sample period on all the channels in the task.

An acquisition with posttrigger data allows you to view data that is acquired after a trigger event is received. A typical posttrigger DAQ sequence is shown in Figure 2-4. The sample counter is loaded with the specified number of posttrigger samples, in this example, five. The value decrements with each pulse on AI Sample Clock, until the value reaches zero and all desired samples have been acquired.

Figure 2-4. Typical Posttriggered DAQ Sequence
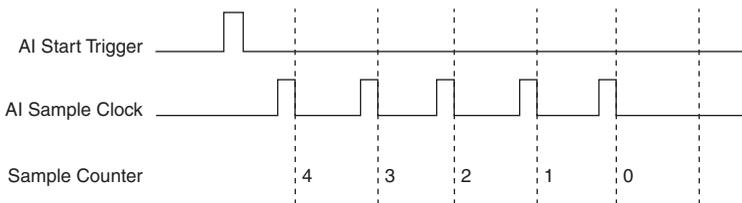
An acquisition with pretrigger data allows you to view data that is acquired before the trigger of interest, in addition to data acquired after the trigger. Figure 2-5 shows a typical pretrigger DAQ sequence. The AI Start Trigger signal (ai/StartTrigger) can be either a hardware or software signal. If AI Start Trigger is set up to be a software start trigger, an output pulse appears on the ai/StartTrigger line when the acquisition begins. When the AI Start Trigger pulse occurs, the sample counter is loaded with the number of pretrigger samples, in this example, four. The value decrements with each pulse on AI Sample Clock, until the value reaches zero. The sample counter is then loaded with the number of posttrigger samples, in this example, three.

Figure 2-5. Typical Pretriggered DAQ Sequence
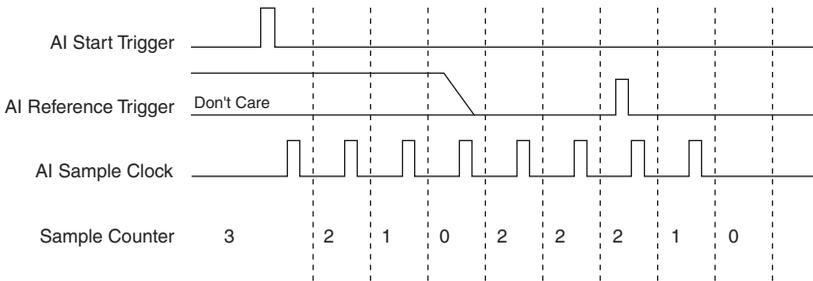
If an AI Reference Trigger (ai/ReferenceTrigger) pulse occurs before the specified number of pretrigger samples are acquired, the trigger pulse is ignored. Otherwise, when the AI Reference Trigger pulse occurs, the sample counter value decrements until the specified number of posttrigger samples have been acquired. For more information about start and reference triggers, refer to the *Analog Triggering* section.

NI PXIe-4300 modules feature the following analog input timing signals:

- AI Sample Clock Signal
- AI Sample Clock Timebase Signal
- AI Start Trigger Signal
- AI Reference Trigger Signal
- AI Pause Trigger Signal

Aggregate versus Single Channel Sample Rates

NI PXIe-4300 modules have one ADC per channel so the single channel maximum sample rate can be achieved on each channel. The maximum single channel rate is the fastest you can acquire data on the device from a single or multiple channels and still achieve accurate results.

The total aggregate determines the maximum bus bandwidth used by the device. The total aggregate sample rate is the product of the maximum sample rate for a single channel multiplied by the number of AI channels that the device support.

Table 2-4 shows the single channels and total aggregate rates for NI PXIe-4300 modules.

Table 2-4. Analog Input Rates for NI PXIe-4300 Modules

Single Channel	Total Aggregate
250 kS/s	2 MS/s

AI Sample Clock Signal

Use the AI Sample Clock (ai/SampleClock) signal to initiate a set of measurements. Your NI PXIe-4300 module samples the AI signals of every channel in the task once for every AI Sample Clock. A measurement acquisition consists of one or more samples.

You can specify an internal or external source for AI Sample Clock. You also can specify whether the measurement sample begins on the rising edge or falling edge of AI Sample Clock.

Using an Internal Source

One of the following internal signals can drive AI Sample Clock:

- AI Sample Clock Timebase (divided down).
- A pulse initiated by host software that does a software, *on demand*, acquisition.

A programmable internal counter divides down the sample clock timebase.

Several other internal signals can be routed to AI Sample Clock through internal routes. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

Using an External Source

Use one of the following external signals as the source of AI Sample Clock:

- PFI <0, 1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A, B>

Routing AI Sample Clock Signal to an Output Terminal

You can route AI Sample Clock out to any PXI_Trig <0..7>, or PXIe_DSTARC terminal. This pulse is always active high.

All PFI terminals are configured as inputs by default.

Other Timing Requirements

Your DAQ device only acquires data during an acquisition. The device ignores AI Sample Clock when a measurement acquisition is not in progress. During a measurement acquisition, you can cause your DAQ device to ignore AI Sample Clock using the AI Pause Trigger signal.

A counter/timing engine on your device internally generates AI Sample Clock unless you select some external source. AI Start Trigger starts this counter and either software or hardware can stop it once a finite acquisition completes. When using an internally generated AI Sample Clock, you also can specify a configurable delay from AI Start Trigger to the first AI Sample Clock pulse. By default, this delay is set to two ticks of the AI Sample Clock Timebase signal.

Figure 2-6 shows the relationship of AI Sample Clock to AI Start Trigger.

Figure 2-6. AI Sample Clock and AI Start Trigger
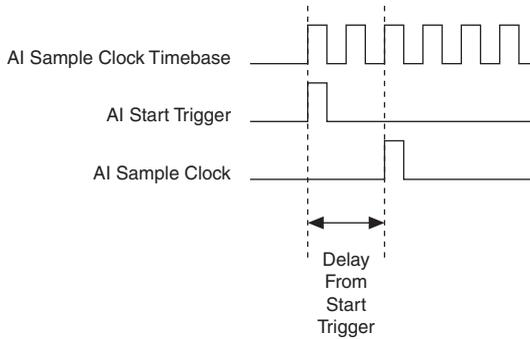
AI Sample Clock Timebase Signal

You can route any of the following signals to be the AI Sample Clock Timebase (ai/SampleClockTimebase) signal:

- 100 MHz Timebase (default)
- 20 MHz Timebase
- 100 kHz Timebase
- PXI_CLK10
- PXI_Trig <0..7>
- PFI <0,1>
- PXI_STAR
- PXIe_DSTAR <A, B>

AI Sample Clock Timebase is not available as an output on the I/O connector. AI Sample Clock Timebase is divided down to provide one of the possible sources for AI Sample Clock. You can configure the polarity selection for AI Sample Clock Timebase as either rising or falling edge, except on 100 MHz Timebase or 20 MHz Timebase.

AI Start Trigger Signal

Use the AI Start Trigger (ai/StartTrigger) signal to begin a measurement acquisition. A measurement acquisition consists of one or more samples. If you do not use triggers, begin a measurement with a software command by starting a task, which sends the software command that begins the measurement. Once the acquisition begins, configure the acquisition to stop:

- When a certain number of points are sampled (in finite mode)
- After a hardware reference trigger (in finite mode)
- With a software command (in continuous mode)

An acquisition that uses a start trigger (but not a reference trigger) is sometimes referred to as a posttriggered acquisition.

Retriggerable Analog Input

The AI Start Trigger can also be configured to be retriggerable. The timing engine will generate the sample and convert clocks for the configured acquisition in response to each pulse on an AI Start Trigger signal.

The timing engine ignores the AI Start Trigger signal while the clock generation is in progress. After the clock generation is finished, the counter waits for another Start Trigger to begin another clock generation. Figure 2-7 shows a retriggerable analog input with three AI channels and four samples per trigger.

Figure 2-7. Retriggerable Analog Input
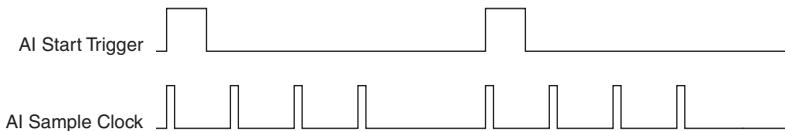
Note Waveform information from LabVIEW will not reflect the delay between triggers. They will be treated as a continuous acquisition with constant t0 and dt information.

Reference triggers are not retriggerable.

Using a Digital Source

To use AI Start Trigger with a digital source, specify a source and an edge. The source can be any of the following signals:

- PFI <0, 1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A, B>

The source also can be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

You also can specify whether the measurement acquisition begins on the rising edge or falling edge of AI Start Trigger.

Routing AI Start Trigger to an Output Terminal

You can route AI Start Trigger out to any PXI_Trig <0..7> or PXIe_DSTARC terminal. The output is an active high pulse. All PFI terminals are configured as inputs by default.

The device also uses AI Start Trigger to initiate pretriggered DAQ operations. In most pretriggered applications, a software trigger generates AI Start Trigger. Refer to the *AI Reference Trigger Signal* section for a complete description of the use of AI Start Trigger and AI Reference Trigger in a pretriggered DAQ operation.

AI Reference Trigger Signal

Use AI Reference Trigger (ai/ReferenceTrigger) signal to stop a measurement acquisition. To use a reference trigger, specify a buffer of finite size and a number of pretrigger samples (samples that occur before the reference trigger). The number of posttrigger samples (samples that occur after the reference trigger) desired is the buffer size minus the number of pretrigger samples.

Once the acquisition begins, the DAQ device writes samples to the buffer. After the DAQ device captures the specified number of pretrigger samples, the DAQ device begins to look for the reference trigger condition. If the reference trigger condition occurs before the DAQ device captures the specified number of pretrigger samples, the DAQ device ignores the condition.

If the buffer becomes full, the DAQ device continuously discards the oldest samples in the buffer to make space for the next sample. This data can be accessed (with some limitations) before the DAQ device discards it. Refer to the KnowledgeBase document, *Can a Pretriggered Acquisition be Continuous?*, for more information. To access this KnowledgeBase, go to ni.com/info and enter the Info Code rdcanq.

When the reference trigger occurs, the DAQ device continues to write samples to the buffer until the buffer contains the number of posttrigger samples desired. Figure 2-8 shows the final buffer.

Figure 2-8. Reference Trigger Final Buffer
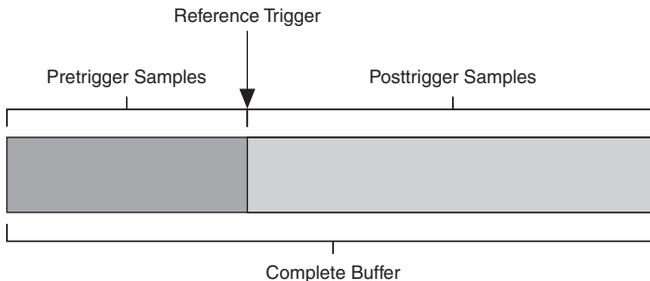
Using a Digital Source

To use AI Reference Trigger with a digital source, specify a source and an edge. The source can be any of the following signals:

- PFI <0, 1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A, B>

The source also can be one of several internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

You also can specify whether the measurement acquisition stops on the rising edge or falling edge of AI Reference Trigger.

Using an Analog Source

When you use an analog trigger source, the acquisition stops on the first rising edge of the Analog Comparison Event signal.

Routing AI Reference Trigger Signal to an Output Terminal

You can route AI Reference Trigger out to any PXI_Trig <0..7>, or PXIe_DSTARC terminal.

All PFI terminals are configured as inputs by default.

AI Pause Trigger Signal

Use the AI Pause Trigger (ai/PauseTrigger) signal to pause and resume a measurement acquisition. The internal sample clock pauses while the external trigger signal is active and resumes when the signal is inactive. You can program the active level of the pause trigger to be high or low, as shown in Figure 2-9. In the figure, T represents the period, and A represents the unknown time between the clock pulse and the posttrigger.

Figure 2-9. Halt (Internal Clock) and Free Running (External Clock)
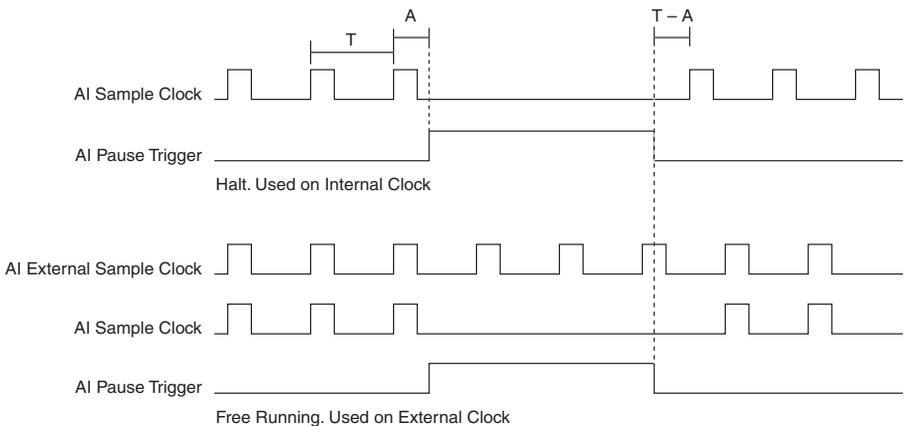
Using a Digital Source

To use AI Pause Trigger, specify a source and a polarity. The source can be any of the following signals:

- PFI <0, 1>
- PXI_Trig <0..7>
- PXI_STAR
- PXIe_DSTAR <A, B>

The source also can be one of several other internal signals on your DAQ device. Refer to *Device Routing in MAX* in the *NI-DAQmx Help* or the *LabVIEW Help* for more information.

Routing AI Pause Trigger Signal to an Output Terminal

You can route AI Pause Trigger out to any PXI_Trig <0..7>, PXI_STAR, or PXIe_DSTARC terminal.

Note   Pause triggers are only sensitive to the level of the source, not the edge.

Getting Started with AI Applications in Software

You can use the NI PXIe-4300 modules in the following analog input applications:

• Simultaneous sampling

• Single-point analog input

• Finite analog input

• Continuous analog input

You can perform these applications through DMA or programmed I/O data transfer mechanisms. Some of the applications also use start and reference pause triggers.

Note   For more information about programming analog input applications and triggers in software, refer to the *NI-DAQmx Help* or the *LabVIEW Help* in version 8.0 or later.

NI PXIe-4300 modules use the NI-DAQmx driver. NI-DAQmx includes a collection of programming examples to help you get started developing an application. You can modify example code and save it in an application. You can use examples to develop a new application or add example code to an existing application.

To locate LabVIEW, LabWindows™/CVI™, Measurement Studio, Visual Basic, and ANSI C examples, refer to the KnowledgeBase document, *Where Can I Find NI-DAQmx Examples?*, by going to ni.com/info and entering the Info Code daqmxexp.

External Reference Clock

An external reference clock can be used as a source for the internal timebase on the NI PXIe-4300. This clock can be sourced using the signals shown in Table 2-5. Since the clock is the input of a PLL, it must be 5 MHz, 10 MHz, 20 MHz, or 100 MHz. A PLL locks to the signal and produces a 100 MHz output, which is then divided down to produce the three timebases of 100 MHz, 20 MHz and 100 kHz. These timebases can then be used to generate sample clocks on the device. This circuit also enables the output of a 10 MHz RefClk that can be routed to PXI_Trig <0..7> and used by another device as its own External Reference Clock as shown in Figure 2-10.

Table 2-5. Clock Signal Sourcing

Signal	Description
PXI_Trig<0..7>	Bi-Directional bus connecting each board in the chassis.
PFI<0, 1>	External User Input
PXIe_Clk100	100 MHz clock routed to all slots in the chassis.
PXI_STAR	Point to point route from the System Timing Slot to all other slots.
PXIe_DSTAR<A, B>	Point to point differential routes from the System Timing Slot to all other slots.

Figure 2-10. External Clock Reference
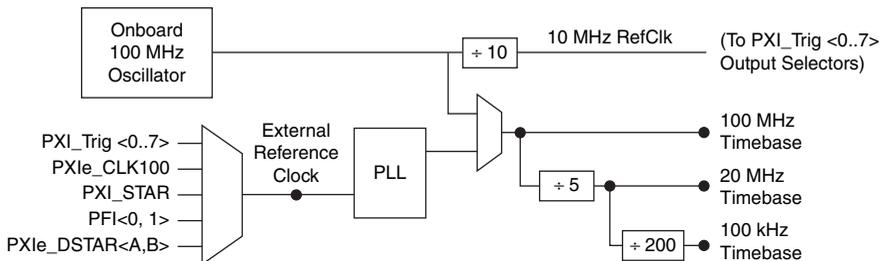
⚠ **Caution** Do not disconnect an external reference clock once the modules have been synchronized or are used by a task. Doing so may cause NI-DAQmx to return an error. Make sure that all tasks using a reference clock are stopped before disconnecting it.

10 MHz Reference Clock

The 10 MHz reference clock can be used to synchronize other devices to the NI PXIe-4300 module. The 10 MHz reference clock can be routed to the PXI_Trig <0..7> terminals. Other devices connected to the PXI_Trig bus can use this signal as a clock input.

The 10 MHz reference clock is generated by dividing down the onboard oscillator.

Synchronizing Multiple Devices

On PXI Express systems, you can synchronize devices to PXIe_CLK100. In this application the PXI Express chassis acts as the initiator. Each PXI Express module uses PXIe_CLK100 as its reference clock. Adding channels from multiple modules to the same NI-DAQmx task will perform synchronization automatically.

Another option in PXI Express systems is to use PXI_STAR. The Star Trigger controller device acts as the initiator and drives PXI_STAR with a clock signal. Each target module uses PXI_STAR as its external reference clock.

With the PXI_Trig bus and the routing capabilities of the NI PXIe-4300 module, there are several ways to synchronize multiple modules depending on your application.

To synchronize multiple modules to a common timebase, choose one module—the master—to generate the timebase. The master module routes its 10 MHz reference clock to one of the PXI_Trig <0..7> signals.

All modules (including the master module) receive the 10 MHz reference clock from PXI_Trig. This signal becomes the external reference clock. A PLL on each module generates the internal timebases synchronous to the external reference clock.

Sharing a trigger between multiple devices using PXI trigger lines introduces skew in the trigger signal, due to the propagation delay of the signal. The NI PXIe-4300 can compensate for that skew by locking the trigger to a clock (PXIe_SYNC100) that is derived from the reference clock (PXIe_CLK100). When you lock triggers to a clock, the device responds to those triggers on a subsequent edge of that clock, rather than immediately. Therefore, skew correction results in increased latency.

When you add multiple NI PXIe-4300 modules to the same NI-DAQmx task, NI-DAQmx automatically enables trigger skew correction. To enable trigger skew correction for applications that use multiple NI-DAQmx tasks, specify which device is the master and which devices are the slaves using the **SyncType** DAQmx Trigger property.

Once all of the devices are using or referencing a common timebase, you can synchronize operations across them by sending a common start trigger out across the PXI_Trig bus and setting their sample clock rates to the same value as shown in Figure 2-11.

Figure 2-11. Synchronization Operation
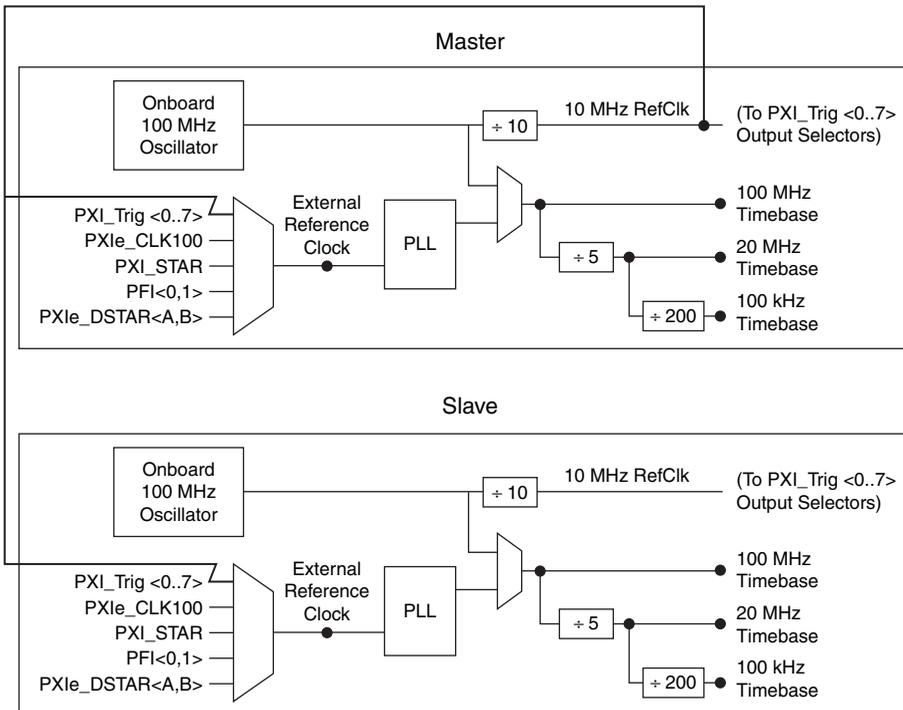
Triggering

The following sections provide details about analog and digital triggering of the NI PXIe-4300 module.

Analog Triggering

You can configure the NI PXIe-4300 analog trigger circuitry to monitor any input channel from which you acquire data. Choosing an input channel as the trigger channel does not influence the input channel acquisition capabilities.

The analog trigger signal can be used as a reference trigger only. This restriction is due to the fact that the analog trigger circuit operates on digitized ADC data, requiring the acquisition to be running in order for the analog trigger circuit to operate. In a reference triggered acquisition, you configure the device to acquire a certain number of pre-trigger samples and a certain number of post-trigger samples.

The trigger circuit generates an internal digital trigger based on the input signal and the user-defined trigger levels.

For example, you can configure the device to generate an analog comparison event after the input signal crosses a specific threshold. You also can route the resulting reference trigger event to the PXI Express trigger bus to synchronize the triggering of other devices in the system.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate. Sampling at a rate less than twice the bandwidth of interest may cause the trigger signal to not reliably be detected.

You can use the following analog triggering modes with the NI PXIe-4300 modules: rising-edge, rising-edge with hysteresis, falling-edge, falling-edge with hysteresis, entering window, and leaving window.

Analog Edge Triggering

For analog edge triggering, configure the device to detect a certain signal level and slope, either rising or falling. Figure 2-12 shows an example of rising edge analog triggering. The trigger asserts when the signal starts below level and then crosses above level.

Figure 2-12. Analog Trigger Level
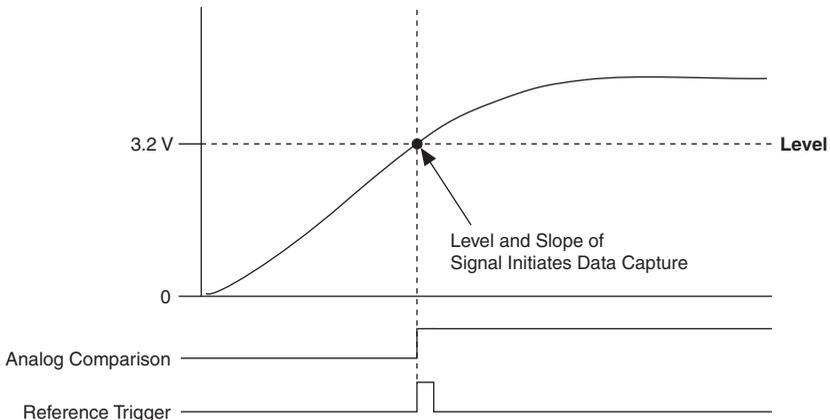
Analog Edge Triggering With Hysteresis

When you add hysteresis to analog edge triggering, you add a window above or below the trigger level. This trigger often is used to reduce false triggering due to noise or jitter in the signal. For example, if you add a hysteresis of 1 V to the example in Figure 2-12, which uses a level of 3.2 V, the signal must start at or drop below 2.2 V to arm the trigger. The trigger asserts when the signal rises above 3.2 V and deasserts when it falls below 2.2 V, as shown in Figure 2-13.

Figure 2-13. Analog Edge Triggering with Hysteresis on Rising Slope
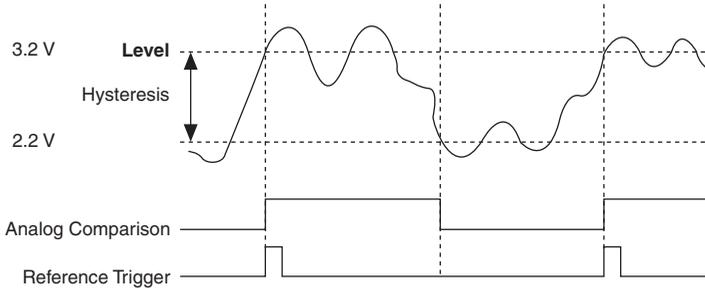
When using hysteresis with a falling slope, the trigger is armed when the signal starts above Level, plus the hysteresis value, and asserts when the signal crosses below Level. For example, if you add a hysteresis of 1 V to a level of 3.2 V, the signal must start at or rise above 4.2 V to arm the trigger. The trigger asserts as the signal falls below 3.2 V and deasserts when it rises above 4.2 V, as shown in Figure 2-14.

**Figure 2-14.** Analog Edge Triggering with Hysteresis on Falling Slope
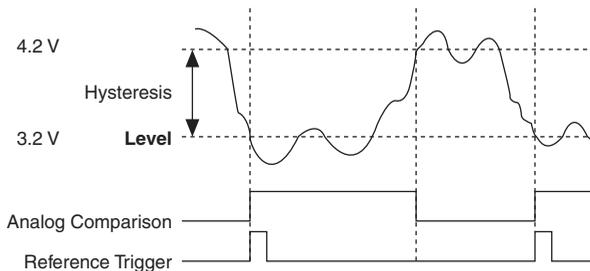
Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two levels. Specify the levels by setting a value for the top and bottom window boundaries. Figure 2-15 demonstrates a trigger that acquires data when the signal enters the window. You can also program the trigger circuit to acquire data when the signal leaves the window.

Figure 2-15. Window Triggering
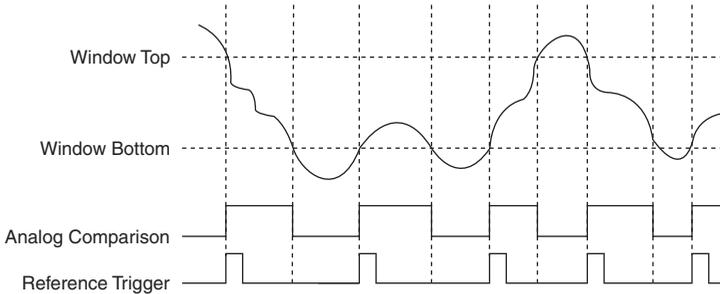
Digital Input Triggering

You can configure the NI PXIe-4300 device to start or pause an acquisition in response to a digital trigger signal from either PFI <0, 1>, PXIe_DSTAR <A, B>, PXI_Trig <0..7>, or PXI_STAR. The trigger circuit can respond to a rising, falling, or level sensitive signal, in one of the following three modes:

- Start—Begins an acquisition when trigger is met.
- Reference—A certain number of pre-trigger and post-trigger samples are specified around the trigger.
- Pause—Acquisition is put on hold when trigger is met (level sensitive only).

In addition, the trigger circuit provides a programmable filter to help with noisy trigger signals. The filter checks that the trigger condition is met for different time intervals before triggering. The filter can select from 90 ns, 5.12 μs, 2.56 ms, or a custom defined time interval. For information about configuring digital filters, refer to the *NI-DAQmx Help*.

TB-4300/B/C Accessory

The TB-4300/B/C terminal blocks provide screw terminals for access to the module.

- The TB-4300 is strictly a voltage feedthrough terminal block.
- The TB-4300B provides 30x attenuation to the input voltage with additional high-voltage protection circuitry and expands the range of the NI PXIe-4300 to 300 V.
- The TB-4300C provides 50 Ω resistors between the AI+ and AI- terminals to convert current to voltage for current measurements.

Refer to the *NI PXIe-4300 and TB-4300/B/C User Guide and Terminal Block Specifications* for more information about the TB-4300/B/C terminal block accessory.

Scaling constants for the TB-4300B are stored in the EEPROM and are used by software to automatically apply scaling to the signal for the selected range. When using the TB-4300C, software automatically applies scaling to convert the measurement to current using the nominal scaling factor of 50. The TB-4300C does not include scaling constants in the EEPROM.

Accessory Auto-Detection

NI SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any scaling information associated with the terminal block.

MAX allows you to see what accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status. Select **Start»All Programs»National Instruments»NI-DAQmx»NI-DAQmx Help**.

Accessory Power

The NI PXIe-4300 provides auxiliary power for accessories connected to the module and has protection in the event of a fault condition. If a fault occurs in the form of an over-power condition, the power supply latches off until it is reset. To reset after a fault condition perform a Device Reset in MAX or programmatically in your ADE.

Isolation

⚠ **Caution** Refer to the *Read Me First: Safety and Electromagnetic Compatibility*, included with your module, for more safety information.

The NI PXIe-4300 provides 300 V channel-to-channel basic isolation as well as 300 V channel-to-earth reinforced isolation. This rating is intended for measurements within Measurement Category II. These isolation levels are verified with a 5second dielectric withstand test. Refer to the *NI PXIe-4300 Device Specifications* for details.

Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system. This category refers to local-level electrical distribution, such as that provided by a standard wall outlet, for example, 115 V for U.S. or 230 V for Europe.

Do not connect the NI PXIe-4300 module to signals or use for measurements within Measurement Categories III or IV.

3

SC Express Considerations

This chapter details the clock and trigger functionality available through the PXI Express chassis. PXI clock and trigger signals are only available on NI PXI Express devices.

SC Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common low-skew 100 MHz reference clock for synchronization of multiple modules in a PXI Express measurement or control system. The PXIe backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXIe_SYNC100

PXIe_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_SYNC100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

On SC Express modules, the eight PXI trigger signals are synonymous with PXI_Trig <0..7>.

Note that in a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple devices or to share a common trigger signal among devices.

A Star Trigger controller can be installed in this system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a Star Trigger controller. PXI_STAR can be used as an external source for many AI, AO, and counter signals.

An SC Express module is not a Star Trigger controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXI_STAR Filters

You can enable a programmable debouncing filter on each PFI, PXI_Trig, PXIe_DSTAR, or PXI_STAR signal.

PXIe_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that create point-to-point, high-frequency connections between a PXI Express system timing module and a peripheral device. Using multiple connections enable you to create more applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

Table 3-1. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at www.pxisa.org.

Data Transfer Methods

The primary ways to transfer data across the PXI Express bus are as follows:

- Direct Memory Access (DMA)—DMA is a method to transfer data between the device and computer memory without the involvement of the CPU. This method makes DMA the fastest available data transfer method. NI uses DMA hardware and software technology to achieve high throughput rates and increase system utilization. DMA is the default method of data transfer for PCI Express and PXI Express devices.

- Programmed I/O—Programmed I/O is a data transfer mechanism where the user's program is responsible for transferring data. Each read or write call in the program initiates the transfer of data. Programmed I/O is typically used in software-timed (on-demand) operations.

A

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