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NI 5771R User Guide and Specifications

The NI 5771 is a high-speed digitizer adapter module designed to work in conjunction with your NI FlexRIO™ FPGA module. The NI 5771 features two analog input (AI) channels with 8-bit sample rates up to 1.5 GS/s when using both channels or 3 GS/s when using only one channel.

This document contains signal information and specifications for the NI 5771R, which is composed of an NI FlexRIO FPGA module and the NI 5771. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI 5771R.

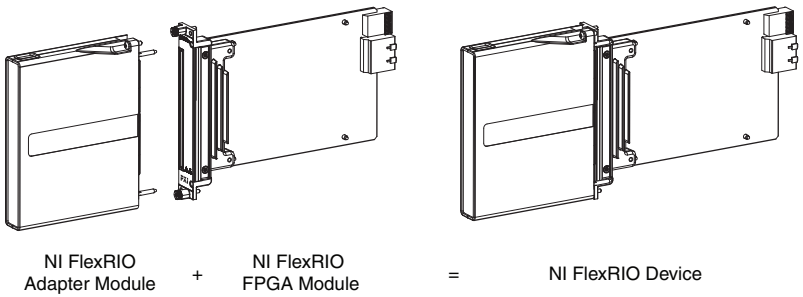
Note Before configuring your NI 5771R, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions.

Contents

NATIONAL INSTRUMENTS™

Figure 1 shows an example of a properly connected NI FlexRIO device.

Figure 1. NI FlexRIO Device



Note *NI 5771R* refers to the combination of your NI 5771 adapter module and your NI FlexRIO FPGA module. *NI 5771* refers to your NI 5771 adapter module only.

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) as stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in its intended operational electromagnetic environment.

This product is intended for use in industrial locations. There is no guarantee that harmful interference will not occur in a particular installation, when the product is connected to a test object, or if the product is used in residential areas. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels (National Instruments part number 778700-01) in adjacent chassis slots. For more information about installing PXI EMC filler panels in your system, refer to the *Appendix: Installing PXI EMC Filler Panels* section of this document.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution This product is sensitive to electrostatic discharge (ESD). To ensure the specified EMC performance, follow the programming instructions listed at the end of the *Using Your NI 5771R with a LabVIEW FPGA Example VI* and *Creating a LabVIEW Project and Running a VI on an FPGA Target* sections of this document.

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 to learn how to use your NI FlexRIO documentation set.

Figure 2. How to Use Your NI FlexRIO Documentation Set

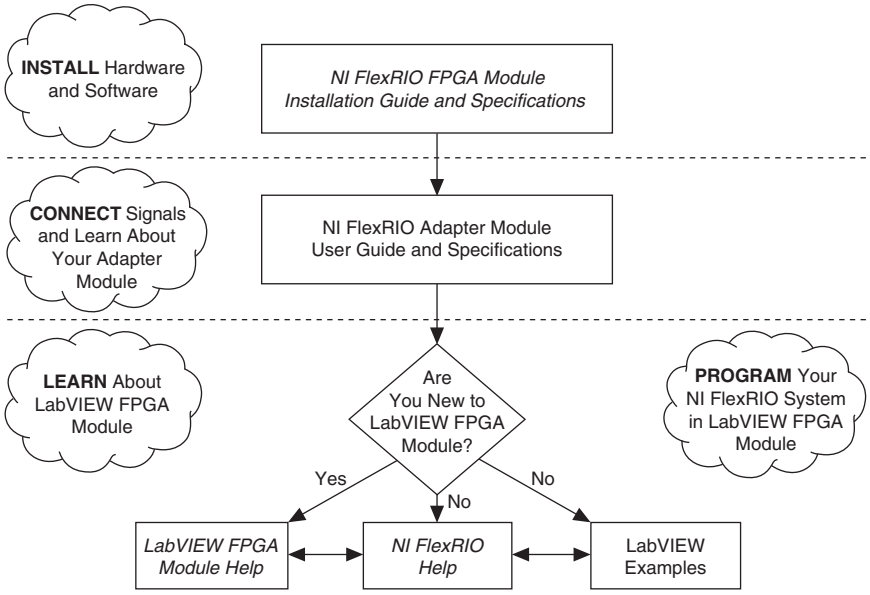


Table 1. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
NI FlexRIO FPGA Module Installation Guide and Specifications	Available in your FPGA module hardware kit, from the Start Menu, and at `ni.com/manuals`.	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
NI 5771R User Guide and Specifications	Available from the Start Menu and at `ni.com/manuals`.	Contains signal information, examples, and specifications for your adapter module.
LabVIEW FPGA Module Help	Embedded in *LabVIEW Help* and at `ni.com/manuals`.	Contains information about the basic functionality of LabVIEW FPGA Module.
NI FlexRIO Help	Available from the Start Menu and at `ni.com/manuals`.	Contains FPGA module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.

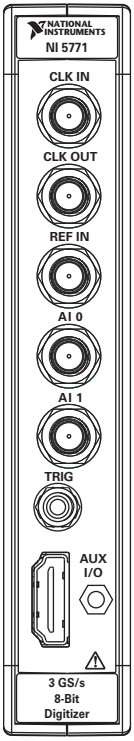
Front Panel and Connector Pinouts

Front Panel

Table 2 shows the front panel connector and signal descriptions for the NI 5771. Refer to the *Specifications* section of this document for additional signal information.

Caution To avoid permanent damage to the NI 5771, disconnect all signals connected to the NI 5771 before powering down the module, and connect signals only after the adapter module has been powered on by the NI FlexRIO FPGA module.

Table 2. NI 5771 Front Panel Connectors

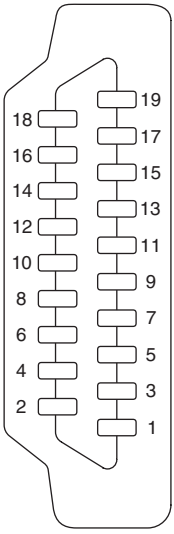
Device Front Panel	Connector	Signal Description
	CLK IN	External clock input, 50 Ω single-ended (SE).
	CLK OUT	Exported clock output.
	REF IN	Reference clock input, 50 Ω, SE.
	AI 0	Analog input channel 0, 50 Ω, SE.
	AI 1	Analog input channel 1, 50 Ω, SE.
	TRIG	Trigger input and output channel.
	AUX I/O	Refer to Table 3 for the signal list and descriptions.

Caution Connections that exceed any of the maximum ratings of any connector on the NI 5771R can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *Specifications* section of this document.

AUX I/O Connector

Table 3 shows the pin assignments for the AUX I/O connector on the NI 5771.

Table 3. NI 5771 AUX I/O Connector Pin Assignments

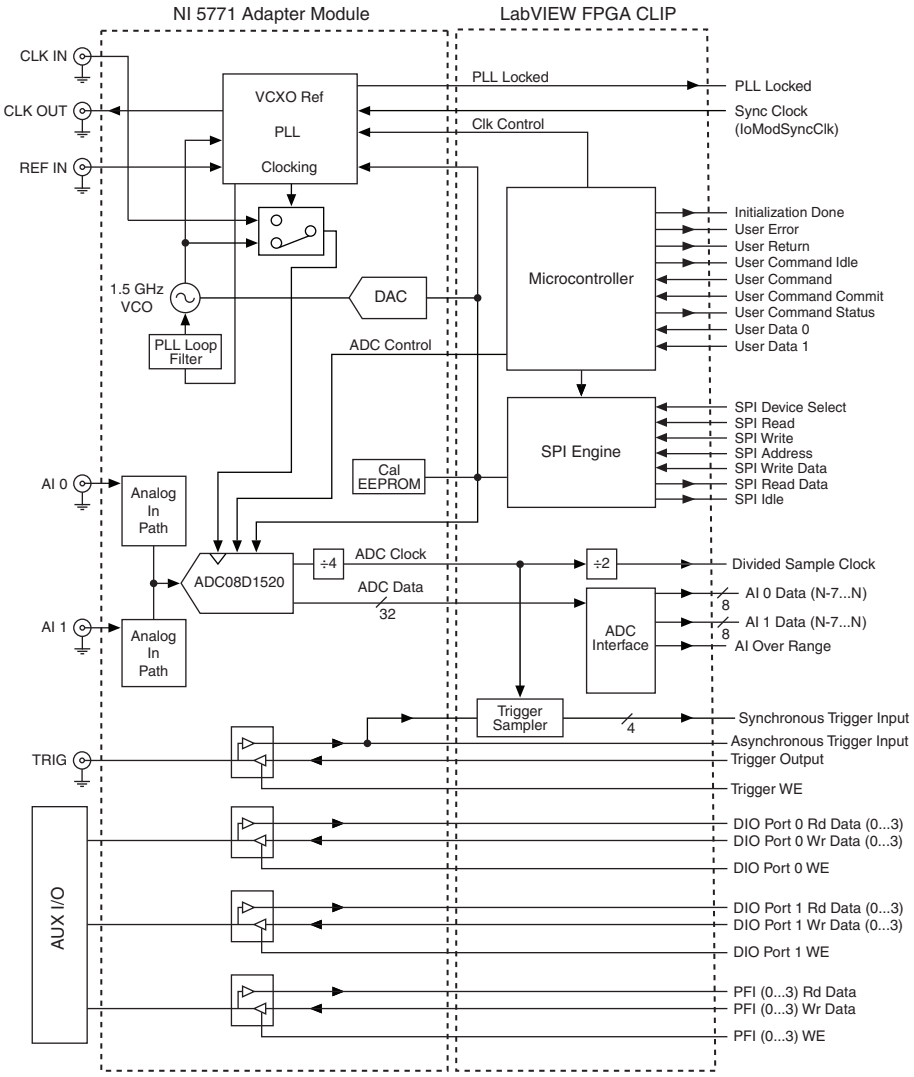
AUX I/O Connector	Pin	Signal	Signal Description
	1	DIO Port 0 (0)	Bidirectional single-ended (SE) digital I/O (DIO) data channel.
	2	GND	Ground reference for signals.
	3	DIO Port 0 (1)	Bidirectional SE DIO data channel.
	4	DIO Port 0 (2)	Bidirectional SE DIO data channel.
	5	GND	Ground reference for signals.
	6	DIO Port 0 (3)	Bidirectional SE DIO data channel.
	7	DIO Port 1 (0)	Bidirectional SE DIO data channel.
	8	GND	Ground reference for signals.
	9	DIO Port 1 (1)	Bidirectional SE DIO data channel.
	10	DIO Port 1 (2)	Bidirectional SE DIO data channel.
	11	GND	Ground reference for signals.
	12	DIO Port 1 (3)	Bidirectional SE DIO data channel.
	13	PFI 0	Bidirectional SE DIO data channel.
	14	NC	No connect.
	15	PFI 1	Bidirectional SE DIO data channel.
	16	PFI 2	Bidirectional SE DIO data channel.
	17	GND	Ground reference for signals.
	18	+5V	+5 V power (10 mA maximum).
	19	PFI 3	Bidirectional SE DIO data channel.

Caution The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do *not* connect the AUX I/O port on the NI 5771 into the HDMI port of another device. NI is *not* liable for any damage resulting from such signal connections.

Block Diagram

Figure 3 shows the NI 5771 block diagram and signal flow to and from the NI 5771 component-level intellectual property (CLIP) by way of the adapter module and the corresponding NI 5771 CLIP in LabVIEW FPGA.

Figure 3. NI 5771 Connector Signals and NI 5771 CLIP Signal Block Diagram



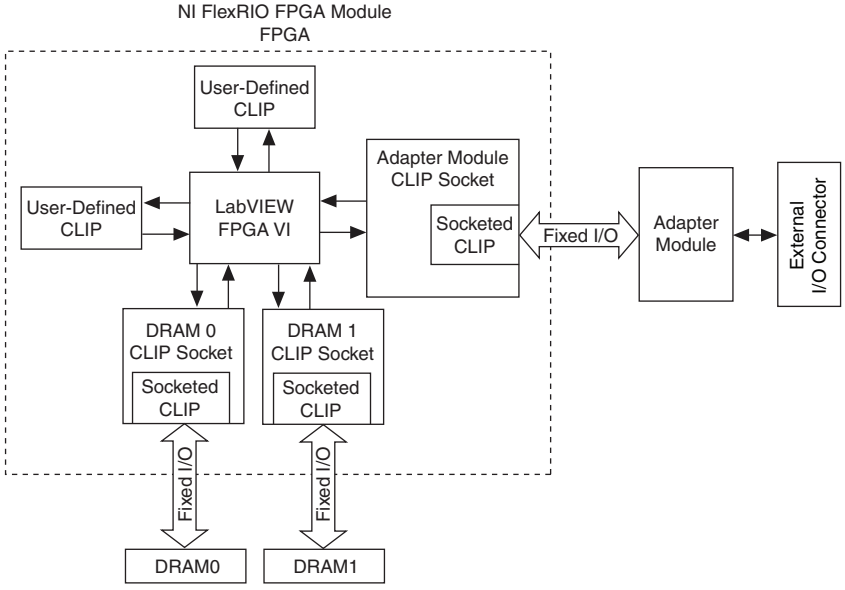
NI 5771 CLIP

The LabVIEW FPGA Module includes a feature for HDL IP integration called CLIP. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration functionality of the user-defined CLIP, but it also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 4 shows the relationship between an FPGA VI and CLIP.

Figure 4. CLIP and FPGA VI Relationship



The NI 5771 ships with a socketed CLIP item that adds module I/O to the LabVIEW project. The NI 5771 CLIP provides access to two analog input channels, eight bidirectional DIO channels, four bidirectional PFI channels, and an input clock selector that can be configured to use one of the following settings:

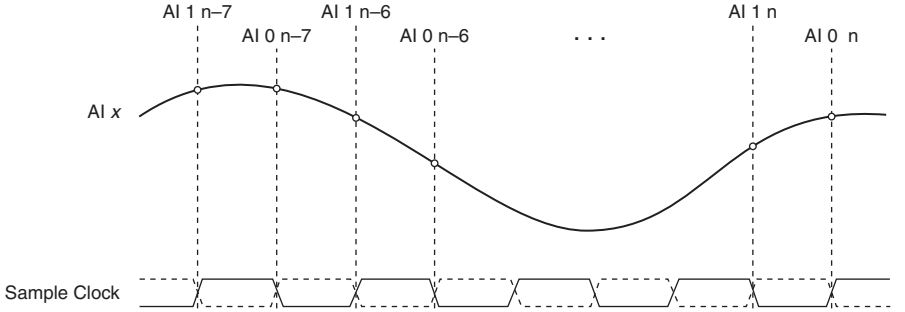
- Internal Sample clock
- Internal Sample clock locked to an external Reference clock through the REF IN connector
- External Sample clock received through the CLK IN connector
- Internal Sample clock locked to an external Reference clock through IoModSyncClock

This CLIP also contains an engine to program the ADC and clock circuit, either through predetermined settings for an easier instrument setup or through a raw SPI address and data signals for a more advanced setup. In the LabVIEW FPGA Module, 8-bit analog input data is accessed using a U8 data type. The DIO signals are grouped into two ports of four signals each and are accessed using a U8 data type and Boolean write enable signal. The four PFI signals are accessed individually using Booleans.

Although real-time sampling is the default sampling mode on the NI 5771, the NI 5771 CLIP also supports *Time Interleaved Sampling* (TIS) on one analog input channel at a time. TIS enables the device to use both channels on the ADC to sample the same waveform at different relative phases, which increases the real-time sample rate. The NI 5771 then interleaves the samples to create a waveform as if only one ADC channel were sampling the waveform at twice the Sample clock rate. To configure the NI 5771 for TIS mode using this CLIP, refer to the *NI FlexRIO Help*.

In TIS mode, the data is returned on both the AI 0 <N-7..N> and AI 1 <N-7..N> signals even though the device is only sampling the single AI channel that you selected with the User Data 1 signal. The first sample of data is always AI 1 N–7, regardless of the channel you are sampling. Figure 5 demonstrates TIS on an NI 5771 device:

Figure 5. TIS Data Returned on an NI 5771



Note The ADC data sheet refers to TIS as *Dual-Edge Sampling* (DES).

Refer to the *NI FlexRIO Help* for more information about NI FlexRIO CLIP items, configuring the NI 5771 with a socketed CLIP, and a list of available socketed CLIP signals.

Cables

This list describes which cables to use when connecting to the NI 5771 front panel connectors.

- Use a shielded 50 Ω coaxial cable less than 3 meters long with an SMB plug end to connect to the TRIG connector.
- Use a shielded 50 Ω coaxial cable less than 3 meters long with an SMA plug end to the other NI 5771 front panel connectors.
- Use the SHH19–H19–AUX cable (NI part number: 152629-0*x*) to connect to the digital I/O and PFI signals on the AUX I/O connector.

For more information about connecting I/O signals on your device, refer to the *Specifications* section of this document.

Clocking

The NI 5771 clocks control the sample rate and other timing functions on the device. Table 4 contains information about the possible NI 5771 clock resources.

Table 4. NI 5771 Clock Sources

Clock	Frequency*	Source Options
Internal Clock Locked to Internal Reference	1.5 GHz	The internal reference is free-running.
Internal Clock PLL On (IoModSyncClock)	1.5 GHz	The internal reference locks to PXI_CLK10 through IoModSyncClock, which is provided only through the backplane of NI PXIe-796*x* devices.
Internal Clock PLL On (CLK IN)	1.5 GHz	The internal reference locks to an external Reference clock (10 MHz), which is provided through the CLK IN front panel connector.
External Clock (CLK IN)	850 MHz to 1.5 GHz	An external Sample clock can be provided through the CLK IN front panel connector.

* You can use TIS to acquire data at rates up to 3 GS/s. To configure your device for TIS, set the **User Command** signal in the NI 5771 CLIP to `4`, set the **User Data 0** signal to `1`, and set the **User Data 1** signal to either `0` or `1`, depending on which AI channel you want to sample. Refer to the *NI FlexRIO Help* for more information about configuring your NI 5771 CLIP.

Note Do *not* connect an external Sample clock with a frequency greater than 1.5 GHz to the CLK IN front panel connector to acquire data at rates greater than 1.5 GS/s. Instead, use an external clock with a frequency between 850 MHz and 1.5 GHz and configure the CLIP to use TIS mode.

PLL settling time ..... 6 s. Refer to the NI FlexRIO Help for more information about settling time.

Using Your NI 5771R with a LabVIEW FPGA Example VI

Note You must install the software before running this example. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes a variety of example projects to help get you started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI 5771R. This example requires at least one SMA cable for connecting signals to your NI 5771R.

Note The examples available for your device are dependent on the version of the software and driver you are using. For more information about which software versions are compatible with your device, visit `ni.com/info` and enter `rdsoftwareversion` in the text field.

Each NI 5771R example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
- A VI that runs on Windows that interacts with the LabVIEW FPGA VI

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that acquires a waveform on CH 0 of the NI 5771.

1. Connect one end of an SMA cable to AI 0 on the front panel of the NI 5771 and the other end of the cable to your device under test (DUT).
2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO» IO Modules»NI 5771**.
5. Select **NI 5771 - Getting Started.lvproj**.
6. In the **Project Explorer** window, open **NI 5771 - Getting Started (Host).vi** under **My Computer**. The host VI opens. The Open FPGA VI Reference function in this VI uses the NI 7952R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7952R, complete the following steps to change to the FPGA VI to support your target.
   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the Open FPGA VI Reference (PXI-7952R) function and select **Configure Open FPGA VI Reference**.

c. In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button

d. In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.

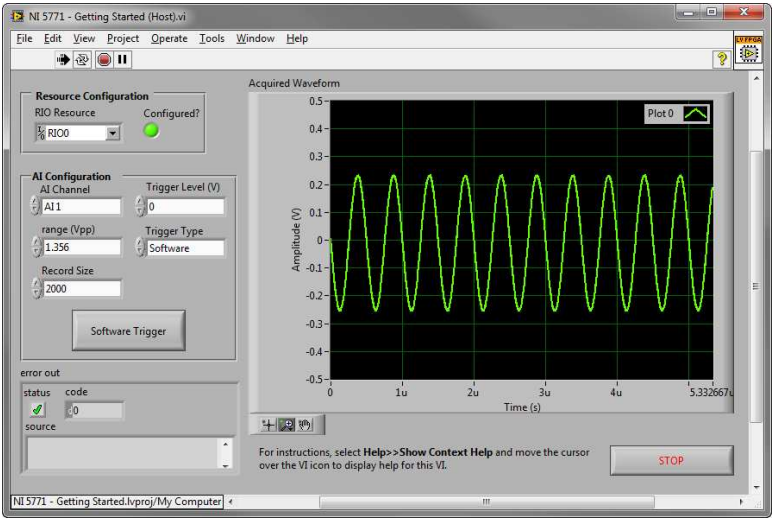
e. Click the **Select** button.

f. Click **OK** in the **Configure Open FPGA VI Reference** dialog box.

g. Save the VI.

7. On the front panel, in the **RIO Resource** pull-down menu, select an NI 5771R resource that corresponds with the target configured in step 6.
8. Select **AI 0** in the **AI Channel** control.
9. Set the **Trigger Level (V)** and the **Record Size** controls to the desired value.
10. In the **Trigger Type** control, you can select either **Software** or **Data Edge**. If you select **Software**, the VI acquires data every time you click the **Software Trigger** button on the front panel of the VI. If you select **Data Edge**, the VI acquires data every time an edge occurs.
11. Click the **Run** button to run the VI.
12. Click the **Software Trigger** button if you selected **Software Trigger** in the **Trigger Type** control. The VI acquires data and displays the captured waveform on the **Acquired Waveform** graph as shown in Figure 6.
13. Click the **STOP** button to stop the VI.
14. Close the VI.

Figure 6. NI 5771 - Getting Started (Host) VI Front Panel



Creating a LabVIEW Project and Running a VI on an FPGA Target

This section explains how to set up your target and create an FPGA VI and host VI for data communication. For more detailed information about acquiring data on your NI 5771R, refer to the device-specific examples available in NI Example Finder.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»Create Project**.
2. In the **Create Project** dialog box, select **FPGA Template** and click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `5771SampleAcq.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing Target or Device** button and expand **FPGA Target**. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the **Project Explorer** window.
4. In the **Project Explorer** window, expand **FPGA Target (RIO*x*, PXI-79*xx*R)**.
5. Right-click **FPGA Target (RIO*x*, PXI-79*xx*R)** and select **New»FPGA Base Clock**.
6. In the **Resource** pull-down menu, select **200 MHz Clock** and click **OK**.
7. Right-click **IO Module** in the **Project Explorer** window and select **Properties**.
8. Select the NI 5771 from the IO Module list. The available CLIP for the NI 5771 is displayed in the **General** category of the Component Level IP pane. If the information in the **General** category is dimmed, select the **Enable IO Module** checkbox.
9. Select **NI 5771 CLIP** in the Name list of the Component Level IP section.
10. In the **Clock Selections** category, select **200 MHz Clock** from the pull-down menu for **Clk200**. Leave **Clk40** configured as the **Top-Level Clock**. This step is necessary to compile the FPGA VI correctly.
11. Click **OK**.

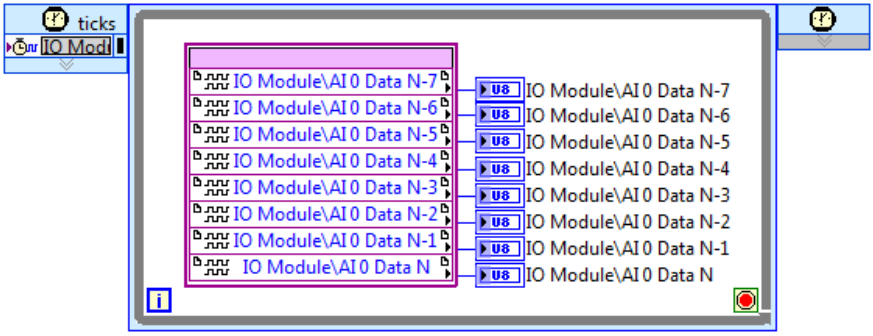
Note Configuring these clocks is required for proper CLIP operation. Refer to the NI 5771 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

12. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens.
13. Select **Window»Show Block Diagram** to open the VI block diagram.
14. In the **Project Explorer** window, expand the **IO Module (NI 5771 : NI 5771)** tree view.

15. Drag **AI 0 Data N–7** to the block diagram.
16. Click the handle on the bottom of the control node with the Positioning tool, and drag the edge down to expose the other signals, **AI 0 Data N–6...AI 0 Data N**.
17. Add a Timed Loop structure around the node.
18. Wire indicators to the output terminals of the **IO Module\AI 0 Data N–7...AI 0 Data N**.
19. Right-click the input node of the Timed Loop and select **Input Node.**
20. In the Input Node dialog box, click the **Select Timing Source** button and then choose **Divided Sample Clock**.

Your block diagram should now resemble the block diagram in Figure 7.

Figure 7. 5771SampleAcq (FPGA).vi Block Diagram



Tip Click the **Clean Up Diagram** button on the toolbar to cleanly organize the VI block diagrams.

21. Save the VI as `5771SampleAcq (FPGA).vi`.
22. Click the **Run** button. LabVIEW creates a default build specification and begins compiling the VI. The **Generating Intermediate Files** window opens and displays the code generation progress. Next, the **Compilation Status** window opens and displays the progress of the compilation. The compilation takes several minutes.
23. Click **Close** in the **Compilation Status** window.
24. Save and close the VI.
25. Save the project.

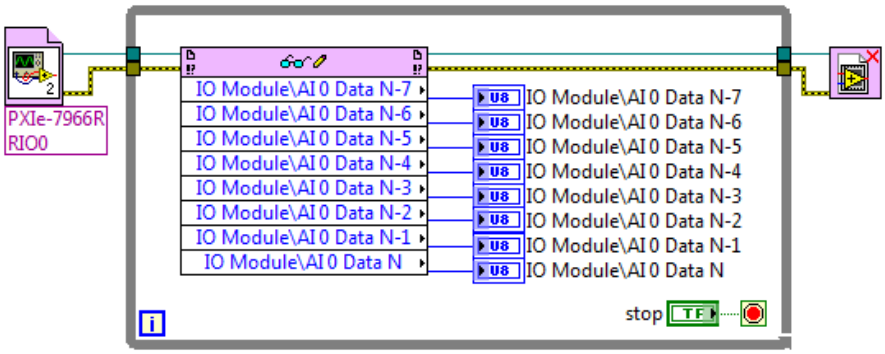
Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens.
2. Select **Window»Show Block Diagram** to open the VI block diagram.
3. Place the Open FPGA VI Reference function, located on the **FPGA Interface** palette, on the block diagram.

4. Right-click the Open FPGA VI Reference function and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** dialog box, select **VI** in the **Open** section.
6. In the **Select VI** dialog box that opens, select **5771SampleAcq (FPGA).vi** under your device and click **OK**.
7. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The target name appears under the Open FPGA VI Reference function in the block diagram.
8. Add a While Loop to the block diagram. Place it to the right of the Open FPGA VI Reference function.
9. Right-click the conditional terminal inside the While Loop and select **Create Control** to create a STOP button on the VI front panel window.
10. Add the Read/Write Control function, located on the **FPGA Interface** palette, inside the While Loop.
11. Wire the **FPGA VI Reference Out** output terminal of the Open FPGA VI Reference function to the **FPGA VI Reference In** input terminal on the Read/Write Control function.
12. Wire the **error out** terminal of the Open FPGA VI Reference function to the **error in** control of the Read/Write Control function.
13. Configure the Read/Write Control function by clicking the terminal section labeled **Unselected**, and selecting **IO Module/AI 0 Data N–7**.
14. Click the handle on the bottom of the control node with the Positioning tool and drag the edge down to add the other signals, **AI 0 Data N–6...AI 0 Data N**, to the Read/Write Control function.
15. Wire indicators to the output terminals of the IO Module\AI 0 Data N–7...AI 0 Data N.
16. Add the Close FPGA VI Reference function, located on the **FPGA Interface** palette, to the right of the While Loop on the block diagram.
17. Wire the **FPGA VI Reference Out** terminal of the Read/Write Control function to the **FPGA VI Reference In** terminal of the Close FPGA VI Reference function.
18. Wire the **error out** terminal of the Read/Write Control function to the **error in** terminal of the Close FPGA VI Reference function.

Your block diagram should now resemble the block diagram in Figure 8.

Figure 8. 5771SampleAcq(Host).vi Block Diagram



19. Save the VI as `5771SampleAcq(Host).vi`.

Running the Host VI

1. Connect one end of an SMA cable to AI 0 on the front panel of the NI 5771 and the other end of the cable to your DUT.
2. Open the front panel of `5771SampleAcq(Host).vi`.
3. Click the **Run** button to run the VI.
4. The VI acquires data from the DUT on **AI 0 Data N and AI 0 Data N-1**.
5. Click the **STOP** button on the front panel and close the VI.

Specifications

This section lists the specifications of the NI 5771 adapter module. Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at `ni.com/manuals`.

Caution To avoid permanent damage to the NI 5771, disconnect all signals connected to the NI 5771 before powering down the module, and only connect signals after the module has been powered on by the NI FlexRIO FPGA module.

Note All numeric specifications are typical unless otherwise noted. All graphs illustrate the performance of a representative module.

Typical values describe useful product performance that are not covered by warranty. Typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with a 85% confidence level, based on measurements taken during development or production.

Analog Input (AI 0 and AI 1)

General Characteristics

Number of channels ..... Two

Connector type ..... SMA

Input type ..... Simultaneously sampled, single-ended

Input impedance ..... 50 Ω, per connector

Input coupling ..... DC

Signal paths ..... Lattice filter

Digital data resolution ..... 8-bit, unsigned, binary data

ADC part number ..... ADC08D1520[1]

Absolute maximum voltage without damage ... 6.3 V_{pk-pk}

Typical Specifications

ADC DC offset ..... –11 mV ± 1.6 mV

Full–scale (FS) input ..... 1.35 V_{pk-pk}

Gain error ..... ±1.6% (at DC)

Average noise density

- nV/√Hz 64.8
- dBm/Hz 130.7
- dBFS/Hz 137.3

Note Average noise density was measured with the following setup conditions: 375 MHz, 262,144 samples, 7-term Blackman–Harris window, bin = 15.059 kHz, 0 dBFS = 6.62 dBm into 50 Ω. (Full scale = 1.35 V_{pk-pk}).

Passband (DC-coupling, real-time sampling mode)

- Low cut-off frequency (–3 dB) ..... 0 Hz
- High cut-off frequency (–3 dB) ..... 900 MHz

Signal–to–noise ratio (SNR)[2] ..... 46.2 dB

Total harmonic distortion (THD)[1] ..... –55.2 dBc

Spurious-free dynamic range (SFDR)[1] ..... 56.4 dBc

Frequency–adjusted DAC range ..... ±110 ppm

Sample rate ..... 1.5 GHz

---

[1] For additional information about the ADC in your NI 5771, use the listed part number to locate the appropriate Texas Instruments data sheet at `www.ti.com`.

[2] Measured at –1 dBFS with an input frequency of 175 MHz.

Measurements

Frequency Response[1]

Figure 9. Low Frequency Response (Average of Multiple Channels)

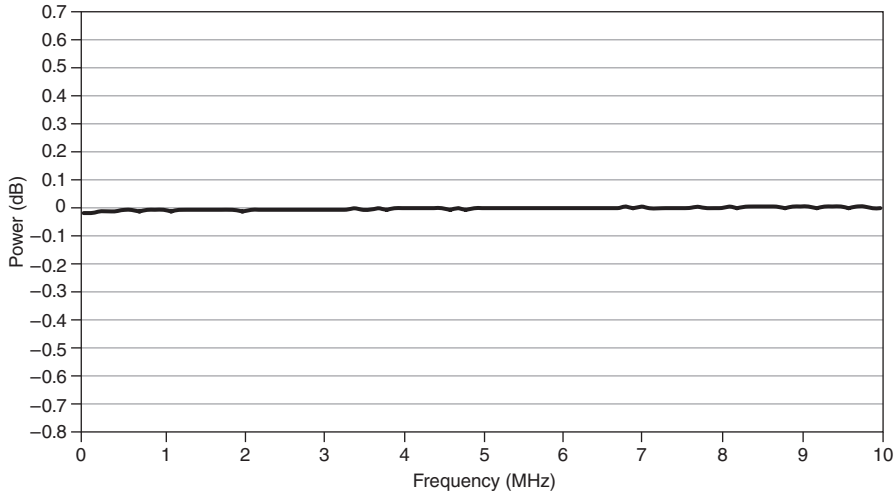
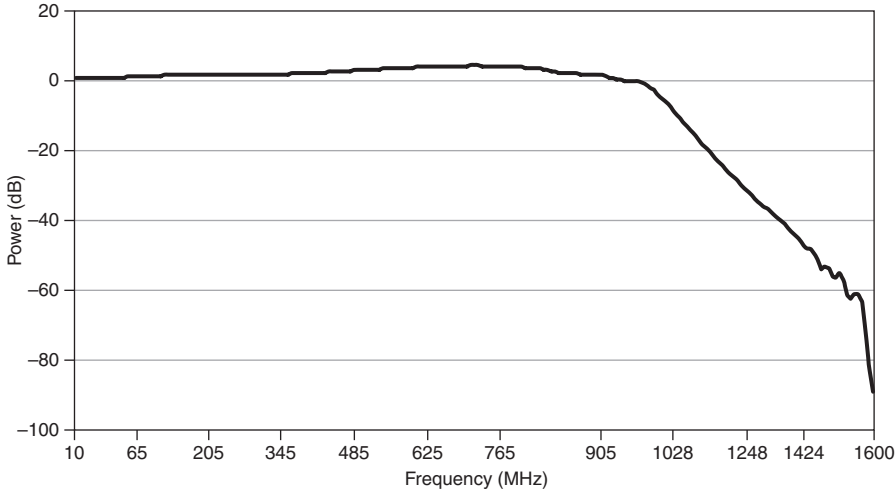
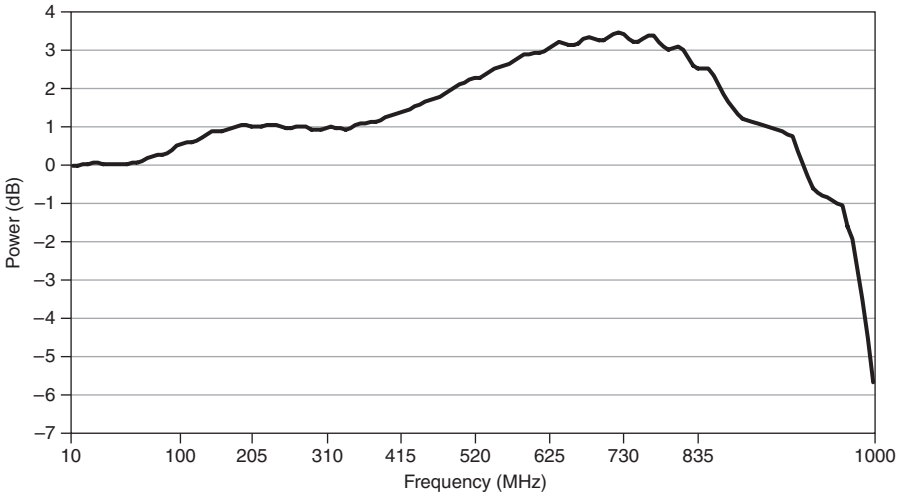


Figure 10. Frequency Response (Average of Multiple Channels)



[1] Reference at 10 MHz.

Figure 11. Frequency Response, +4 dB to –6 dB (Average of Multiple Channels)



Spectral Measurements

Figure 12. Low Power Source Spectral Measurements
(262,144 Point FFT, 10 Average RMS, –1 dBFS, 175 MHz)

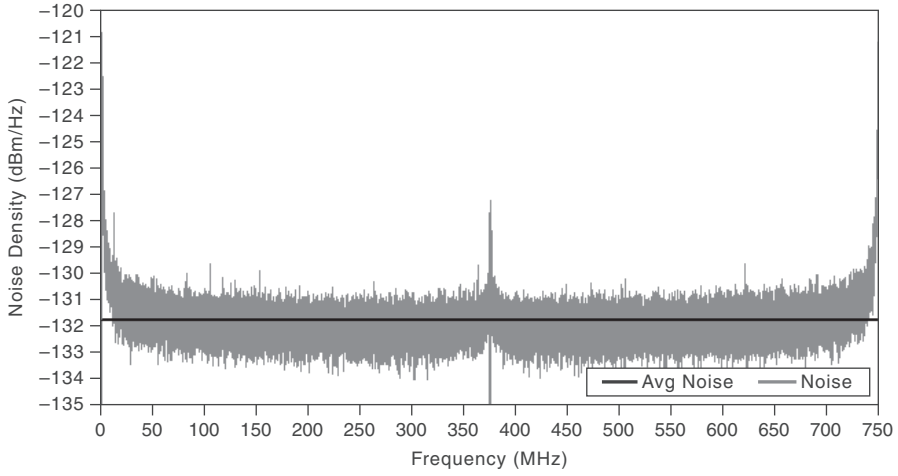
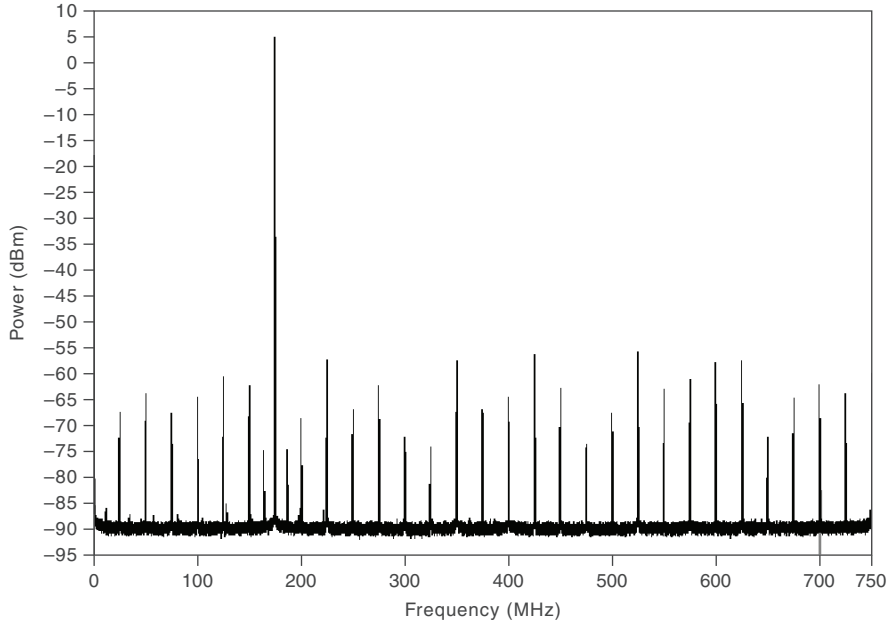


Figure 13. Spectral Measurements
(131,072 Point FFT, 10 Average RMS, –1 dBFS, 175 MHz)



Analog Input Total Phase Noise

Figure 14. AI Phase Noise (100 MHz Input, PLL Locked to PXI_CLK10,
1.2 pS RMS Jitter, –1 dBFS)

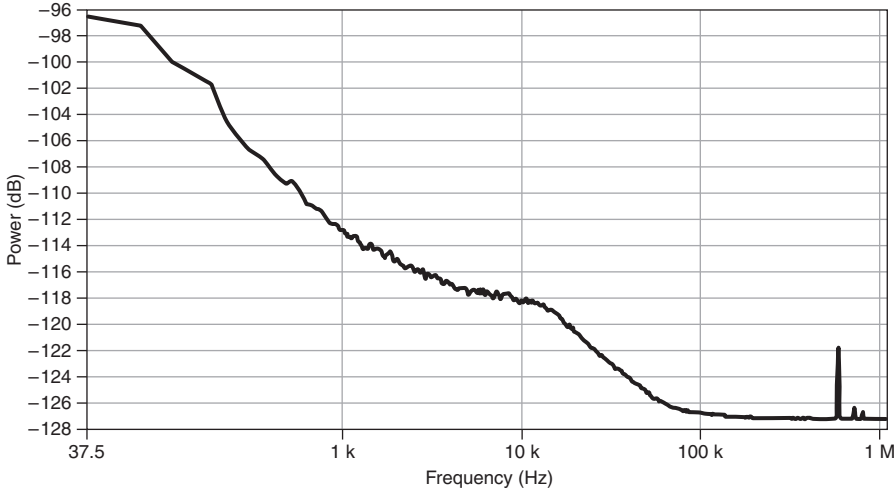


Table 5. Analog Input Total Phase Noise

Offset Frequency	Phase Noise (dBc/Hz)
100 Hz	–98.9
1 kHz	–112.8
10 kHz	–118.2
100 kHz	–126.9
1 MHz	–127.3

Internal Sample Clock

General Characteristics

Oscillator type ..... VCXO

Frequency ..... 1.5 GHz

Phase noise ..... Refer to the *Analog Input Total Phase Noise*

Typical Specifications

Frequency stability

Temperature ..... ±30 ppm over the operating temperature range

Aging ..... ±5 ppm per year

CLK IN

General Characteristics

Number of channels ..... 1, single-ended

Connector type ..... SMA

Input impedance ..... 50 Ω

Input coupling ..... DC

Input voltage range ..... 0.9 V_{pk-pk} to 3.5 V_{pk-pk}

Absolute maximum voltage without damage ... 10 V_{pk-pk}

Duty cycle ..... 45% to 55%

CLK OUT

General Characteristics

Number of channels ..... 1, single-ended

Connector type ..... SMA

Output impedance ..... 50 Ω

Output coupling ..... AC

Output voltage range ..... 0.9 V_{pk-pk} to 3.5 V_{pk-pk}

Absolute maximum input without damage ..... 10 V_{pk-pk}

Duty cycle ..... 45% to 55%

REF IN

General Characteristics

Number of channels ..... 1, single-ended

Connector type ..... SMA

Frequency ..... 10 MHz

Input impedance ..... 50 Ω

Input coupling ..... DC

Input voltage range ..... 0.9 V_{pk-pk} to 3.5 V_{pk-pk}

Absolute maximum voltage without damage ... 10 V_{pk-pk}

Duty cycle ..... 40% to 60%

TRIG

General Characteristics

Number of channels ..... 1, single-ended

Connector type ..... SMB

Input impedance ..... 50 Ω

Coupling ..... DC

Interface logic

- V_{IL} ..... 0.9 V_{pk-pk}
- V_{IH} ..... 3.5 V_{pk-pk}
- V_{OL} ..... 0.55 V
- V_{OH} ..... 2.40 V

Absolute maximum voltage without damage ... 10 V_{pk-pk}

Maximum retrigger rate ..... 140 MHz

AUX I/O (Port 0 DIO <0..3>, Port 1 DIO <0..3>, and PFI <0..3>)

General Characteristics

Number of channels ..... 12, bidirectional (8 DIO and 4 PFI)

Connector type ..... HDMI

Interface standard ..... 3.3 V LVCMOS

Interface logic

- Maximum V_{IL} ..... 0.8 V
- Minimum V_{IH} ..... 2.0 V
- Maximum V_{OL} ..... 0.4 V
- Minimum V_{OH} ..... 2.7 V
- Maximum V_{OH} ..... 3.6 V
- Z_{out} ..... 50 Ω ±20%
- I_{out} (DC) ..... ±2 mA

Pull-down resistor ..... 150 kΩ

Recommended operating voltage ..... –0.3 V to 3.6 V

Overvoltage protection ..... ±10 V

Maximum toggle frequency ..... 6.6 MHz

+5 V maximum current ..... 10 mA

+5 V voltage tolerance ..... 4 V to 5 V

Identification EEPROM Map

Byte Address	Size (Bytes)	Field Name
0x0	2	Vendor ID
0x2	2	Product ID
0x4	4	Serial Number
0x8	116	Reserved
0x7C	132	User Space

Caution *Only* write to *User Space*. Writing to any other offset may cause the NI 5771 to stop functioning.

Calibration EEPROM Map

Byte Address	Size (Bytes)	Field Name
0x0C	56	Reserved

Power

Total power, typical operation ..... 5.3 W

Physical

Dimensions ..... 12.9 × 2.0 × 12.1 cm
(5.1 × 0.8 × 4.7 in.)

Weight ..... 413 g (14.6 oz)

Front panel connectors ..... 5 SMA, one SMB, and one HDMI connector

Environmental

Maximum altitude ..... 2,000 m (at 25 °C ambient temperature).

Pollution Degree 2

Indoor use only.

Operating Environment

Ambient temperature range[1] ..... 0 °C to 55 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range ..... 10% to 90%, noncondensing (tested in accordance with IEC-60068-2-56.)

Storage Environment

Ambient temperature range ..... –20 °C to 70 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range ..... 5% to 95%, noncondensing,
tested in accordance with IEC-60068-2-56.

Operational shock ..... 30 g peak, half-sine, 11 ms pulse,
tested in accordance with IEC-60068-2-27.
Test profile developed in accordance with MIL-PRF-28800F.

[1] For PXI/PXI Express chassis configurations that group NI FlexRIO adapter modules in three or more contiguous slots, National Instruments recommends limiting the ambient operating temperature to less than 50 °C.

Random vibration

Operating ..... 5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating ..... 5 Hz to 500 Hz, 2.4 g_{rms}, tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For EMC declarations and certifications, refer to the *Online Product Certification* section of this document.

Caution For EMC compliance, operate this device with shielded cables and accessories.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At `ni.com/support` you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at `ni.com/support` and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

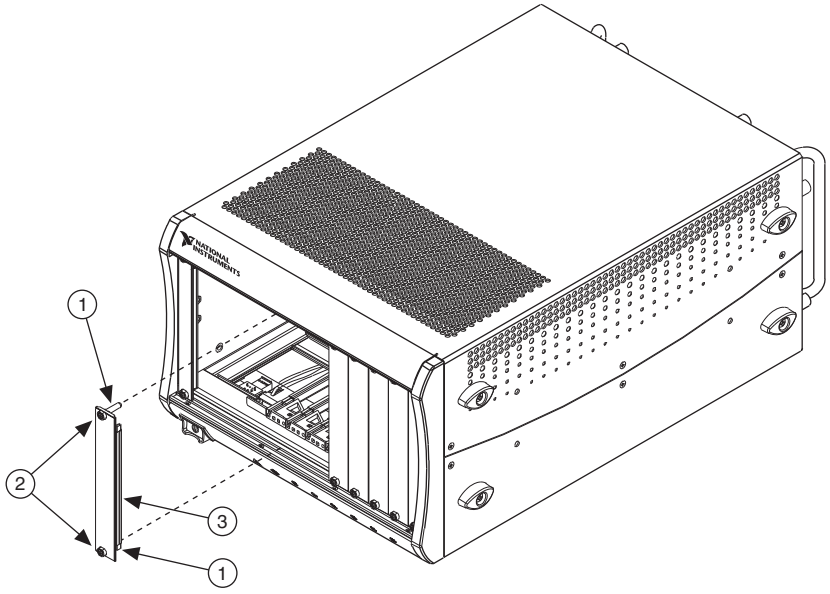
Appendix: Installing PXI EMC Filler Panels

To ensure specified EMC performance, PXI EMC filler panels must be properly installed in your NI FlexRIO system. The PXI EMC filler panels (National Instruments part number 778700-01) must be purchased separately. For more installation information, refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications*.

Complete the following steps to install PXI EMC filler panels in your PXI chassis:

1. Remove the captive screw covers.
2. Install the PXI EMC filler panels by securing the captive mounting screws to the chassis, as shown in Figure 15. Make sure that the EMC gasket is on the right side of the PXI EMC filler panel.

Figure 15. PXI EMC Filler Panels and Chassis



1	Captive Screw Covers	2	Captive Mounting Screws	3	EMC Gasket

Note You must populate all slots with a module or a PXI EMC filler panel to ensure proper module cooling. Do not overtighten screws (2.5 lb-in. maximum). For additional information about the use of PXI EMC filler panels in your PXI system, visit `ni.com/info` and enter `emcpanels`.

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