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Board Assembly Part Number(s)

Part Number	Description
156502A-11L or later	**cRIO-9030**
156502A-01L or later	**cRIO-9031**
156502A-02L or later	**cRIO-9033**
156502A-03L or later	**cRIO-9034**
157732A-11L or later	**cRIO-9035**
157732A-01L or later	**cRIO-9036**
157732A-02L or later	**cRIO-9038**
157732A-03L or later	**cRIO-9039**

Manufacturer: National Instruments

Volatile Memory

Type[1]	Size	User Accessible/ System Accessible[2]	Battery Backup?	Purpose	Method of Clearing[3]
(9030)					
DDR3-SDRAM	*1 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K70T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9031)					
DDR3-SDRAM	*1 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K70T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9033)					
DDR3-SDRAM	*2 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K160T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9034)					
DDR3-SDRAM	*2 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K325T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
FPGA DRAM	*128 MB*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9035)					
DDR3-SDRAM	*1 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K70T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9036)					
DDR3-SDRAM	*1 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K70T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*

[1] Calibration constants that are stored in device EEPROMs include information for the device's full operating range. Calibration constants do not maintain any unique data for specific configurations at which the device is used unless otherwise specified.

[2] Items are designated **No** for the following reason(s):
a) Hardware changes or a unique software tool from National Instruments are required to modify contents of the memory listed.
b) Hardware-modifying software tools are not distributed to customers for any personal access or customization, also known as non-normal use.

[3] The designation *None Available to User* indicates that the ability to clear this memory is not available to the user under normal operation. The utilities required to clear the memory are not distributed by National Instruments to customers for normal use.

(9038)					
DDR3-SDRAM	*2 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K160T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9039)					
DDR3-SDRAM	*2 GB*	*Yes/Yes*	*No*	*System Memory*	*Cycle Power*
FPGA RAM	*Kintex-7 7K325T*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
FPGA DRAM	*128 MB*	*Yes/Yes*	*No*	*LabVIEW and User Data*	*Cycle Power*
(9030/9031/9033/9034/9035/9036/9038/9039)					
CPLD-SDRAM	*51 Mb*	*No/Yes*	*No*	*CPLD Memory*	*Cycle Power*
SoC RTC RAM	*242Bytes*	*Yes/Yes*	*Yes*	*Battery Backed portion of RTC*	*CMOS reset button*

Non-Volatile Memory

Type	Size	User Accessible/ System Accessible	Battery Backup?	Purpose	Method of Clearing
(9030)					
Disk-on-Chip	*4 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*32 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*
(9031)					
Disk-on-Chip	*4 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*32 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*
(9033)					
Disk-on-Chip	*8 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*64 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*

(9034)

Disk-on-Chip	*16 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*128 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*

(9035)

Disk-on-Chip	*4 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*32 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*

(9036)

Disk-on-Chip	*4 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*32 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*

(9038)

Disk-on-Chip	*8 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*64 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*

(9039)

Disk-on-Chip	*16 GB*				
-Firmware		*No/Yes*	*No*	*Safemode*	*None available to user*
-OS		*No/Yes*	*No*	*Operating System*	*Format drive in MAX*
-User Disk		*Yes/Yes*	*No*	*User Data*	*Format drive in MAX*
Flash	*128 Mb*				
-Firmware		*No/Yes*	*No*	*FPGA Firmware*	*None available to user*
-FPGA Bitstream		*Yes/Yes*	*No*	*User LV FPGA VI Bitstream*	*NI-RIO Device Setup*

(9030/9031/9033/9034/9035/9036/9038/9039)

CPLD	*0.47 Mb*	*No/Yes*	*No*	*General Logic*	*None available to user*
Ethernet NVM	*8 Mb*	*No/Yes*	*No*	*Firmware*	*None available to user*
SPD EEPROM	*256 bytes*	*No/Yes*	*No*	*Describes DDR3L memory*	*None available to user*
System BIOS	*8 MB*	*No/Yes*	*No*	*BIOS firmware*	*BIOS update process*

Media Storage

Type	Size	User Accessible/ System Accessible	Battery Backup?	Purpose	Method of Clearing

NONE

Clearing Notes:

CMOS reset button: To clear the CMOS follow the steps below:

1. Disconnect power from the cRIO controller.
2. Locate the CMOS reset button in the center of the cRIO backplane.
3. Press the CMOS reset button and hold it for 1 second.

Format drive in MAX: To format the drive in MAX, follow the steps below:

1. Open NI Measurement & Automation Explorer (MAX).
2. On the left pane, expand *Remote Systems* and select your cRIO.
3. Right-click on the cRIO and select *Format Disk*.
4. Ensure *Reset all of the network adapters to their default settings* is selected.
5. Click the *Format* button.

NI-RIO Device Setup: To erase the bitfile from the flash follow the steps below:

1. Add the cRIO Target to your LabVIEW project by right-clicking on the project and selecting New » Targets and Devices and selecting your cRIO.
2. Right-click on the FPGA project item and select RIO Device Setup.
3. In the *Advanced* section, select *Erase Bitfile on Flash*.

BIOS update process: In order to update the BIOS, please contact NI by emailing support@ni.com or calling 866-275-6964.

Terms and Definitions

User Accessible Allows the user to directly write or modify the contents of the memory during normal instrument operation.

System Accessible Does not allow the user to access or modify the memory during normal instrument operation. However, system accessible memory may be accessed or modified by background processes. This can be something that is not deliberate by the user and can be a background driver implementation, such as storing application information in RAM to increase speed of use.

Cycle Power The process of completely removing power from the device and its components. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory Requires power to maintain the stored information. When power is removed from this memory, its contents are lost.

Non-Volatile Retains its contents when power is removed. This type of memory typically contains calibration or chip configuration information, such as power up states.