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Manufacturer: National Instruments

Board Assembly Part Numbers (Refer to Procedure 1 for identification procedure):

Part Number and Revision	Description
156502A-01L or later	**cRIO-9031**

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
System Memory	DDR3-SDRAM	1 GB	No	Yes	Yes	Cycle Power
LabVIEW and User Data	FPGA RAM	Kintex-7 7K70T	No	Yes	Yes	Cycle Power
CPLD Memory	CPLD-SDRAM	51 Mb	No	No	Yes	Cycle Power
Real-Time Clock Data	SoC RTC RAM	242 Bytes	Yes	Yes	Yes	Procedure 2

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Primary storage	Disk-on-Chip	4 GB	No			
• Safemode				No	Yes	None
• Operating System				No	Yes	Procedure 3
• User Data				Yes	Yes	Procedure 3
FPGA storage	FLASH	32 Mb	No			
• FPGA Firmware				No	Yes	None
• User FPGA VI Bitstream				Yes	Yes	Procedure 4
General Logic	CPLD	0.47 Mb	No	No	Yes	None
Firmware	Ethernet NVM	8 Mb	No	No	Yes	None
Describes DDR3L memory	SPD EEPROM	256 bytes	No	No	Yes	None
BIOS firmware	FLASH	8 MB	No	No	Yes	None

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

Procedures

Procedure 1 – Board Assembly Part Number identification:
To determine the Board Assembly Part Number and Revision, check the top left corner of the white label on the bottom of the module (15xxxx<REV>-xxL).

Procedure 2 – SoC RTC RAM (Real-Time Clock Data):
The battery-backed Real-Time Clock data can be cleared from the SoC RTC RAM using the CMOS reset button. To clear the Real-Time Clock data, perform the following steps:

1. Disconnect power form the cRIO controller.
2. Locate the CMOS reset button in the center of the cRIO backplane.
3. Press the CMOS reset button and hold it from 1 second.

Procedure 3 – Primary Storage Disk-on-Chip (OS and User Data):
The Primary Storage DoC can be reformatted to clear the OS and User Data areas. The format operation is a "quick format" that re-initializes the file table, thereby making the existing files inaccessible. Format the drive for this NI Linux Real-Time target by performing one of the following steps:

1. Right-click the controller in MAX and click on "Format Drive".
2. Issue the nisystemformat command via a serial console local connection or SSH remote connection. Visit ni.com/info and enter the info code *format* for details.
3. Write a .VI that invokes the Format VI using the System Configuration API for the controller.

Procedure 4 – FPGA Storage Flash (User FPGA Bitstream):
The User FPGA Bitstream in the FPGA Storage Flash can be cleared using NI-RIO Device Setup. To clear the bitstream from the flash, perform the following steps:

1. Add the cRIO target to your LabVIEW project by right-clicking on the project and selecting New » Targets and Devices and selecting your cRIO.
2. Right-click on the FPGA project item and select RIO Device Setup.
3. In the *Advanced* section, select *Erase Bitfile on Flash*.

Terms and Definitions

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or write addressable from the host without the need to physically alter the product.

Clearing:
Per *NIST Special Publication 800-88 Revision 1*, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization:
Per *NIST Special Publication 800-88 Revision 1*, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.