SC Express

NI PXIe-4304/4305 User Manual

32 Ch, 24-bit, ±42 V, 5 kS/s or 51.2 kS/s Simultaneous Filtered Data Acquisition Module

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1 Getting Started

The NI PXIe-4304/4305 provides 32 simultaneously sampled filtered analog input channels. The PXIe-4304 can operate at sample rates up to 5 kS/s/ch and the PXIe-4305 can operate at sample rates up to 51.2 kS/s/ch. These modules can measure an analog voltage up to 42 V when using the TB-4304. Each channel has a 24-bit ADC and selectable digital filters to reject out-of-band noise.

Installation

Refer to the *PXIe-4304/4305 and TB-4304 User Guide and Terminal Block Specifications* document for step-by-step software and hardware installation instructions.

Note For a complete list of terminal blocks supported by a specific release of NI-DAQmx, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Module Specifications

Refer to the *PXIe-4304/4305 Specifications* document for module specifications.

Module Accessories

Refer to `ni.com/scexpress` for information about and a complete listing of supported accessories.

2

Using the Module

This chapter describes how to connect voltage input signals to the PXIe-4304/4305. It also provides the I/O connector signal pin assignments of the modules.

Driver support for the PXIe-4304/4305 was first available in NI-DAQmx 15.1.1. For the list of devices supported by a specific release, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Connecting Voltage Signals

This section provides information regarding connecting voltage signals.

Caution To ensure the specified EMC performance, operate this product only with shielded, twisted pair cables, and shielded accessories.

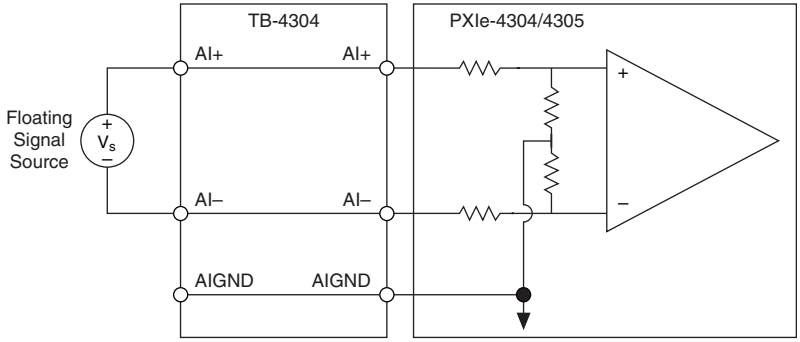
Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 30 m (100 ft.).

Connecting Floating Signal Sources

A floating signal source is not connected to the building ground system, but has an isolated ground-reference point through the ground of the device. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolators, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source.

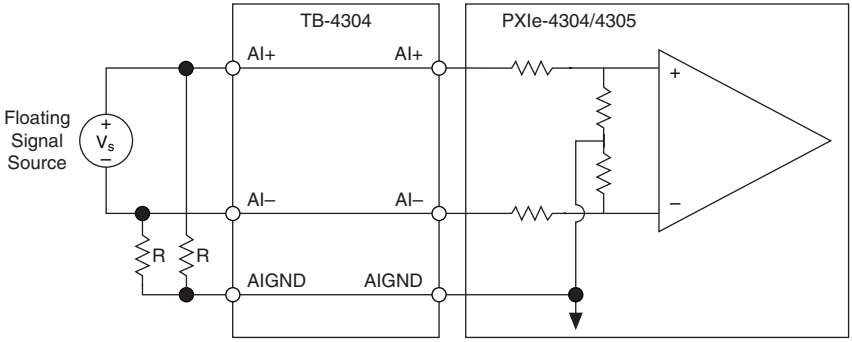
Refer to Figure 2-1 to connect the floating signal source to the TB-4304. Connect the positive terminal of the floating source to the AI+. Connect the negative terminal of the floating source to the AI-. The PXIe-4304/4305 input attenuators provide a ground reference for floating signal sources; therefore, external grounding bias resistor are not necessary.

Figure 2-1. Connecting Floating Signal Sources without External Bias Resistors



Between AIGND and each AI terminal, there is 575 kΩ resistance that is susceptible to electrically coupled noise. You can put the extra balanced bias resistors between AI terminals and AIGND to reduce the input impedance and improve the immunity to electrically coupled noise. Refer to Figure 2-2 to connect the floating signal source to the TB-4304 with the extra balanced bias resistors.

Figure 2-2. Connecting Floating Signal Sources with External Bias Resistors

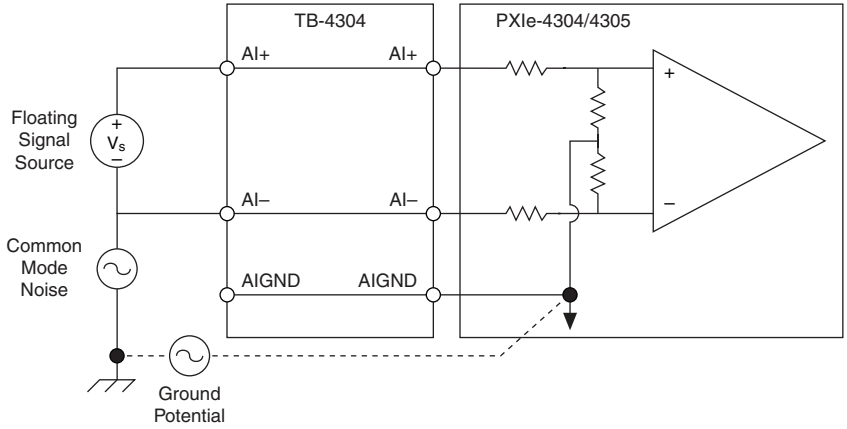


The disadvantage of extra balanced bias resistors is that it loads the source down with the series combination of the two resistors. For example, if the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produces an extra -1% gain error.

Connecting Ground-Referenced Voltage Signal Sources

A ground-referenced signal source is a signal source connected to a common-ground point with respect to the measurement device. Figure 2-3 shows how to connect a ground-referenced signal source to the PXIe-4304/4305 using a TB-4304.

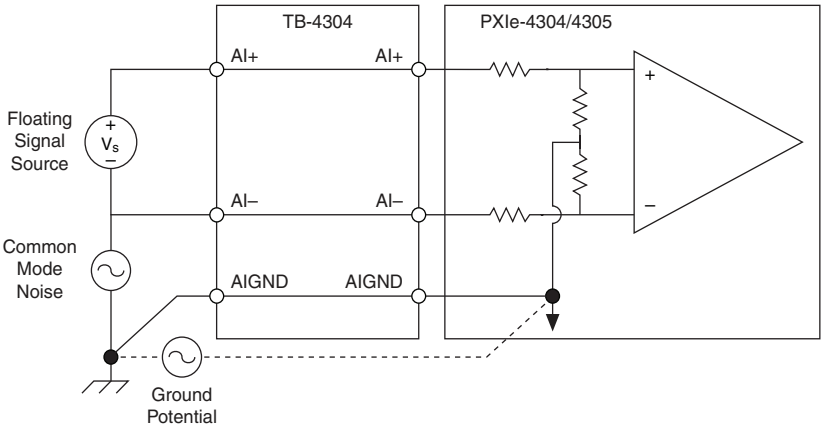
Figure 2-3. Connecting Ground-Referenced Signal Sources without an Extra Ground Connection



In this configuration the common-mode noise and ground potential will appear at the differential input of the instrument and create an unwanted common-mode voltage to the differential front end of the PXIe-4304/4305. The common-mode voltage related measurement error will be reduced by the common-mode rejection (CMRR) of the differential amplifier of the instrument. Refer to the *NI PXIe-4304/4305 Specifications* for CMRR specifications.

The difference in ground potential between two instruments connected to the same building power system is typically between 1 mV and 100 mV, or even higher. Connecting the ground reference of the signal source to the AIGND helps reduce the ground potential and the measurement error related to it. Refer to Figure 2-4 to connect the ground reference of the signal source to AIGND.

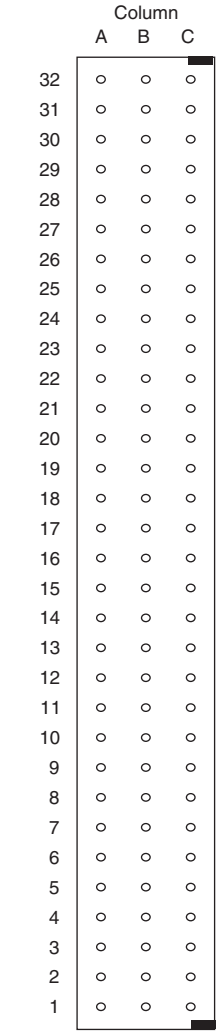
Figure 2-4. Connecting Ground-Referenced Signal Sources with an Extra Ground Connection



Module Pinout

Table 2-1 shows the pinout of the front connector of the PXIe-4304/4305. Refer to the *I/O Connector Signal Descriptions* section for definitions of each signal. Refer to the *PXIe-4304/4305 and TB-4304 User Guide and Terminal Block Specifications* for signal locations on the terminal blocks.

Table 2-1. Front Connector Signal Pin Assignments

Front Connector Diagram	Row Number	Column A	Column B	Column C
	32	AIGND	AI0+	AI1+
	31	AI2+	AI0-	AI1-
	30	AI2-	AI3-	AI3+
	29	AIGND	AI4+	AI5+
	28	AI6+	AI4-	AI5-
	27	AI6-	AI7-	AI7+
	26	AIGND	AI8+	AI9+
	25	AI10+	AI8-	AI9-
	24	AI10-	AI11-	AI11+
	23	AIGND	AI12+	AI13+
	22	AI14+	AI12-	AI13-
	21	AI14-	AI15-	AI15+
	20	AIGND	AI16+	AI17+
	19	AI18+	AI16-	AI17-
	18	AI18-	AI19-	AI19+
	17	AIGND	AI20+	AI21+
	16	AI22+	AI20-	AI21-
	15	AI22-	AI23-	AI23+
	14	AIGND	AI24+	AI25+
	13	AI26+	AI24-	AI25-
	12	AI26-	AI27-	AI27+
	11	AIGND	AI28+	AI29+
	10	AI30+	AI28-	AI29-
	9	AI30-	AI31-	AI31+
	8	AIGND	NC	NC
	7	NC	NC	NC
	6	NC	NC	NC
	5	PFI0	RSVD	RSVD
	4	RSVD	RSVD	RSVD
	3	RSVD	RSVD	RSVD
RSVD is reserved NC is no connection	2	RSVD	DGND	RSVD
	1	RSVD	RSVD	RSVD

I/O Connector Signal Descriptions

Table 2-2 describes the signals found on the I/O connector.

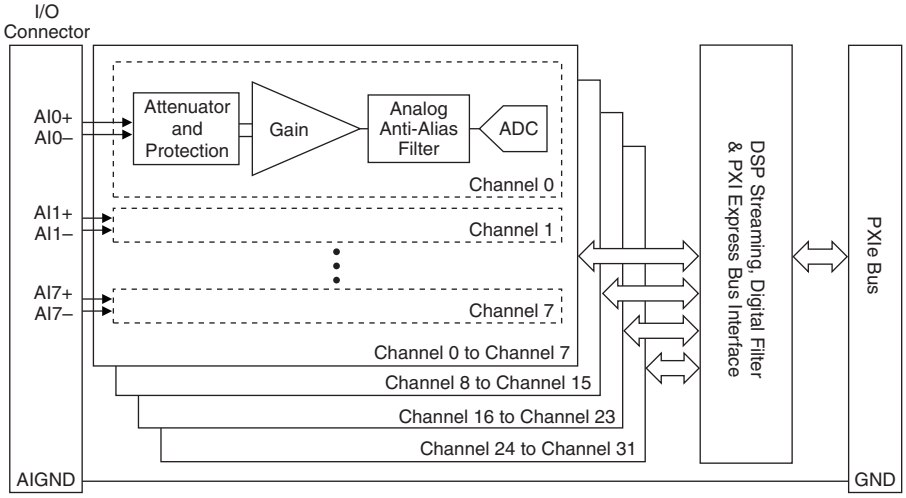
Table 2-2. I/O Connector Signal Descriptions

Signal Names	Direction	Description
AIGND	—	Analog Input Ground
AI<0..31>+	Input	Positive inputs of the differential analog input channels 0 to 31.
AI<0..31>-	Input	Negative inputs of the differential analog input channels 0 to 31.
RSVD	—	These pins are reserved for communication with the accessory.
DGND	—	Digital ground—this pin supplies the reference for module digital signals and is connected to the module digital ground.
PFI0	Input or Output	3.3 V digital signal for sending or receiving trigger and synchronization signals. This line is referenced to DGND.

PXIe-4304/4305 Block Diagram

Figure 2-5 shows the block diagram of the PXIe-4304/4305. The analog signal conditioning for each channel consists of an attenuator, the gain block, and an anti-alias filter. Each conditioned signal is then digitized by a 24-bit delta-sigma ADC to achieve simultaneous data acquisition. After the signal is digitized it passes through various DSP steps before being sent to software. Refer to the *Timing Engines and DSP Streams* section for more information about this digital block.

Figure 2-5. PXIe-4304/4305 Block Diagram



Signal Acquisition Considerations

This section contains information about signal acquisition concepts, including operation modes, delta-sigma converters, Nyquist frequency and bandwidth, timing, triggering, and synchronization.

Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an ADC, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of f_s can represent only signals with frequencies lower than $f_s/2$. This maximum frequency is known as the *Nyquist frequency*. The bandwidth from 0 Hz to the Nyquist frequency is the *Nyquist bandwidth*.

ADC

The PXIe-4304/4305 ADCs use a conversion method known as delta-sigma modulation. This approach involves oversampling the input signal and then decimating and filtering the resulting data to achieve the desired sample rate. The PXIe-4304 supports rates of 1 S/s to 5 kS/s. The PXIe-4305 supports rates of 1 S/s to 51.2 kS/s.

Operation Modes

The PXIe-4304/4305 supports two modes of operation: Buffered Mode and Hardware-Timed Single Point Mode. In a Buffered Mode acquisition, oversampled data is decimated to your requested sample rate and digital anti-alias filters are applied to filter out frequency content above the Nyquist frequency. These digital anti-alias filters introduce group delay and for some applications this may be undesirable. For this reason, the PXIe-4304/4305 also supports Hardware-Timed Single Point Mode. In Hardware-Timed Single Point Mode the oversampled data is filtered with a much looser filter to reduce the group delay.

Buffered Mode Acquisitions

In Buffered Mode, the PXIe-4304/4305 uses a combination of analog and digital filtering to provide an accurate representation of in-band signals while rejecting out-of-band signals. These filters discriminate between signals based on the frequency range, or bandwidth, of the signal. The three important bands to consider are the passband, the stopband, and the alias-free bandwidth.

In Buffered Mode, the PXIe-4304/4305 accurately represents signals within the passband, as quantified primarily by passband flatness and phase nonlinearity. All signals that appear in the alias-free bandwidth are either unaliased signals or signals that have been filtered by at least the amount of the stopband rejection.

Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine if aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. In Buffered Mode, the PXIe-4304/4305 employs both digital and analog lowpass filters to achieve this protection.

In Buffered Mode, the PXIe-4304/4305 uses an oversampled architecture and sharp digital filters[1] with cut-off frequencies that track the sampling rate. Therefore the filter automatically adjusts to follow the Nyquist frequency. Although the digital filter eliminates almost all out-of-band components, it is still susceptible to aliases from certain narrow frequency bands located at frequencies far above the sampling rate. These frequencies are referred to as the ADC alias holes.

[1] Looser filters with degraded alias-free bandwidth are used for sample rates <25 Hz. This is done in order to reduce the large group delays associated with filtering at lower sample rates. Refer to the *PXIe-4304/4305 Specifications* document for performance at lower rates.

To minimize the error from the ADC alias holes, the PXIe-4304/4305 features a fixed-frequency analog filter. This analog filter removes high-frequency components in the analog signal path before they reach the ADC. This filtering addresses the possibility of high-frequency aliasing from the narrow bands that are not covered by the digital filter.

Passband

The signals within the passband have frequency-dependent gain or attenuation. The small amount of variation in gain with respect to frequency is called the passband flatness. The digital anti-alias filters of the PXIe-4304/4305 adjust the frequency range of the passband to match the sample rate. Therefore, the amount of gain or attenuation at a given frequency depends on the sample rate.

Stopband

The digital anti-alias filter significantly attenuates all signals above the stopband frequency to prevent aliasing. Therefore, the stopband frequency scales precisely with the sample rate. The stopband rejection is the minimum amount of attenuation applied by the anti-alias filter to all signals with frequencies within the stopband.

Alias-Free Bandwidth

Any signal that appears in the alias-free bandwidth of the PXIe-4304/4305 is not an aliased artifact of signals at a higher frequency. The alias-free bandwidth is defined by the ability of the filter to reject frequencies above the stopband frequency, and it is equal to the sample rate minus the stopband frequency.

Filter Group Delay

The anti-alias digital filtering performed by the PXIe-4304/4305 produces a delay of many samples worth of time between when an event occurs on the input signal going into the PXIe-4304/4305 and when the data associated with that event is available at the output of the acquisition and filtering process. This delay is called the group delay.

In order to simplify the process of acquiring data from the PXIe-4304/4305 modules and correlating that data with data from other modules, the PXIe-4304/4305 compensates for this group delay in the following ways:

- The Sample Clock output from the PXIe-4304/4305 is generated at the point in time when the input signal is valid at the ADC input pins. When acquiring data, the PXIe-4304/4305 generates a Sample Clock, then waits for the data associated with that Sample Clock to be acquired, then returns that data. As a result, any other acquisitions timed with this Sample Clock line up with the data returned by the PXIe-4304/4305.
- Any triggers generated or received by the PXIe-4304/4305 are interpreted based on their relationship to the Sample Clock being generated. For example, a Start Trigger that starts an acquisition results in data from the next Sample Clock being returned as the first point in the acquisition. Refer to the *Triggering and Filter Delay* section for more details about how this affects analog trigger events.

- On demand software sampling returns a single sample from an acquisition running at the maximum supported sample rate of the module. For any on-demand, software timed acquisition the PXIe-4304/4305 waits for the group delay to elapse before returning the sample. As a result, the data returned aligns closely in time with when the data was requested and is delayed by the sum of the analog input delay and digital filter delay.[1]

Optional Buffered Mode IIR Filtering

In addition to the sharp anti-alias filters used in Buffered Mode, the PXIe-4304/4305 also provides optional fourth order elliptical lowpass IIR filters that can be used in Buffered Mode. These lowpass filters have fixed cut-off frequencies that are not related to the sample rate and are intended to replicate placing an analog filter on the input. For example, if you want to filter out 60 Hz power line noise, you can select the digital 2 Hz lowpass filter and still use any desired sample rate.

The optional lowpass filter is in addition to the anti-alias filter. Therefore, the optional lowpass filter is only meaningful in the passband of the anti-alias filter. The anti-alias filter will still reject frequencies beyond the Nyquist frequency.

By default, the optional lowpass digital filter is not enabled. Each channel in a Buffered Mode task can independently be configured to use any of the available filters that the PXIe-4304/4305 supports. Refer to *Digital AI Filtering* in the *NI-DAQmx Help* for more information about how to configure the filter used. Refer to the *NI PXI-4304/4305 Specifications* for more information about the cut-off frequencies supported and response characteristics of these filters.

Filter Settling Time

When a lowpass filter is first enabled, it takes time for the filter to settle to a correct value. Software automatically waits a fixed amount of time after enabling the filter and before starting a task to prevent showing invalid data. The amount of time software waits is dependent on the cut-off frequency of the filter selected. The lower the cut-off frequency, the longer software must wait for the filter to settle. Refer to the *PXIe-4304/4305 Specifications* for more information.

Filter Group Delay

Like all filters, the optional lowpass filter has group delay associated with it. Since the optional filters are IIR, the group delay is a function of both cut-off frequency and the frequency of the signal being attenuated. Since the group delay is not constant for all input frequencies, it cannot be automatically compensated for and will therefore appear as an additional delay on the input. Refer to the *PXIe-4304/4305 Specifications* for more information.

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[1] The maximum sample rate of the PXIe-4304/4305 is 51.2 kS/s. In addition to the fixed analog input delay, you must also account for the digital-filter group delay. For 51.2 kS/s, the digital filter group delay is

$$1.79742\ \text{ms} + \frac{48.5\ \text{S}}{51.2\ \text{kS/s}} = 1.79837\ \text{ms}\ .$$

The total delay is 1.79837 ms + 6.77 µs = 1.80514 ms. Refer to the *PXIe-4304/4305 Specifications* for more information.

Hardware-Timed Single Point Acquisitions

Hardware-Timed Single Point (HWTSP) is a Hardware-Timed Acquisition Mode in which a digital hardware signal (SampleClock) controls the rate of the acquisition. The SampleClock signal can be imported or internally generated on the PXIe-4304/4305 using the sample rate configured with a NI-DAQmx task.

During Buffered acquisitions, the device may wait to transfer data to the host machine to build larger bus transactions. This optimizes throughput. During HWTSP acquisitions, the device sends data to the host in response to every sample clock. This optimizes latency.

These features make HWTSP ideal for real-time control applications. HWTSP acquisitions, in conjunction with the wait for next sample clock function, provide more deterministic synchronization between the software layer and the hardware layer. Refer to the *NI-DAQmx Hardware-Timed Single Point Lateness Checking* document for more information. To access this document, go to `ni.com/info` and enter the Info Code `daqhwtsp`.

Hardware-Timed Single Point Acquisition Model

The HWTSP data path is optimized for low-latency applications and is different than the data path used in Buffered Mode acquisitions.

When in HWTSP mode, the filtering and sampling systems can be modeled as being decoupled, which allows you to configure the filter and sampling rate independently.

Figure 2-6 shows the HWTSP data path model.

Figure 2-6. HWTSP Data Path Model

The ADC samples the input stream and returns it to the PXI Express controller or computer based on the SampleClock signal.

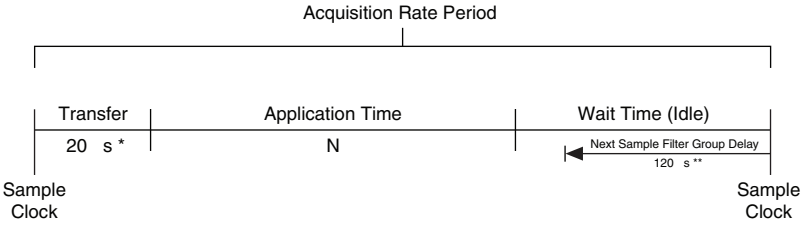
Maximum HWTSP Rate Analysis

During HWTSP acquisitions the maximum achievable acquisition rate without missing a sample is affected by both the transfer and application time. Refer to Figure 2-7.

$$Rate_{MAX} = \frac{1}{TransferTime + ApplicationTime}$$

Note HWTSP acquisitions can detect if they cannot keep up with the acquisition rate. Refer to the *Hardware-Timed Single Point Sample Mode* topic in the *NI-DAQmx Help* for more information.

Figure 2-7. Transfer Time and Application Time Relationship



*Transfer time may vary depending on system.
**120 s is the approximate group delay of the 2 kHz filter for input frequencies < 1 kHz (passband of the filter).

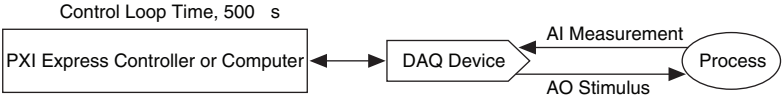
Note For control applications, it is important to consider the group delay of the data being acquired and analyzed when calculating the control system bandwidth. Regardless of the sample rate, the bandwidth of the system is as follows:

$$bandwidth = \frac{1}{TransferTime + ApplicationTime + GroupDelay}$$

2 kHz Control Loop Rate Calculation Example

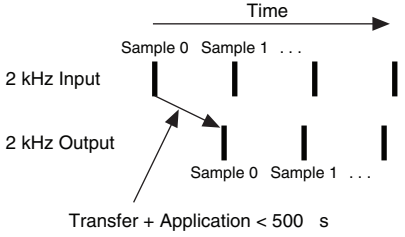
Figure 2-8 represents a typical control system in which you have a process to control, a DAQ device to do the acquisitions and generate stimulus, and a PXI Express controller or computer to do the data processing and determine the proper AO value and returning it to the process.

Figure 2-8. Typical Control System



To successfully close a 2 kHz control loop, make sure that the time between the time the AI sample is acquired and the time the AO stimulus is generated is <500 µs. Refer to Figure 2-9.

Figure 2-9. Input and Output of a Control System with Bandwidth ≥2 kHz



To make sure that your application can run and control a process at 2 kHz, and that the first output is generated within the first sample period, make sure that the following conditions are satisfied:

$$500\ \mu s \leq Transfer\ Time + Application\ Time \quad (2\text{-}1)$$

where:

Transfer Time—the time it takes to transfer samples between the DAQ device and the PXI Express controller or computer.

Application Time—the time it takes for the PXI Express controller or computer to analyze the acquired data and generate the AO stimulus.

Using Equation 2-1 and the Transfer Time from the sample system described in this section, you can determine that an application time of 480 µs is required to close a 2 kHz control loop.

$$Application\ Time \leq 500\ \mu s - Transfer\ Time$$

$$Application\ Time \leq 500\ \mu s - 20\ \mu s$$

$$Application\ Time \leq 480\ \mu s$$

Any application taking more than 480 µs will fail to close the 2 kHz control loop.

When analyzing the bandwidth of the system, you must consider the group delay of all the components of the system. When using only the PXIe-4304/4305 internal 2 kHz filter, the bandwidth of the control loop is as follows:

$$ControlBandwidth = \frac{1}{TransferTime + ApplicationTime + FilterGroupDelay}$$

$$ControlBandwidth = \frac{1}{20\ s + 480\ s + 120\ s}$$

$$Control\ Bandwidth = 1.613\ kHz$$

Note You can increase the bandwidth of the system by either reducing the application time or by using another filter option with lower group delay.

Timing and Triggering

This section contains information about the timing and triggering theory of operation.

Sample Clock Timebase

The ADCs require an oversample clock to drive the conversion. The oversample clock frequency is greater than the sample rate. On the PXIe-4304/4305 modules the oversample clock is produced from a 106.25 MHz reference clock. This 106.25 MHz reference clock can be phase locked with the PXI Express backplane 100 MHz clock or be generated by an internal timebase

that runs freely. Multiple modules can be synchronized by selecting the PXI Express backplane 100 MHz clock as the reference clock source for all the modules. Refer to the *Reference Clock Synchronization* section for more information.

External Clock

The PXIe-4304/4305 ADCs cannot be clocked from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit `ni.com/soundandvibration` for more information about the Sound and Vibration Measurement Suite.

Digital Triggering

You can configure the PXIe-4304/4305 modules to start an acquisition in response to a digital trigger signal from one of the PXI Express backplane trigger lines or the PFI from the front connector. The trigger circuit can respond either to a rising or a falling edge.

Analog Triggering

Analog triggering allows you to trigger your application based on an input signal and trigger level you define. You can configure the analog trigger circuitry to monitor any input channel acquiring data. Choosing an input channel as the trigger channel does not change the input channel acquisition specifications.

The analog trigger signal can be used as a reference trigger only. In a reference-triggered acquisition, you configure the module to acquire a certain number of pre-trigger samples and a certain number of post-trigger samples. Reference-triggered acquisitions can therefore only be configured as finite tasks. The analog trigger on the PXIe-4304/4305 cannot be used as a start trigger. This restriction is a result of the way the module compensates for the filter group delay.

When using an analog reference trigger, the module first waits for the specified number of pre-trigger samples to be acquired. Once enough pre-trigger samples are acquired, the reference trigger will occur the next time the analog trigger condition is met. You also can route the resulting reference trigger event to supported digital terminals. Refer to the device panels in NI Measurement & Automation Explorer (MAX) for additional information.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

You can use several analog triggering modes with the PXIe-4304/4305 modules, for instance analog edge, analog edge with hysteresis, and window triggering.

Triggering and Filter Delay

The PXIe-4304/4305 interprets triggers based on where they occur in time. The hardware automatically compensates for its group delay such that data from this module will line up closely in time with the occurrence of the trigger event. However, the group delay affects how long it takes to receive data when starting an acquisition. Since linear phase FIR filters are used in the digital filtering, it is necessary to wait for the filter group delay to elapse after sending a sync pulse before the start trigger can be correctly handled in time. Step 6 in the *Reference Clock Synchronization* section allows NI-DAQmx to handle this delay automatically. After the digital start trigger, you cannot read data for the first sample in software until the digital filter group delay has elapsed. Therefore, it takes a total of twice the digital filter group delay to start an acquisition. You can insert additional time between when the sync pulse occurs and when the start trigger occurs. This will not affect the time it takes before samples are available after the start trigger, which is always the group delay time. Group delay time increases as sample rates decrease. Refer to the *PXIe-4304/4305 Specifications* document for details regarding the group delay at different sample rates.

Synchronization

Some applications require tight synchronization between input and output operations on multiple modules. Synchronization is important to minimize skew between channels and to eliminate clock drift between modules in long-duration operations. You can synchronize the analog input operations on two or more PXIe-4304/4305 modules to extend the channel count for your measurements. In addition, the PXIe-4304/4305 can synchronize with certain DSA modules, such as the PXIe-449x modules, using Reference Clock Synchronization.

Reference Clock Synchronization

With reference clock synchronization, master and slave modules generate their ADC oversample clock from the shared 100 MHz reference clock from the PXI Express backplane (PXIe_CLK100). The backplane supplies an identical copy of this clock to each peripheral slot. In addition, multiple chassis can be synchronized by using a timing and synchronization board to lock the 100 MHz clock across chassis.

When you acquire data from multiple modules within the same NI-DAQmx task, NI-DAQmx will automatically handle all of the Reference Clock Synchronization details required to synchronize the modules within the task. This is known as a Multi-Device Task.

To perform Reference Clock Synchronization when using multiple NI-DAQmx tasks that are acquiring at the same rate, complete the following steps to synchronize the hardware.

1. Specify PXIe_CLK100 as the reference clock source for all modules to force all the modules to lock to the reference clock on the PXI Express chassis.
2. Choose an arbitrary PXIe-4304/4305 master module to issue a sync pulse on one of the PXIe Trigger lines. The sync pulse resets the ADCs and oversample clocks, phase aligning all the clocks in the system to within nanoseconds.
3. Configure the rest of the modules in your system to receive their sync pulse from the sync pulse master module. This will ensure all ADCs are running in lockstep.

4. Choose one module to be the start trigger master. This does not have to be the same module you chose in step 3.
5. Configure the rest of the modules in your system to receive their start trigger from the start trigger master module. This ensures that all modules will begin returning data on the same sample.
6. Set the synchronization type of the Start Trigger slaves at **DAQmx Trigger»Advanced» Synchronization»Synchronization Type** to Slave and that of the Master to Master.
7. Query **DAQmx Timing»More»Synchronization Pulse»Synchronization Time** on all modules being synchronized, choose the maximum value and set that as the **DAQmx Timing»More»Synchronization Pulse»Minimum Delay To Start** on the module from which the synchronization pulse originates.
8. Commit all of the sync pulse slave module tasks using the DAQmxTaskControl VI/Function. This sets them up to expect the sync pulse from the master.
9. Commit the sync pulse master module task using the DAQmxTaskControl VI/Function. This will issue the sync pulse.
10. Start all of the start trigger slave module tasks. This sets them up to expect the start trigger from the master.
11. Start the start trigger master module task. You can now acquire data.

Tip Consider using a Multi-Device task when synchronizing multiple devices at the same rate.

Tip You can find example VIs in the NI Example Finder. Select **Help»Find Examples** to launch the NI Example Finder.

Consider the following caveat to using Reference Clock synchronization:

- The PXIe-4304/4305 automatically compensates for its filter group delay. However, some other device families do not compensate for their filter delay. In this case, manually compensate for group delay in the waveforms when you synchronize between device families if this level of synchronization is required for your application.

Timing Engines and DSP Streams

This section gives an overview of the internal implementation of the PXIe-4304/4305 and the limitations that exist on how the PXIe-4304/4305 can be configured. The use of NI-DAQmx software allows you to easily configure the PXIe-4304/4305 without you needing in depth knowledge about the internal workings of hardware. However, there are limitations in the way in which the PXIe-4304/4305 can be configured and to understand them requires some explanation about what is happening in hardware.

Timing Engines

When you create a task in software, that software task interacts with one or more timing engines in the PXIe-4304/4305. There are a total of four timing engines in hardware that can be operated simultaneously. Each of these timing engines can have individualized configuration settings for timing, triggering, and the sample mode. Depending on the sample mode selected, the timing engine will use either a Buffered Mode or Hardware-Timed Single Point DSP stream.

DSP Streams

The DSP streams in the PXIe-4304/4305 perform the digital signal processing on the acquired data before sending the data to software. There are two types of DSP streams: Buffered Mode streams and Hardware-Timed Single Point streams. The PXIe-4304/4305 has four streams for each of these types and each stream can handle up to 8 channels. Therefore, it is possible to use all 32 channels in either Buffered Mode or Hardware-Timed Single Point Mode.

AI Channels and DSP Streams

While all 32 analog input channels are simultaneously digitized by their ADC, the controls of the ADCs are grouped into four banks of eight. The configuration of the ADCs is different for Buffered Mode and Hardware-Timed Single Point Mode, and as a result, there are limitations on how channels can be used when both buffered and Hardware-Timed Single Point tasks operate simultaneously. Analog input channels in the following banks must all be configured for either Buffered Mode or Hardware-Timed Single Point Mode: ai0:7, ai8:15, ai16:23, and ai24:31.

To allow greater flexibility in how the PXIe-4304/4305 can be configured, a cross-point switch exists between the ADCs and the DSP streams. This cross-point switch allows a single DSP stream to use any eight of the 32 analog input channels, as long as the ADC for the analog input channel selected is configured for the same mode as the DSP stream. Once an analog input channel is used in a task, it is not available for use in other tasks.

Examples of Limitations

The following configuration scenarios will cause errors:

- A task is setup and started using ai0 in Buffered Mode. A second task is created with ai1 in Hardware-Timed Single Point Mode. The second task will produce an error since the first task has already placed ai0:7 in Buffered Mode and therefore ai1 cannot be used in Hardware-Timed Single Point Mode.
- A task is set up and started using ai0 in Buffered Mode. A second task is created with ai0 also in Buffered Mode. The second task will produce an error since the first task is already using ai0.
- Four Buffered Mode tasks are setup and started, each with a single and different ai channel and operating at different sample rates. A fifth task is created. The fifth task will produce an error, regardless of how it is configured, since the first four tasks are using the four timing engines, one per task.
- A Buffered Mode task is setup and started using ai0:24. A second Buffered Mode task is created using ai25. The second task will produce an error since the first task has 25 total

channels and therefore must use all four Buffered Mode streams; each stream can handle only eight channels. There is not an unused Buffered Mode stream available. If the second task was set for Hardware-Timed Single Point Mode, an error would still be produced by the second task since ai24 in the first task has forced ai24:ai31 to all be Buffered Mode channels.

Accessory Auto-Detection

SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any calibration or scaling information associated with the terminal block.

MAX allows you to see which accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status.

3

SC Express Considerations

This chapter details the clock and trigger functionality available through the PXI Express chassis.

SC Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common, low-skew 100 MHz reference clock used for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXIe_SYNC100

PXIe_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe_SYNC100 independently to each peripheral slot in a PXI Express chassis. PXIe_SYNC100 allows modules using PXIe_CLK100 as their reference to recreate the timing of the PXI_CLK10 signal while taking advantage of the lower skew of PXIe_CLK100. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common, low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis. In PXI Express chassis, the PXI_CLK10 signal is in phase with PXIe_CLK100.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI/PXI Express chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

In a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple modules or to share a common trigger signal among modules.

A system timing controller can be installed in the system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a System timing controller. PXI_STAR can be used as a trigger signal for input operations.

An SC Express module is not a System timing controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXIe_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that route between a PXI Express system timing controller and a peripheral device. Using multiple connections simplifies the creation of applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

Table 3-1. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

A

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