COMPREHENSIVE SERVICES

We offer competitive repair and calibration services, as well as easily accessible documentation and free downloadable resources.

SELL YOUR SURPLUS

We buy new, used, decommissioned, and surplus parts from every NI series. We work out the best solution to suit your individual needs.

Sell For Cash Get Credit Receive a Trade-In Deal

OBSOLETE NI HARDWARE IN STOCK & READY TO SHIP

We stock **New, New Surplus, Refurbished,** and **Reconditioned** NI Hardware.

APEX WAVES

Bridging the gap *between the manufacturer and your legacy test system.*

1-800-915-6216

www.apexwaves.com

sales@apexwaves.com

Request a Quote CLICK HERE *sbRIO-9651*

NI sbRIO-9651

System on Module

Carrier Board Design Guide

March 2017
376960C-01

NATIONAL INSTRUMENTS™

Worldwide Technical Support and Product Information

ni.com

Worldwide Offices

Visit ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

National Instruments Corporate Headquarters

11500 North Mopac Expressway Austin, Texas 78759-3504 USA Tel: 512 683 0100

For further support information, refer to the *NI Services* appendix. To comment on National Instruments documentation, refer to the National Instruments website at ni.com/info and enter the Info Code feedback.

Legal Information

Limited Warranty

This document is provided ‘as is’ and is subject to being changed, without notice, in future editions. For the latest version, refer to `ni.com/manuals`. NI reviews this document carefully for technical accuracy; however, NI MAKES NO EXPRESS OR IMPLIED WARRANTIES AS TO THE ACCURACY OF THE INFORMATION CONTAINED HEREIN AND SHALL NOT BE LIABLE FOR ANY ERRORS.

NI warrants that its hardware products will be free of defects in materials and workmanship that cause the product to fail to substantially conform to the applicable NI published specifications for one (1) year from the date of invoice.

For a period of ninety (90) days from the date of invoice, NI warrants that (i) its software products will perform substantially in accordance with the applicable documentation provided with the software and (ii) the software media will be free from defects in materials and workmanship.

If NI receives notice of a defect or non-conformance during the applicable warranty period, NI will, in its discretion: (i) repair or replace the affected product, or (ii) refund the fees paid for the affected product. Repaired or replaced Hardware will be warranted for the remainder of the original warranty period or ninety (90) days, whichever is longer. If NI elects to repair or replace the product, NI may use new or refurbished parts or products that are equivalent to new in performance and reliability and are at least functionally equivalent to the original part or product.

You must obtain an RMA number from NI before returning any product to NI. NI reserves the right to charge a fee for examining and testing Hardware not covered by the Limited Warranty.

This Limited Warranty does not apply if the defect of the product resulted from improper or inadequate maintenance, installation, repair, or calibration (performed by a party other than NI); unauthorized modification; improper environment; use of an improper hardware or software key; improper use or operation outside of the specification for the product; improper voltages; accident, abuse, or neglect; or a hazard such as lightning, flood, or other act of nature.

THE REMEDIES SET FORTH ABOVE ARE EXCLUSIVE AND THE CUSTOMER’S SOLE REMEDIES, AND SHALL APPLY EVEN IF SUCH REMEDIES FAIL OF THEIR ESSENTIAL PURPOSE.

EXCEPT AS EXPRESSLY SET FORTH HEREIN, PRODUCTS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND AND NI DISCLAIMS ALL WARRANTIES, EXPRESSED OR IMPLIED, WITH RESPECT TO THE PRODUCTS, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE OR NON-INFRINGEMENT, AND ANY WARRANTIES THAT MAY ARISE FROM USAGE OF TRADE OR COURSE OF DEALING. NI DOES NOT WARRANT, GUARANTEE, OR MAKE ANY REPRESENTATIONS REGARDING THE USE OF OR THE RESULTS OF THE USE OF THE PRODUCTS IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. NI DOES NOT WARRANT THAT THE OPERATION OF THE PRODUCTS WILL BE UNINTERRUPTED OR ERROR FREE.

In the event that you and NI have a separate signed written agreement with warranty terms covering the products, then the warranty terms in the separate agreement shall control.

Copyright

End-User License Agreements and Third-Party Legal Notices

You can find end-user license agreements (EULAs) and third-party legal notices in the following locations:

- Notices are located in the `<National Instruments>\_Legal Information` and `<National Instruments>` directories.
- EULAs are located in the `<National Instruments>\Shared\MDF\Legal\license` directory.
- Review `<National Instruments>\_Legal Information.txt` for information on including legal information in installers built with NI products.

U.S. Government Restricted Rights

If you are an agency, department, or other entity of the United States Government (“Government”), the use, duplication, reproduction, release, modification, disclosure or transfer of the technical data included in this manual is governed by the Restricted Rights provisions under Federal Acquisition Regulation 52.227-14 for civilian agencies and Defense Federal Acquisition Regulation Supplement Section 252.227-7014 and 252.227-7015 for military agencies.

Trademarks

Refer to the *NI Trademarks and Logo Guidelines* at `ni.com/trademarks` for more information on National Instruments trademarks.

ARM, Keil, and µVision are trademarks or registered trademarks of ARM Ltd or its subsidiaries.

LEGO, the LEGO logo, WEDO, and MINDSTORMS are trademarks of the LEGO Group.

TETRIX by Pitsco is a trademark of Pitsco, Inc.

FIELDBUS FOUNDATION™ and FOUNDATION™ are trademarks of the Fieldbus Foundation.

Patents

For patents covering National Instruments products/technology, refer to the appropriate location: **Help»Patents** in your software, the `patents.txt` file on your media, or the *National Instruments Patent Notice* at `ni.com/patents`.

Export Compliance Information

Refer to the *Export Compliance Information* at `ni.com/legal/export-compliance` for the National Instruments global trade compliance policy and how to obtain relevant HTS codes, ECCNs, and other import/export data.

WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

YOU ARE ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY AND RELIABILITY OF THE PRODUCTS WHENEVER THE PRODUCTS ARE INCORPORATED IN YOUR SYSTEM OR APPLICATION, INCLUDING THE APPROPRIATE DESIGN, PROCESS, AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

PRODUCTS ARE NOT DESIGNED, MANUFACTURED, OR TESTED FOR USE IN LIFE OR SAFETY CRITICAL SYSTEMS, HAZARDOUS ENVIRONMENTS OR ANY OTHER ENVIRONMENTS REQUIRING FAIL-SAFE PERFORMANCE, INCLUDING IN THE OPERATION OF NUCLEAR FACILITIES; AIRCRAFT NAVIGATION; AIR TRAFFIC CONTROL SYSTEMS; LIFE SAVING OR LIFE SUSTAINING SYSTEMS OR SUCH OTHER MEDICAL DEVICES; OR ANY OTHER APPLICATION IN WHICH THE FAILURE OF THE PRODUCT OR SERVICE COULD LEAD TO DEATH, PERSONAL INJURY, SEVERE PROPERTY DAMAGE OR ENVIRONMENTAL HARM (COLLECTIVELY, “HIGH-RISK USES”). FURTHER, PRUDENT STEPS MUST BE TAKEN TO PROTECT AGAINST FAILURES, INCLUDING PROVIDING BACK-UP AND SHUT-DOWN MECHANISMS. NI EXPRESSLY DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY OF FITNESS OF THE PRODUCTS OR SERVICES FOR HIGH-RISK USES.

Contents

About This Document

Chapter 1
Fixed Behavior Signals

Chapter 2
User-Defined FPGA Signals

Chapter 3
Carrier Board PCB Layout Guidelines

Chapter 4
Mechanical Considerations

Appendix A
Reference Carrier Board Specifications and User Guide

Appendix B
Revision History

Appendix C
NI Services

About This Document

The NI sbRIO-9651 System on Module (SOM) provides an embedded real-time processor and reconfigurable FPGA. The sbRIO-9651 SOM requires a user-designed carrier board to provide power and I/O interfaces. You can optimize the carrier board to implement the exact functions your application requires. You can design the carrier board size and connector locations to fit the packaging or enclosure of your specific system.

This document provides detailed information about carrier board design techniques, guidelines, and requirements.

Note Refer to the documents listed in the *Additional Documentation Resources* section of this chapter for more information as you design, prototype, and implement your sbRIO-9651 SOM application. In particular, refer to the *NI sbRIO-9651 System on Module OEM Device Specifications* for dimensions, pinout information, functional specifications, and electrical specifications for the sbRIO-9651 SOM.

Terminology

Table 1 defines terms used in this document to describe sbRIO-9651 SOM concepts and technology.

Table 1. sbRIO-9651 SOM Terminology in This Document

Term	Definition
System Components	
J1	Molex 45971-4185 320-pin, 8 × 40 position, SEARAY open-pin-field-array connector on the sbRIO-9651 SOM.
SEARAY	Connector family used for the J1 connector on the sbRIO-9651 SOM. Manufactured by Samtec and Molex.
SOM	System on Module.
SoC	System on Chip.
USB Device	Physical, electrical, addressable, and logical entity that is attached to USB and performs a function.
USB Device port	Port on a carrier board that provides a USB Device interface to the SOM.
USB Host	USB interface that controls the bus and communicates with connected USB devices.
USB Host port	Port on a carrier board that provides a USB Host interface from the SOM.

Table 1. sbRIO-9651 SOM Terminology in This Document (Continued)

Term	Definition
Reference Schematic and Signal Naming	
LVTTL	In compliance with the Low-Voltage Transistor-Transistor Logic (LVTTL) specification.
LVCMOS	In compliance with the Low-Voltage Complementary Metal Oxide Semiconductor (LVCMOS) specification.
PUDC	Pull-up During Configuration
Mechanical	
CPU/FPGA temperature	The temperature reported digitally by a sensor that measures the die junction temperature of the Xilinx Zynq SoC.
Primary System temperature	The temperature reported digitally by a sensor on the Xilinx Zynq SoC side of the circuit card assembly underneath the integrated heat spreader. This value is an approximation of the local ambient temperature inside the heat spreader.
Secondary System temperature	The temperature reported digitally by a sensor on the SEARAY side of the circuit card assembly. This value is a conservative approximation of the local ambient temperature on that side of the circuit card assembly.

Schematic Conventions

Table 2 describes symbol conventions used in the I/O interface schematic diagrams in this document.

Table 2. Schematic Conventions in This Document

Symbol	Description
	Off-page symbol that represents communication to and from the mating connector.
	Off-page symbol that represents communication from the mating connector.
	Off-page symbol that represents communication to the mating connector.
	On-page symbol that represents the signal being driven.

Table 2. Schematic Conventions in This Document (Continued)

Symbol	Description
	On-page symbol that represents the signal being received.
	Power supply rail.
	Analog ground.
	Digital ground.
	Chassis ground.
SPARE	Refers to an unpopulated reference designator.

Additional Documentation Resources

Refer to the following additional resources as you design, prototype, and implement your sbRIO-9651 SOM application.

What Would You Like to Learn More About?	Resources	Availability
NI sbRIO-9651 System on Module OEM Device	*NI sbRIO-9651 System on Module OEM Device Specifications*	PDF
NI sbRIO-9651 System on Module Development Kit	*NI sbRIO-9651 System on Module Development Kit Quick Start Guide*	PDF, Included in the shipping kit
Designing a carrier board for your application	*NI sbRIO-9651 System on Module Carrier Board Design Guide*	PDF
Adding an sbRIO-9651 System on Module target in LabVIEW	*LabVIEW Help (NI-RIO)*	Help file available locally
Creating a socketed CLIP that defines the I/O configuration to use in your application	*NI Single-Board RIO CLIP Generator Help*	Help file available locally

NI Training and Support	`ni.com/singleboard/setup`
	`ni.com/training`
	`ni.com/support`
		Available online at ni.com

PDF available online at ni.com/manuals | Help file available locally | Included in the shipping kit | Available online at ni.com

1 Fixed Behavior Signals

A subset of pins on the J1 connector on the sbRIO-9651 SOM are dedicated to implementing the following specific I/O functionality:

- Primary Ethernet (GBE0)
- USB Host/Device (USB0)
- USB Host (USB1)
- UART/Console Out (Serial1)
- SD Card

Other pins on the J1 connector are dedicated to implementing the following support signals:

- RTC Battery (VBAT)
- Resets
- Status LED
- FPGA Config
- Temp Alert

Note Refer to the *NI sbRIO-9651 System on Module OEM Device Specifications* for a complete list of all pins and signals on the J1 connector.

The reference carrier board included with the sbRIO-9651 SOM development kit demonstrates how to implement each of these signals. Refer to the specific sections in this chapter for more information about how the reference carrier board implements each signal.

Primary Ethernet (GBE0)

The sbRIO-9651 SOM provides a primary Gigabit Ethernet port (GBE0) for use on a carrier board. Refer to the *Secondary Ethernet (GBE1)* section of Chapter 2, *User-Defined FPGA Signals*, for information about implementing a secondary Gigabit Ethernet port.

GBE0 Signal Definitions

Table 1-1 describes the GBE0 port pins and signals on the J1 connector on the sbRIO-9651 SOM.

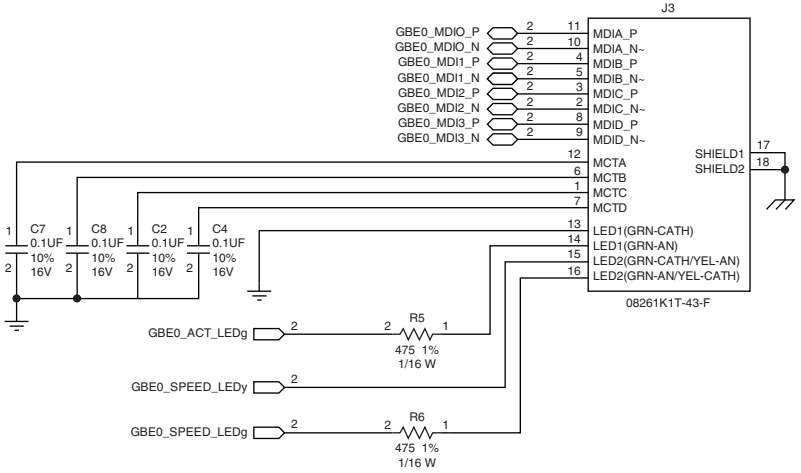
Table 1-1. GBE0 Signal Definitions

Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
GBE0_MDI0_P GBE0_MDI0_N GBE0_MDI1_P GBE0_MDI1_N GBE0_MDI2_P GBE0_MDI2_N GBE0_MDI3_P GBE0_MDI3_N	1 9 18 26 3 11 20 28	I/O	Defined by Ethernet PHY specification.	Pre-magnetic Gigabit Ethernet data pairs.
GBE0_SPEED_LEDg GBE0_SPEED_LEDy	5 13	O	LVTTL	Speed LED signals.
GBE0_ACT_LEDg	6	O	LVTTL	Activity/link LED signal.
* I/O direction is with respect to the sbRIO-9651 SOM.				

GBE0 Implementation on the Reference Carrier Board

Figure 1-1 shows a schematic design for the GBE0 implementation on the reference carrier board.

Figure 1-1. GBE0 Reference Schematic



Reference Schematic Design Considerations

Table 1-2 lists design considerations for the schematic shown in Figure 1-1.

Table 1-2. GBE0 Reference Schematic Design Considerations

Consideration	Notes
MDI data pairs	• The MDI data pairs are routed differentially and connected directly to the Ethernet connector. • The Ethernet connector has the required Ethernet magnetics built into it. You may use discrete magnetics instead.
LED signals	• The LED signals can be used to directly drive connector LEDs. • The current-limiting resistors must be sized so that the drive current of the LED signals is not exceeded. • Refer to the *Ethernet Speed LED Behavior* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for information about Ethernet LED signal behavior and rated drive current.

Gigabit Ethernet Magnetic Requirements

The Ethernet PHY on the sbRIO-9651 SOM uses voltage-mode drivers for the MDI pairs, which greatly reduces the power that the magnetics consume and eliminates the need for a sensitive center tap power supply.

You must consider the following requirements for connecting center taps:

- Do not connect the center taps of the isolation transformer on the MDI pair side to any power source. Keep the center taps separate from each other.
- Connect each center tap through separate 0.1 µF capacitors to ground. The separation is required because the common-mode voltage on each MDI pair might be different.

Table 1-3 lists recommended magnetic characteristics.

Table 1-3. Recommended Magnetic Characteristics

Parameter	Value	Test Condition
Turns ratio	1 CT : 1 CT	—
Open-circuit inductance (min)	350 µH	100 mV, 100kHz, 8 mA
Insertion loss (max)	1.0 dB	0 MHz to 100 MHz
HIPOT (min)	1500 Vrms	—

The sbRIO-9651 SOM development kit uses the Gigabit Ethernet connector parts described in Table 1-4.

Table 1-4. Gigabit Ethernet Connector Parts

Part	Manufacturer	Part Number
sbRIO-9651 SOM PHY	Micrel	KSZ9031MNXIA
Reference carrier board Gigabit Ethernet connector	Bel Stewart Magjack	0826-1K1T-43-F

Refer to the datasheet for the Micrel Ethernet PHY for more information about magnetic requirements.

GBE0 Routing Considerations

NI recommends the following design practices for properly routing GBE0 signals on your carrier board:

- Route MDI pairs differentially with 100 Ω differential trace impedance.
- Length-match the positive and negative signal for each MDI data pair to within 10 mils.

- Limit the MDI trace lengths on the carrier board to 6.0 in. or less, which is the length at which Ethernet compliance was tested.

USB (USB0, USB1)

The sbRIO-9651 SOM provides two USB 2.0-compliant ports for use on a carrier board: USB Host/Device port (USB0) and USB Host port (USB1).

Note Your carrier board design must provide the 5 V USB_VBUS power to USB Host ports and must limit the current supplied to each host port according to USB specifications.

USB0 Host/Device Signal Definitions

Table 1-5 describes the USB0 Host/Device port pins and signals on the sbRIO-9651 SOM connector.

Table 1-5. USB0 Host/Device Signal Definitions

Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
USB0_DP	33	I/O	Defined by USB specification.	USB0 data pair.
USB0_DN	41			
USB0_MODE	65	I	LVTTL	Controls whether the USB0 port provides a Host or Device connection. Refer to the *Configuring the USB0 Mode* section of this chapter for more information.
USB0_CPEN	73	O	LVTTL	USB0 over-current protection enable.
USB0_VBUS	81	I	5 V tolerant voltage sense	USB0 VBUS input. Allows USB PHY to sense if VBUS is present on the connector.

* I/O direction is with respect to the sbRIO-9651 SOM.

Configuring the USB0 Mode

You can configure the USB0 interface to be a USB Host port or a USB Device port, as shown in Table 1-6. This mode is set when the system boots and does not change dynamically. The reference carrier board uses the USB0 interface for a USB Device port.

Note USB On-The-Go (OTG) is not supported.

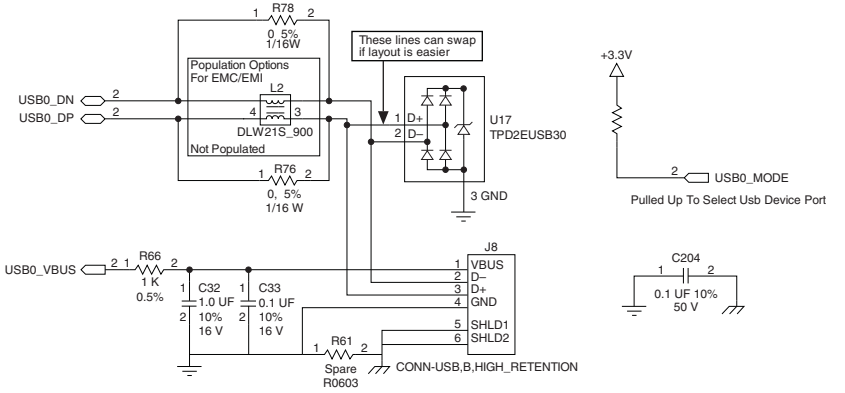
Table 1-6. Configuring the USB0 Mode

Mode	How to Enable
USB Host	Connect the USB0_MODE signal to digital ground on your carrier board. You can implement USB0 Host functionality in the same way that the USB1 Host signal is implemented on the reference carrier board, as described in the *USB1 Host Implementation on the Reference Carrier Board* section of this chapter.
USB Device	Connect the USB0_MODE signal to the VCC_3V3 rail on your carrier board. Refer to the *USB0 Device Implementation on the Reference Carrier Board* section of this chapter for more information about the USB0 Device implementation on the reference carrier board.

USB0 Device Implementation on the Reference Carrier Board

Figure 1-2 shows a schematic design for the USB0 Device implementation on the reference carrier board.

Figure 1-2. USB0 Device Reference Schematic



Reference Schematic Design Considerations

Table 1-7 lists design considerations for the schematic shown in Figure 1-2.

Table 1-7. USB0 Device Reference Schematic Design Considerations

Consideration	Notes
USB data pair	• The USB0_DP and USB0_DN data pair is routed differentially to the USB connector. • On the reference carrier board, the L2 common-mode choke is not populated, but you can populate it in your design to help with conducted immunity or emissions. • If you choose to populate L2, remove R76 and R78 from your design. • If your design does not include a common-mode choke, you can route the USB pair directly from the USB connector to the sbRIO-9651 SOM connector. • U17 provides ESD protection to the USB data pair and should be placed close to the USB connector.
USB0_MODE	The USB0_MODE signal is pulled up to 3.3 V to select USB Device functionality.
USB0_CPEN	Leave the USB0_CPEN signal disconnected for a USB Device port.
USB0_VBUS	• For the USB Device port to function properly, the USB0_VBUS signal must be connected to the VBUS pin on the USB connector. • This is a low-current, voltage-sense connection. • In layout, you can treat this connection as a data signal. • R66 helps provide some overvoltage protection on USB0_VBUS and should be placed close to the USB connector. NI recommends that you use a 1 kΩ resistor.

USB1 Host Signal Definitions

Table 1-8 describes the USB1 Host port pins and signals on the sbRIO-9651 SOM connector.

Table 1-8. USB1 Host Signal Definitions

Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
USB1_DP	35	I/O	Defined by USB specification.	USB1 data pair.
USB1_DN	43			

Table 1-8. USB1 Host Signal Definitions (Continued)

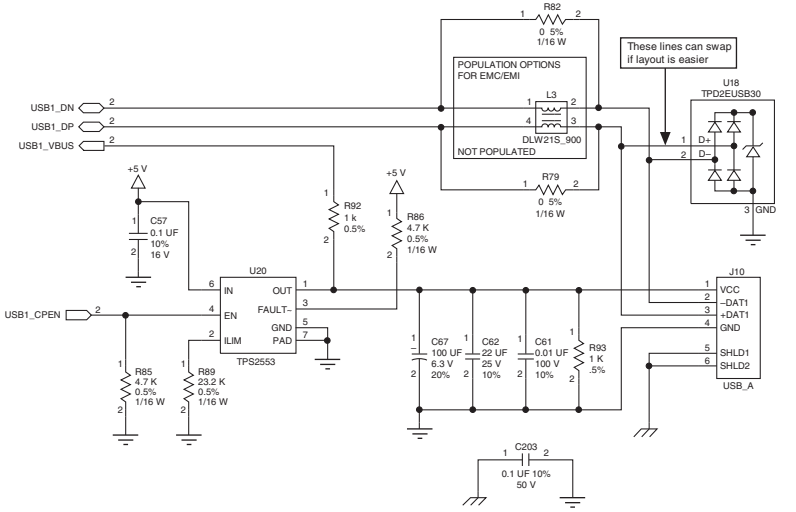
Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
USB1_CPEN	50	O	LVTTL	USB1 over-current protection enable.
USB1_VBUS	58	I	5 V tolerant voltage sense	USB1 VBUS input. Allows USB PHY to sense if VBUS is present on the connector.

* I/O direction is with respect to the sbRIO-9651 SOM.

USB1 Host Implementation on the Reference Carrier Board

Figure 1-3 shows a schematic design for the USB1 Host implementation on the reference carrier board.

Figure 1-3. USB1 Host Reference Schematic



Reference Schematic Design Considerations

Table 1-9 lists design considerations for the schematic shown in Figure 1-3.

Table 1-9. USB1 Host Reference Schematic Design Considerations

Consideration	Notes
USB data pair	• The USB1_DP and USB1_DN data pair is routed differentially to the USB connector. • On the reference carrier board, the L3 common-mode choke is not populated, but you can populate it in your design to help with conducted immunity or emissions. • If you choose to populate L3, remove R79 and R82 from your design. • If your design does not include a common-mode choke, you can route the USB pair directly from the USB connector to the sbRIO-9651 SOM connector. • U18 provides ESD protection to the USB data pair and should be placed close to the USB connector.
USB1_CPEN	The USB1_CPEN signal must be connected to the enable of the VBUS current limit switch (U20). This allows the sbRIO-9651 SOM to power-cycle USB devices when the processor is reset.
USB1_VBUS	• For the USB Host port to function properly, the USB1_VBUS signal must be connected to VBUS on the USB connector. • This is a low-current, voltage-sense connection. • In layout, you can treat the trace after R92 going to the sbRIO-9651 SOM connector as a data signal. • R92 helps provide some overvoltage protection on USB1_VBUS and should be placed close to the USB connector. NI recommends that you use a 1 kΩ resistor. • The carrier board must provide 5 V VBUS power for the USB Host port. • A current limit switch is required between the 5 V rail and the USB connector. • U20 is the current limiter. • NI recommends that you provide 100 µF of capacitance on the VBUS rail.

Supporting Onboard USB Devices

When you implement a USB device directly on your carrier board, you can connect the device to a USB Host port from the sbRIO-9651 SOM. For this case, use the following design guidelines:

- You can connect the USB data pair directly to a USB device on your carrier board.
- A current limiter is not required.
- Use the CARRIER_RST# signal to reset the USB device when the sbRIO-9651 SOM is in reset.
- Tie the USB*x*_VBUS signal to 3.3 V or 5 V.

USB Routing Considerations

NI recommends the following design practices for properly routing USB signals on your carrier board:

- Route the USB*x*_DP and USB*x*_DN signals as differential pairs with 90 Ω differential impedance.
- Length-match the positive and negative signal for each USB data pair to within 10 mils.
- Limit the USB*x*_DP and USB*x*_DN trace lengths on the carrier board to 8.0 in. or less, which is the length at which USB compliance was tested.

UART/Console Out (Serial1)

The sbRIO-9651 SOM provides a dedicated UART (Serial1) interface for use on a carrier board. This interface also functions as an operating system console when Console Out is enabled. Refer to the *Additional RS-232 (Serial2, Serial3, Serial4)* and *RS-485 (Serial5, Serial6)* sections of Chapter 2, *User-Defined FPGA Signals*, for information about implementing additional serial ports.

Serial1 Signal Definitions

Table 1-10 describes the Serial1 port pins and signals on the sbRIO-9651 SOM connector.

Note The NI-Serial driver has been developed for and tested with the Texas Instruments TRS3253EIRSMR RS-232 transceiver. Other transceivers may be compatible.

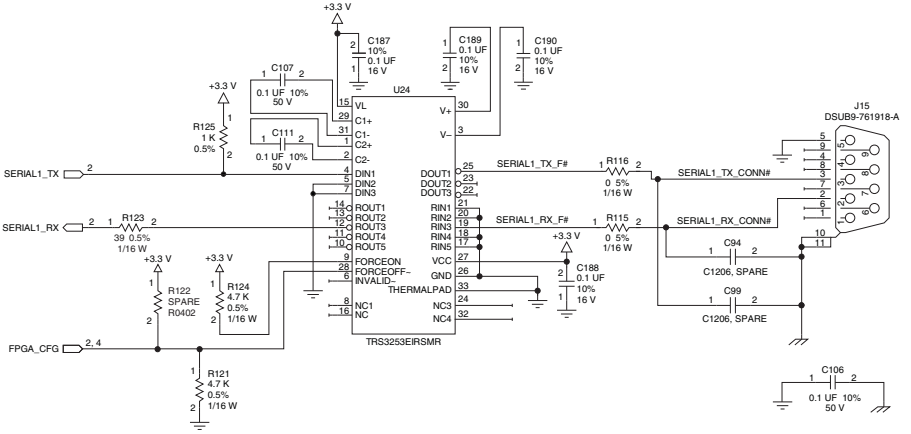
Table 1-10. Serial1 Signal Definitions

Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
SERIAL1_TX	52	O	LVTTL	Two-wire serial and console out signals for the sbRIO-9651 SOM.
SERIAL1_RX	60	I		
* I/O direction is with respect to the sbRIO-9651 SOM.				

Serial1 Implementation on the Reference Carrier Board

Figure 1-4 shows a schematic design for the Serial1 implementation on the reference carrier board.

Figure 1-4. Serial1 Reference Schematic



Reference Schematic Design Considerations

Table 1-11 lists design considerations for the schematic shown in Figure 1-4.

Table 1-11. Serial1 Reference Schematic Design Considerations

Consideration	Notes
Interface	The reference carrier board demonstrates how to use the Serial1 interface to implement a two-wire RS-232 serial port.
Serial transceiver	U24 is the RS-232 serial transceiver that converts between RS-232 and LVTTL signal levels. To minimize the impact of higher voltage signals on your carrier board, place the serial transceiver near the RS-232 connector.

Table 1-11. Serial1 Reference Schematic Design Considerations (Continued)

Consideration	Notes
Series termination	R123 is the series termination for SERIAL1_RX. Use series termination at the serial transceiver on all signals being driven to the sbRIO-9651 SOM. The sbRIO-9651 SOM provides onboard series termination for SERIAL1_TX near the Xilinx Zynq SoC.
FPGA	All serial port signals pass through the FPGA on the sbRIO-9651 SOM. The FPGA_CFG signal is used to disable the serial transceiver when the FPGA is not configured. Disabling the transceiver in this way prevents any unwanted glitches on the RS-232 port.

Adding Flow Control and Modem Control Signals

You can use the sbRIO CLIP Generator application included with the NI-RIO Device Drivers software to add optional flow control and modem control signals to the Serial1 interface.

Refer to the *Additional RS-232 (Serial2, Serial3, Serial4)* section of Chapter 2, *User-Defined FPGA Signals*, for an example of how to implement a full-modem RS-232 port. Refer to the *NI Single-Board RIO CLIP Generator Help*, described in the *Additional Documentation Resources* section of the *About This Document* preface, for more information about using the sbRIO CLIP Generator application.

SD Card

The sbRIO-9651 SOM provides a Secure Digital (SD) Card interface for use on a carrier board. This interface supports SD and SDHC cards. You can implement this interface with standard SD or microSD card connectors. The maximum supported SDHC card capacity is 32 GB.

SD Signal Definitions

Table 1-12 describes the SD pins and signals on the sbRIO-9651 SOM connector.

Table 1-12. SD Signal Definitions

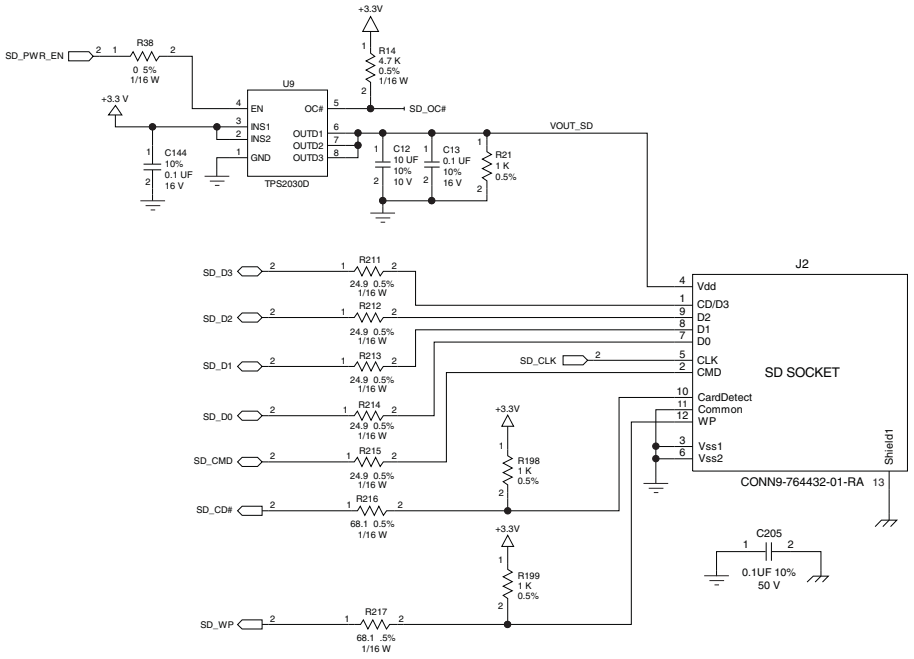
Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
SD_CLK	15	O	LVTTL	SD clock.
SD_CMD	31	I/O	LVTTL	SD command.
SD_D0 SD_D1 SD_D2 SD_D3	8 22 24 30	I/O	LVTTL	SD data bus.
SD_CD#	32	I	LVTTL	SD card detect. Assert low when card is present. Can connect to a mechanical switch in the SD card socket.
SD_WP	40	I	LVTTL	SD write protect. Assert high to enable protection. Can connect to a mechanical switch in the SD card socket.
SD_PWR_EN	38	O	LVTTL	Power enable for SD card socket.

* I/O direction is with respect to the sbRIO-9651 SOM.

SD Implementation on the Reference Carrier Board

Figure 1-5 shows a schematic design for the SD implementation on the reference carrier board.

Figure 1-5. SD Reference Schematic



Reference Schematic Design Considerations

Table 1-13 lists design considerations for the schematic shown in Figure 1-5.

Table 1-13. SD Reference Schematic Design Considerations

Consideration	Notes
SD_CLK, SD_CMD, and SD_D0 through SD_D3	• You can route these signals directly from the sbRIO-9651 SOM to the SD connector. • Each of these signals requires series termination near its driver. The sbRIO-9651 SOM provides series termination near the Xilinx Zynq SoC to prevent overshoot on the SD card when the sbRIO-9651 SOM drives these signals. The bi-directional signals also require series termination at the SD converter. • Use series termination at the SD connector for the SD_CMD and SD_D0 through SD_D3 signals to prevent overshoot on the sbRIO-9651 SOM when the SD card drives these signals.
SD_CD#	• The SD_CD# signal is connected to the mechanical card-detect switch in the SD connector. • When a card is inserted, the card-detect pin on the SD connector is shorted to ground. • Because this is a mechanical switch with low output impedance, you must place a series termination resistor (R216) at the SD connector. • You must have a card-detect switch to properly support hot-swapping cards. If you do not need to support hot-swapping cards, you can use an SD connector without a card-detect switch. In this case, tie the SD_CD# signal to ground so that the sbRIO-9651 SOM attempts to initialize a card on boot.

Table 1-13. SD Reference Schematic Design Considerations (Continued)

Consideration	Notes
SD_WP	• When the SD_WP signal is asserted high, the sbRIO-9651 will not write to the SD card. • Standard-size SD card connectors provide a mechanical write-protect switch that you can connect to the SD_WP signal. The switch detects the position of the lock slide on the SD card. • Because this is a mechanical switch with low output impedance, you must place a series termination resistor (R217) at the SD connector. • If you are using a microSD connector or do not have a write-protect switch, you can tie the SD_WP signal to ground in order to disable write protection and allow changes to the SD card.
SD_PWR_EN	• Use the SD_PWR_EN signal to gate power to the SD connector. • U9 acts as a power switch and current limiter for the SD interface. SDHC cards must not draw more than 200 mA. • The SD_PWR_EN signal controls when power is going to the SD card. • The SD_PWR_EN signal asserts high when a card is detected using the SD_CD# signal. The SD_PWR_EN signal deasserts when a card is not present.

SD Routing Considerations

NI recommends the following design practices for properly routing SD signals on your carrier board:

- Length-match the SD_CMD and SD_D0 through SD_D3 signals to within ±250 mils of SD_CLK.
- Limit the trace length of the SD_CLK, SD_CMD, and SD_D0 through SD_D3 signals on the carrier board to 8.0 in. or less.

RTC Battery (VBAT)

The reference carrier board contains a lithium cell battery that maintains the real-time clock (RTC) on the sbRIO-9651 SOM when the sbRIO-9651 SOM is powered off. A slight drain on the battery occurs when power is not applied to the sbRIO-9651 SOM. For information about the VBAT current drain, refer to the *VBAT Requirements* section of the *NI sbRIO-9651 System on Module OEM Device Specifications*.

If the battery is dead, or if no voltage has been applied to the VBAT pins, the system still starts but the system clock resets to the UNIX epoch date and time.

VBAT Signal Definitions

Table 1-14 describes the VBAT pins and signals on the sbRIO-9651 SOM connector.

Table 1-14. VBAT Signal Definitions

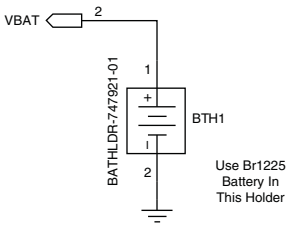
Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
VBAT	64	I	Power rail	RTC battery input that provides backup power to the RTC to keep track of absolute time.

* I/O direction is with respect to the sbRIO-9651 SOM.

VBAT Implementation on the Reference Carrier Board

Figure 1-6 shows a schematic design for the VBAT implementation on the reference carrier board.

Figure 1-6. VBAT Reference Schematic



Reference Schematic Design Considerations

You can directly connect the battery to VBAT. The sbRIO-9651 SOM already provides a current-limiting resistor and reverse-voltage protection.

Eliminating the Effects of Contact Bounce

If you are using the A revision of the sbRIO-9651 SOM, it is important to eliminate the effects of contact bounce when you initially attach the battery.

Note To determine the revision, check the bottom side of the sbRIO-9651 SOM for a sticker with the part number 157660*x*-01L, where *x* is the revision letter.

Contact bounce can cause a momentary power interruption to the RTC, which might result in drift greater than the RTC accuracy listed in the *NI sbRIO-9651 System on Module OEM Device Specifications*.

To eliminate the effects of contact bounce, try one of the following methods:

- (Preferred) Use power sequencing by applying Vcc to the RTC before attaching the battery.
- Filter the signal using a small capacitor between VBAT and ground. The manufacturer recommends capacitor values between 0.1 nf and 1.0 nf.

Resets

The sbRIO-9651 SOM provides signals for implementing a reset button on a carrier board and indicating that the sbRIO-9651 SOM is in reset.

Reset Signal Definitions

Table 1-15 describes the Reset pins and signals on the sbRIO-9651 SOM connector.

Table 1-15. Reset Signal Definitions

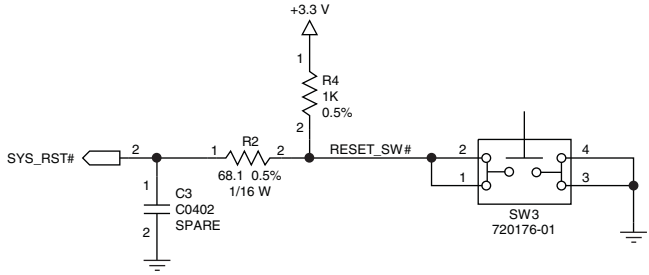
Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
CARRIER_RST#	37	O	LVTTL	Reset that indicates that main power is not adequate or that the sbRIO-9651 SOM is in reset. Asserted low.
SYS_RST#	47	I	LVTTL	System reset that puts the sbRIO-9651 SOM in reset. Asserted low. Asserting this signal causes the CARRIER_RST# signal to also assert. You can also assert this signal to put the sbRIO-9651 SOM into safe mode or reset IP address settings.

* I/O direction is with respect to the sbRIO-9651 SOM.

Reset Implementation on the Reference Carrier Board

Figure 1-7 shows a schematic design for the Reset implementation on the reference carrier board.

Figure 1-7. Reset Reference Schematic



Refer to the *SYS_RST#* and *CARRIER_RST#* sections of the *NI sbRIO-9651 System on Module OEM Device Specifications* for more information about the behavior of the Reset signals.

Reference Schematic Design Considerations

Table 1-16 lists design considerations for the schematic shown in Figure 1-7.

Table 1-16. Reset Reference Schematic Design Considerations

Consideration	Notes
Series termination	When SYS_RST# is driven, you must place a series termination resistor at the driver. When the driver is a mechanical switch, placing series termination is especially important due to the low output impedance of the switch.

Status LED

The sbRIO-9651 SOM provides a Status LED signal for use on a carrier board. The Status LED indicates the status of the SOM boot process or Safe Mode and can be used to report software errors.

Status LED Signal Definitions

Table 1-17 describes the Status LED pins and signals on the sbRIO-9651 SOM connector.

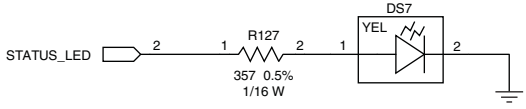
Table 1-17. Status LED Signal Definitions

Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
STATUS_LED	14	O	LVTTL	Status LED indicator.
* I/O direction is with respect to the sbRIO-9651 SOM.				

Status LED Implementation on the Reference Carrier Board

Figure 1-8 shows a schematic design for the Status LED implementation on the reference carrier board.

Figure 1-8. Status LED Reference Schematic



Refer to the *STATUS_LED* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for more information about the behavior of the Status LED signal.

FPGA Config

The sbRIO-9651 SOM provides an FPGA Config signal to indicate when the FPGA is configured.

FPGA Config Signal Definitions

Table 1-18 describes the FPGA Config pins and signals on the sbRIO-9651 SOM connector.

Table 1-18. FPGA Config Signal Definitions

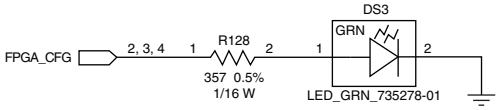
Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
FPGA_CFG	53	O	Refer to the *NI sbRIO-9651 System on Module OEM Device Specifications* for more information about the behavior of this signal.	FPGA Config Asserts when the FPGA is configured. Asserted high when the FPGA has been programmed.

* I/O direction is with respect to the sbRIO-9651 SOM.

FPGA Config Implementation on the Reference Carrier Board

Figure 1-9 shows a schematic design for the FPGA Config implementation on the reference carrier board.

Figure 1-9. FPGA Config Reference Schematic



Refer to the *FPGA_CFG* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for more information about the behavior of the FPGA Config signal.

Temp Alert

The sbRIO-9651 SOM provides a Temp Alert signal to indicate that the onboard CPU/FPGA or Primary System temperature has exceeded the minimum or maximum temperature specifications of the sbRIO-9651 SOM. Refer to the *Environmental* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for the minimum and maximum temperature specifications.

Temp Alert Signal Definitions

Table 1-19 describes the Temp Alert pins and signals on the sbRIO-9651 SOM connector.

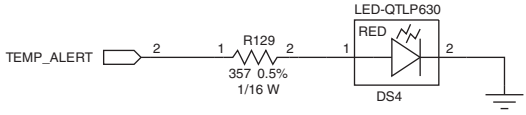
Table 1-19. Temp Alert Signal Definitions

Signal Name	Dedicated SOM Pin #	Direction*	I/O Standard	Description
TEMP_ALERT	46	O	LVTTL	Temp Alert indicator. Asserted high.
* I/O direction is with respect to the sbRIO-9651 SOM.				

Temp Alert Implementation on the Reference Carrier Board

Figure 1-10 shows a schematic design for the Temp Alert implementation on the reference carrier board.

Figure 1-10. Temp Alert Reference Schematic



Refer to the *TEMP_ALERT* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for more information about the behavior of the Temp Alert signal.

Refer to the *Validating Temperature Measurements* section of Chapter 4, *Mechanical Considerations*, for information about validating the system temperatures of your sbRIO-9651 SOM application.

2 User-Defined FPGA Signals

The sbRIO-9651 SOM connector provides several banks of FPGA pins that you can configure for purposes specific to your application. In addition to FPGA Digital I/O (DIO), you can use these pins to implement the following run-time peripheral interfaces:

- Secondary Ethernet (GBE1)
- Additional RS-232 (Serial2, Serial3, Serial4)
- RS-485 (Serial5, Serial6)
- CAN (CAN0, CAN1)

The reference carrier board included with the sbRIO-9651 SOM development kit shows an example of how to implement these signals. Refer to the specific sections in this chapter for more information about how the reference carrier board implements each signal.

Note To read or write to this I/O from a LabVIEW project, you must use the sbRIO CLIP Generator application to create a socketed component-level IP (CLIP) that defines the I/O configuration of the sbRIO-9651 SOM to use in your application. Refer to the *Getting Started with the NI sbRIO-9651 in LabVIEW* topic in the *LabVIEW Help* for more information about creating a CLIP.

Tip When you create your own CLIP, you must compile your FPGA VI and download it to the flash of the sbRIO-9651 SOM. This ensures that the driver for each enabled peripheral can load properly at boot time. Refer to the *Downloading an FPGA VI to the Flash Memory of an FPGA Target* topic in the *LabVIEW Help (FPGA Module)* for more information.

Secondary Ethernet (GBE1)

You must use specific FPGA pins to implement a secondary Ethernet port due to the strict timing requirements across semiconductor process and temperature variations.

The reference carrier board implements one secondary Ethernet port (GBE1) in addition to the primary Ethernet port. Refer to the *Primary Ethernet (GBE0)* section of Chapter 1, *Fixed Behavior Signals*, for more information about implementing a primary Ethernet port.

Note The sbRIO CLIP Generator enforces the selection of specific FPGA pins when you implement a secondary Ethernet port.

GBE1 Signal Definitions on the Reference Carrier Board

Table 2-1 describes the GBE1 pins and signals on the sbRIO-9651 SOM connector used to implement a secondary Ethernet port on the reference carrier board.

Table 2-1. GBE1 Signal Definitions

Signal Name	Pin #*	DIO Signal on Reference Carrier Board	Direction†	Description
TX Signals				
GBE1_GMII_GTX_CLK	192	DIO_62_N	O	Gigabit transmit clock.
GBE1_MII_TX_CLK	207	DIO_60_SRCC	I	10/100 transmit clock.
GBE1_GMII_TX_EN	215	DIO_60_N	O	Transmit enable.
GBE1_GMII_TX_ER	183	DIO_59	O	Transmit error.
GBE1_GMII_TX_D0 GBE1_GMII_TX_D1 GBE1_GMII_TX_D2 GBE1_GMII_TX_D3 GBE1_GMII_TX_D4 GBE1_GMII_TX_D5 GBE1_GMII_TX_D6 GBE1_GMII_TX_D7	235 227 211 203 187 179 234 242	DIO_49_N DIO_49 DIO_48_N DIO_48 DIO_47_N DIO_47 DIO_46_N DIO_46	O	Transmit data bus.
RX Signals				
GBE1_GMII_RX_CLK	231	DIO_61_MRCC	I	Receive clock.
GBE1_GMII_RX_DV	200	DIO_62_MRCC	I	Receive data valid.
GBE1_GMII_RX_ER	239	DIO_61_N	I	Receive error.

Table 2-1. GBE1 Signal Definitions (Continued)

Signal Name	Pin #*	DIO Signal on Reference Carrier Board	Direction†	Description
GBE1_GMII_RX_D0 GBE1_GMII_RX_D1 GBE1_GMII_RX_D2 GBE1_GMII_RX_D3 GBE1_GMII_RX_D4 GBE1_GMII_RX_D5 GBE1_GMII_RX_D6 GBE1_GMII_RX_D7	210 218 194 186 170 162 225 233	DIO_45_N DIO_45 DIO_44 DIO_44_N DIO_43 DIO_43_N DIO_42 DIO_42_N	I	Receive data bus.
Support Signals				
GBE1_GMII_COL	201	DIO_41	I	Collision detect.
GBE1_GMII_CRS	209	DIO_41_N	I	Carrier sense.
GBE1_MDC	177	DIO_40	O	MDIO clock, which needs to be pulled up on carrier board.
GBE1_MDIO	185	DIO_40_N	I/O	MDIO data, which needs to be pulled up on carrier board.
GBE1_IRQ#	191	DIO_59_N	I	PHY interrupt request, which should be pulled high on reference carrier board.

Table 2-1. GBE1 Signal Definitions (Continued)

Signal Name	Pin #*	DIO Signal on Reference Carrier Board	Direction†	Description
GBE1_SPEED_LEDg GBE1_SPEED_LEDy	126‡ 118‡	DIO_33 DIO_33_N	O	Speed LED signals: Yellow = 1000 Green = 100 Off = 10

* When you use the sbRIO CLIP Generator to enable secondary Ethernet, you must use the pins listed in this table. If you do not enable secondary Ethernet, you can use these pins for other FPGA DIO.

† I/O direction is with respect to the sbRIO-9651 SOM. I/O standards for these signals are defined in the sbRIO CLIP Generator.

‡ You can use any available FPGA DIO lines to implement these signals. In NI-RIO Device Drivers February 2015 or later, you can use the sbRIO CLIP Generator to assign FPGA DIO to these signals.

GBE1 Reference Schematic

Figure 2-1 shows a schematic design for the GBE1 implementation on the reference carrier board.

Figure 2-1. GBE1 Reference Schematic

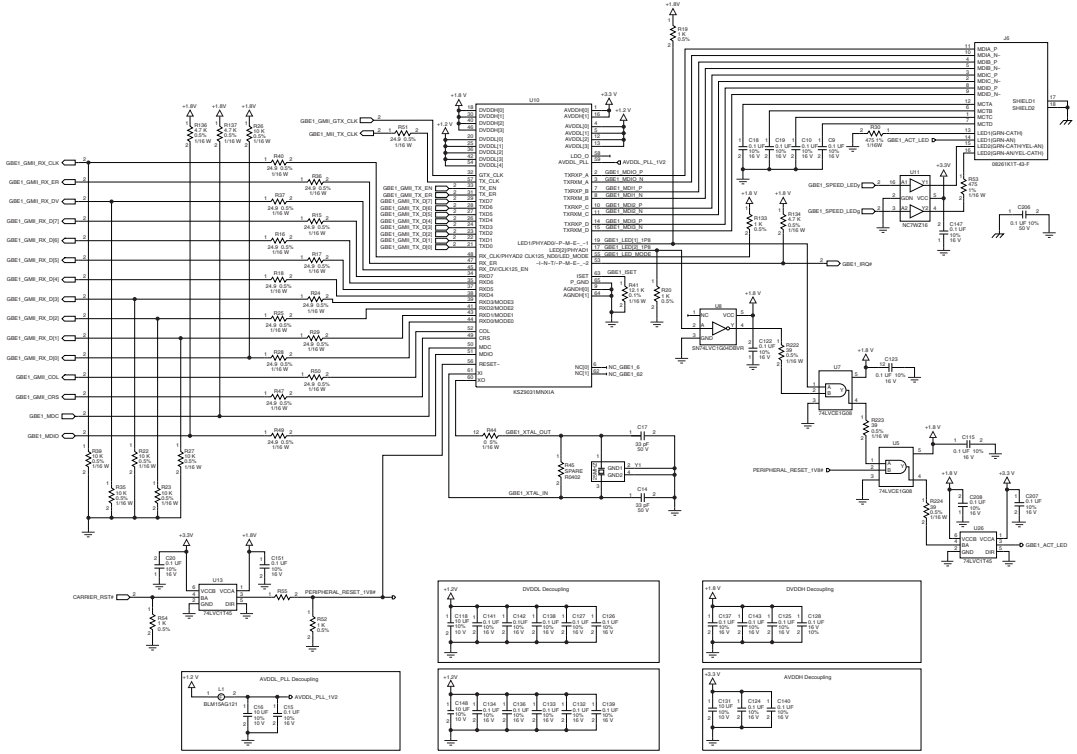
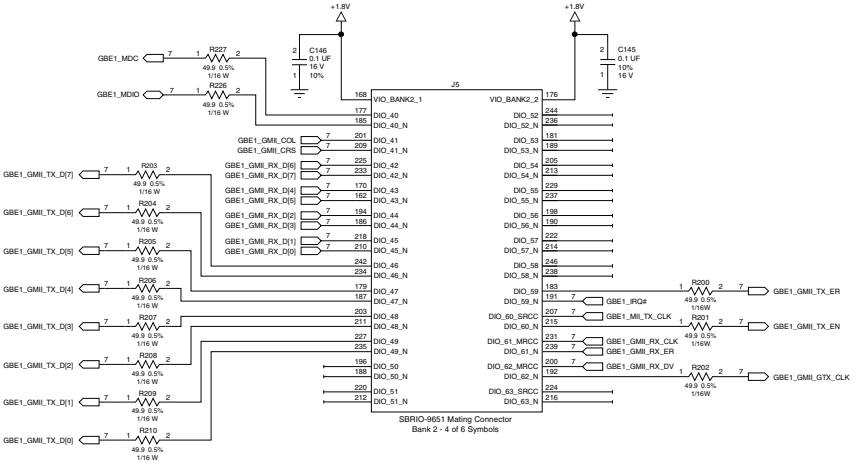


Figure 2-2 shows additional schematic details for the GBE1 TX signal series termination resistors at the SEARAY.

Figure 2-2. GBE1 TX Series Termination Reference Schematic



Reference Schematic Design Considerations

Table 2-2 lists design considerations for the schematics shown in Figures 2-1 and 2-2.

Table 2-2. GBE1 Reference Schematic Design Considerations

Consideration	Notes
Ethernet PHY selection	• The only PHY supported for secondary Ethernet is the Micrel Ethernet PHY, part number KSZ9031MNXIA. Refer to Table 1-4, *Gigabit Ethernet Connector Parts*, of Chapter 1, *Fixed Behavior Signals*, for information about the Gigabit Ethernet connector parts used in the sbRIO-9651 SOM development kit. • To meet GMII timing to the sbRIO-9651 SOM, the DIO bank for the PHY (DVDDH) and VIO_BANK2 on the sbRIO-9651 SOM must be powered at 1.8 V. • All pull-up and pull-down resistors connected to the PHY must be implemented in your carrier board design as shown in Figure 2-1. These connections ensure that the PHY is set up properly for sbRIO-9651 SOM software support. • Refer to the datasheet for the Micrel Ethernet PHY for more information about secondary Ethernet PHY requirements.
GMII TX signals	• Route the GMII TX signals directly to the Ethernet PHY. • To meet timing requirements, the TX signals must be 1.8 V logic. • You must place series termination resistors at the sbRIO-9651 SOM connector on the TX signals driving to the Ethernet PHY, as shown in Figure 2-2.
GMII RX signals	• Connect the GMII RX signals directly to the Ethernet PHY. • The pull resistors on the RX signals set options in the PHY when coming out of reset. • The pull resistors must be implemented in your carrier board design as shown in Figure 2-1 to ensure that secondary Ethernet works properly. The resistors must be the same values shown in Figure 2-1. • You must place series termination resistors near the Ethernet PHY on all RX signals, as shown in Figure 2-1.
PHY crystal selection	• NI recommends that you use a crystal with the Ethernet PHY. • The crystal must be 25 MHz with 50 ppm or better accuracy. • Ensure that you use suitable load capacitors for your crystal.

Table 2-2. GBE1 Reference Schematic Design Considerations (Continued)

Consideration	Notes
MDI data pairs	• The MDI data pairs are connected directly to the Ethernet connector. • Route the MDI data pairs differentially from the PHY to the connector. • The Ethernet connector has magnetics built into it. You may use discrete magnetics instead.
Magnetic selection	Refer to the *Gigabit Ethernet Magnetic Requirements* section of Chapter 1, *Fixed Behavior Signals*, for information about magnetic requirements.
Ethernet speed LEDs	Refer to the *Ethernet Speed LED Behavior* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for information about Ethernet LED signal behavior and rated drive current.
Ethernet link activity LEDs	Figure 2-1 shows the logic required to create the same link activity LED behavior that the primary Ethernet signal uses.
GBE1 support signals listed in Table 2-1	Connect these signals as shown in Figure 2-1.
CARRIER_RST#	The CARRIER_RST# signal should control the Ethernet PHY reset. Because the PHY has 1.8 V I/O, including the reset input, and the CARRIER_RST# signal is a 3.3 V signal, level translation is required to connect the CARRIER_RST# signal to the PHY. U13 provides this translation in Figure 2-1.

GBE1 Routing Considerations

NI recommends the following design practices for properly routing GBE1 signals on your carrier board:

- Length-match GMII TX signals to within ±250 mils of the GBE1_GMII_GTX_CLK signal.
- Length-match GMII RX signals to within ±250 mils of the GBE1_GMII_RX_CLK signal.
- Limit the overall length of GMII TX and RX signals to 5.0 in. or less.
- Route MDI pairs differentially with 100 Ω differential trace impedance.
- Length-match the positive and negative signal for each MDI data pair to within 10 mils.
- Limit the MDI trace lengths to 6.0 in. or less, which is the length at which Ethernet compliance was tested.

Additional RS-232 (Serial2, Serial3, Serial4)

You can use any FPGA pins to implement additional RS-232 ports.

The reference carrier board implements one secondary RS-232 port (Serial2) in addition to the primary UART/Console Out port. You can implement additional RS-232 ports (Serial3 and Serial4) in the same way that the Serial1 signal is implemented on the reference carrier board. Refer to the *UART/Console Out (Serial1)* section of Chapter 1, *Fixed Behavior Signals* for more information about implementing the primary UART/Console Out port.

Serial2 Signal Definitions on the Reference Carrier Board

Table 2-3 describes the Serial2 pins and signals on the sbRIO-9651 SOM connector used to implement an additional RS-232 port on the reference carrier board.

Note The NI-Serial driver has been developed for and tested with the Texas Instruments TRS3253EIRSMR RS-232 transceiver. Other transceivers may be compatible.

Table 2-3. Serial2 Signal Definitions

Signal Name	Pin #*	DIO Signal on Reference Carrier Board	Direction†	Description
SERIAL2_TX	66	DIO_0	O	Full-modem RS-232 serial port signals.
SERIAL2_RX	69	DIO_7	I	
SERIAL2_RTS#	74	DIO_1	O	
SERIAL2_CTS#	76	DIO_6	I	
SERIAL2_DTR#	59	DIO_2	O	
SERIAL2_DSR#	83	DIO_4	I	
SERIAL2_DCD#	75	DIO_3	I	
SERIAL2_RI#	68	DIO_5	I	

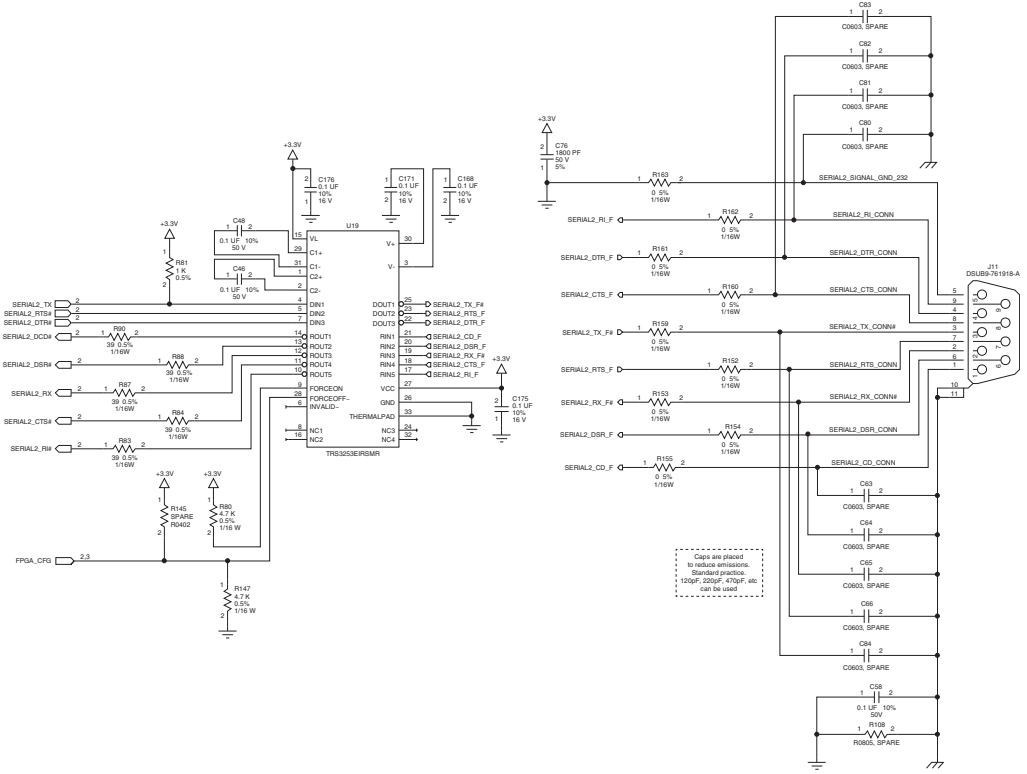
* The pin numbers listed in this table are the pins used on the reference carrier board. For your carrier board design, you can use the sbRIO CLIP Generator to configure these pins for any FPGA DIO.

† I/O direction is with respect to the sbRIO-9651 SOM. I/O standards for these signals are defined in the sbRIO CLIP Generator.

Serial2 Reference Schematic

Figure 2-3 shows a schematic design for the Serial2 implementation on the reference carrier board.

Figure 2-3. Serial2 Reference Schematic



Reference Schematic Design Considerations

Table 2-4 lists design considerations for the schematic shown in Figure 2-3.

Table 2-4. Serial2 Reference Schematic Design Considerations

Consideration	Notes
Interface	The reference carrier board demonstrates how to use the Serial2 interface to implement a null-modem RS-232 serial port.
Serial transceiver	U19 is the RS-232 serial transceiver that converts between RS-232 and LVTTL signal levels. To minimize the impact of higher voltage signals on your carrier board, place the serial transceiver near the RS-232 connector.
Series termination	• R83, R84, R87, R88, and R90 are the series termination for Serial2. Use series termination at the serial transceiver on all signals being driven to the sbRIO-9651 SOM. • FPGA DIO signals from DIO Bank 0 include series termination on the sbRIO-9651 SOM. Use series termination at the SEARAY connector on all signals outside of Bank 0 being driven from the sbRIO-9651 SOM to the serial transceiver.
FPGA	All serial port signals pass through the FPGA on the sbRIO-9651 SOM. The FPGA_CFG signal is used to disable the serial transceiver when the FPGA is not configured. Disabling the transceiver in this way prevents any unwanted glitches on the RS-232 port.

RS-485 (Serial5, Serial6)

You can use any FPGA pins to implement an RS-485 port.

The reference carrier board implements one RS-485 port (Serial5). You can implement an additional RS-485 port (Serial6) in the same way that the Serial5 signal is implemented on the reference carrier board.

Serial5 Definitions on the Reference Carrier Board

Table 2-5 describes the Serial5 pins and signals on the sbRIO-9651 SOM connector used to implement an RS-485 port on the reference carrier board.

Note The NI-Serial driver has been developed for and tested with the Analog Devices ADM2587EBRWZ Isolated RS-485 transceiver. Other isolated and non-isolated transceivers may be compatible.

Table 2-5. Serial5 Signal Definitions

Signal Name	Pin #*	DIO Signal on Reference Carrier Board	Direction†	Description
SERIAL5_TX	70	DIO_11	O	Isolated RS-485 interface signals.
SERIAL5_TX_EN	78	DIO_12	O	
SERIAL5_RX	79	DIO_14	I	
SERIAL5_RX_EN	87	DIO_15_MRCC	O	

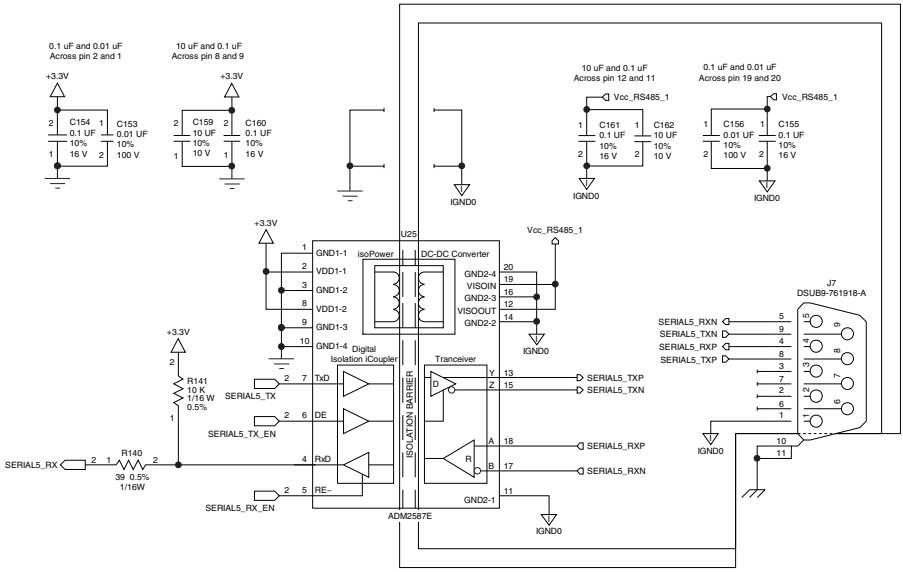
* The pin numbers listed in this table are the pins used on the reference carrier board. For your carrier board design, you can use the sbRIO CLIP Generator to configure these pins for any FPGA DIO.

† I/O direction is with respect to the sbRIO-9651 SOM. I/O standards for these signals are defined in the sbRIO CLIP Generator.

Serial5 Reference Schematic

Figure 2-4 shows a schematic design for the Serial5 implementation on the reference carrier board.

Figure 2-4. Serial5 Reference Schematic



Reference Schematic Design Considerations

Table 2-6 lists design considerations for the schematic shown in Figure 2-4

Table 2-6. Serial5 Reference Schematic Design Considerations

Consideration	Notes
Interface	The reference carrier board demonstrates how to use the Serial5 interface to implement an isolated RS-485 serial port.
Serial transceiver	U25 is the RS-485 serial transceiver that converts between RS-485 and LVTTL signal levels. This transceiver provides functional isolation of the RS-485 signals to prevent ground loops from affecting the RS-485 signals.
Series termination	• R140 is the series termination for Serial5. Use series termination at the serial transceiver on all signals being driven to the sbRIO-9651 SOM. • FPGA DIO signals from DIO Bank 0 include series termination on the sbRIO-9651 SOM. Use series termination at the SEARAY connector on all signals outside of Bank 0 being driven from the sbRIO-9651 SOM to the serial transceiver.

RS-485 Layout Considerations

Pay close attention to how the ground planes are arranged under the isolated RS-485 transceiver. Isolated and non-isolated ground planes overlap across layers to provide some capacitance between the grounds and help with EMC. Refer to the datasheet for the RS-485 transceiver for more information.

CAN (CAN0, CAN1)

You can use any FPGA pins to implement a CAN interface port.

The reference carrier board implements one CAN port (CAN0). You can implement an additional CAN port (CAN1) in the same way that the CAN0 signal is implemented on the reference carrier board.

CAN0 Signal Definitions on the Reference Carrier Board

Table 2-7 describes the CAN0 pins and signals on the sbRIO-9651 SOM connector used to implement a CAN interface port on the reference carrier board.

Note The NI-Embedded CAN driver has been developed for and tested with the NXP PCA82C251T/YM CAN transceiver. Other transceivers may be compatible.

Table 2-7. CAN0 Signal Definitions

Signal Name	Pin #*	DIO Signal on Reference Carrier Board	Direction†	Description
CAN0_TX	85	DIO_8	O	Transmit line.
CAN0_RX	54	DIO_9	I	Receive line.
CAN0_RS	62	DIO_10	O	Slope control and standby.

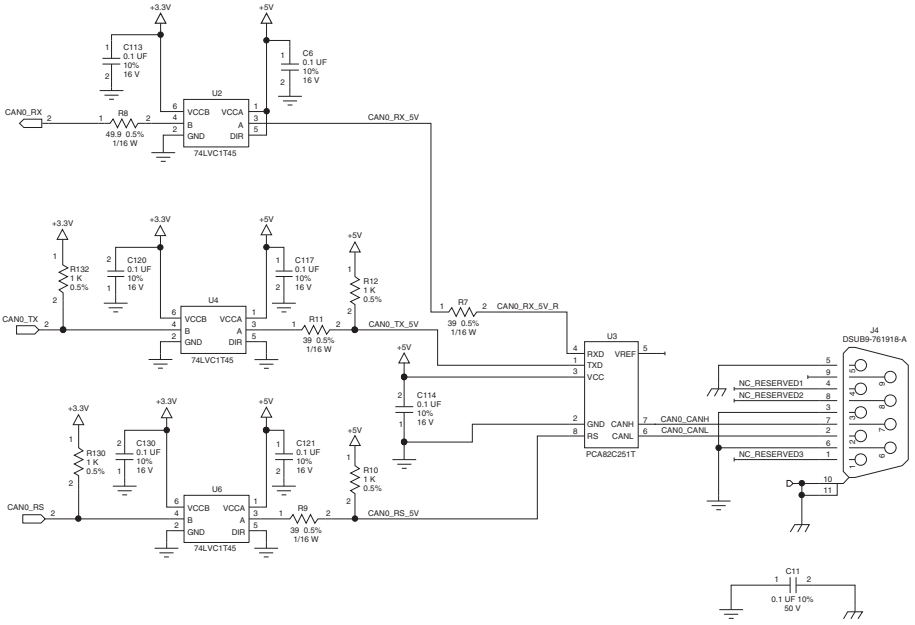
* The pin numbers listed in this table are the pins used on the reference carrier board. For your carrier board design, you can use the sbRIO CLIP Generator to configure these pins for any FPGA DIO.

† I/O direction is with respect to the sbRIO-9651 SOM. I/O standards for these signals are defined in the sbRIO CLIP Generator.

CAN0 Reference Schematic

Figure 2-5 shows a schematic design for the CAN0 implementation[1] on the reference carrier board.

Figure 2-5. CAN0 Reference Schematic



[1] The NXP PCA82C251T CAN transceiver requires 5 V logic levels. The reference carrier board uses external discrete buffers to translate 3.3 V FPGA lines to 5 V logic levels.

Reference Schematic Design Considerations

Table 2-8 lists design considerations for the schematic shown in Figure 2-5

Table 2-8. CAN0 Reference Schematic Design Considerations

Consideration	Notes
CAN*x*_RX, CAN*x*_TX, and CAN*x*_RS	• The recommended CAN transceiver requires 5 V I/O. • U2, U4, and U6 provide level translation between the 3.3 V I/O on the sbRIO-9651 SOM and the 5 V I/O on the transceiver. Use caution when implementing this level translation. • The TXD and RS inputs of the CAN transceiver must remain high during power-down and power-up of the sbRIO-9651 SOM and carrier board. This prevents glitches on the CAN bus that might disrupt communication between other devices on the bus. The level translator IC in this schematic prevents these glitches. • The level translator output remains at high impedance until both of its power supply rails are powered to allow the 5 V power supply to power-up before the 3.3 V power supply. • All signals have series termination at the outputs to prevent over- or under-shoot at the receivers. • FPGA DIO signals from DIO Bank 0 include series termination on the sbRIO-9651 SOM. Use series termination at the SEARAY connector on all signals outside of Bank 0 being driven from the sbRIO-9651 SOM to the CAN transceiver.
CAN*x*_CANH and CAN*x*_CANL	• Route these signals differentially with a 120 Ω differential trace impedance. • Minimize the overall length of the traces so that you can place termination resistors in the CAN cabling as close as possible to the CAN transceiver. • Depending on your design requirements, you can also place the CAN termination resistor on the carrier board.

Termination Resistors for CAN Cables

The termination resistors should match the nominal impedance of the CAN cable and therefore comply with the values in Table 2-9.

Table 2-9. Termination Resistor Specification

Characteristic	Value	Condition
Termination resistor	100 Ω minimum 120 Ω nominal 130 Ω maximum	Minimum power dissipation: 220 mW

3

Carrier Board PCB Layout Guidelines

Use the guidelines in this chapter to help you arrange the I/O signals you implement in your carrier board design.

Impedance-Controlled Signaling

Use the following guidelines for implementing impedance for all I/O signals:

- All signals connected to the sbRIO-9651 SOM must use impedance-controlled traces. Refer to the sections of this document listed in Table 3-1 for information about impedance requirements.

Table 3-1. Impedance Requirements Resources

Impedance Requirement	Resource
General requirements for single-ended signals	*Single-Ended Signal Best Practices* section of this chapter
General requirements for differential signals	*Differential Signal Best Practices* section of this chapter
Signal-specific requirements	Signal-specific sections in Chapter 1, *Fixed Behavior Signals*, or Chapter 2, *User-Defined FPGA Signals*

- Trace geometry to meet impedance requirements vary depending on your specific carrier board PCB stack-up. Collaborate with your vendor to match impedance requirements, stack-up, and trace geometry appropriate for your application.
- To properly maintain trace impedance and avoid discontinuities, you cannot route traces over gaps in the reference plane. Use stitching vias and capacitors when appropriate near layer changes to provide a transient return path between reference planes.

Single-Ended Signal Best Practices

Use the following guidelines for implementing single-ended I/O signals:

- Route all single-ended signals that are implemented on your carrier board and connected to the sbRIO-9651 SOM with 50 Ω characteristic trace impedance.
- Maintain at minimum a 2 × *H* line spacing between single-ended traces, where *H* is the distance in the board stack-up from the trace to its reference plane.
- When you configure FPGA DIO signals from DIO Bank 1, 2, or 3 as single-ended traces, observe the following guidelines:
  - Use the DIO_*x* positive signals first because those signals have slightly lower crosstalk in the J1 connector on the sbRIO-9651 SOM than the DIO_*x* negative (DIO_*x*_N) signals.
  - To minimize crosstalk when using the DIO_*x*_N signals, ensure that you implement corresponding positive and negative signals in the same direction. For example, if you are using DIO_16 and DIO_16_N, implement both signals as inputs or both as outputs. Avoid implementing one as an input and the other as an output.
  - To improve signal integrity on the carrier board, place series termination resistors on outputs from the sbRIO-9651 SOM as close to the mating connector as possible.

Note FPGA DIO signals from DIO Bank 0 include series termination resistors near the Xilinx Zynq SoC on the sbRIO-9651 SOM. Refer to the *FPGA DIO* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for more information.

Differential Signal Best Practices

Use the following guidelines for implementing differential I/O signals:

- Route all differential signals that are implemented on your carrier board and connected to the sbRIO-9651 SOM—other than USB data pair signals—with 100 Ω differential trace impedance. Route USB data pair signals with 90 Ω differential trace impedance.
- Maintain at minimum a 3 × *H* spacing between differential pairs and any other copper features on the same layer, where *H* is the distance in the board stack-up from the trace to its reference plane.

Ground and Power Plane Recommendations

Use the following guidelines for implementing ground and power planes:

- You must include ground planes on your carrier board. All GND pins on the J1 connector of the sbRIO-9651 SOM must connect to the carrier board ground planes.
- If possible, use planes to connect power to the sbRIO-9651 SOM. All power pins on the J1 connector of the sbRIO-9651 SOM must be connected and powered, even if a bank of DIO is unused.

Fanout and Layout Options

Refer to Samtec SEARAY documentation for information about possible fanout and layout options with various layer count carrier boards.

4

Mechanical Considerations

Proper mechanical design is critical for rugged environments in which the sbRIO-9651 SOM may be subjected to extreme temperatures, shock, vibration, and other factors. In particular, pay special attention to thermal performance to ensure that your application meets the sbRIO-9651 SOM operating requirements.

Mounting

You can mount the sbRIO-9651 SOM and carrier board in a variety of ways in order to maximize system performance. Some mounting methods might require custom fasteners or unique assembly techniques to maintain required connector stack heights and enable improved thermal and structural design for rugged environments.

Selecting an Appropriate Mating Connector

The J1 connector on the sbRIO-9651 SOM is a Molex 45971-4185 320-pin, 8 × 40 position, SEARAY open-pin-field-array connector. To interface with the J1 connector, your carrier board design must implement a mating connector that is compatible with the Molex 45971 series or Samtec SEAF series. Table 4-1 lists compatible mating connectors, such as the Molex 45970 series or Samtec SEAM series.

Table 4-1. sbRIO-9651 SOM Connector and Compatible Mating Connectors

Connector	Manufacturer, Part Number
sbRIO-9651 SOM J1 connector	Molex, 45971-4185 (equivalent to Samtec SEAF-40-05.0-S-08-2-A-K-TR)
Recommended mating connector*	Molex, 45970-4130
Alternative 7-mm stack height mating connectors	Molex, 45970-4185 Samtec, SEAM-40-02.0-S-08-2-A-K-TR

* Compatible connectors are available in multiple stack height and termination options. NI has secured a special Molex connector part number, 45970-4130, with a 7-mm mated pair stack height. Refer to the *Ordering the Recommended Mating Connector* section of this chapter for information about ordering connectors. Consult Molex or Samtec for alternative stack heights and terminations.

Ordering the Recommended Mating Connector

The recommended mating connector is distributed through TTI, Inc. at NI-negotiated pricing and with shortened lead times. Complete the following steps to order individual bulk or reel quantities of the mating connector.

1. Visit www.ttiinc.com.
2. Search for the 45970-4130 part number. Table 4-2 describes the available parts.
3. Contact TTI, Inc. directly and request NI pricing when obtaining a quote. You may also be able to place an order directly from the TTI, Inc. website.

Table 4-2. Orderable Mating Connector Parts from TTI, Inc.

Part Number	Description
45970-4130	A packaged reel of 300 connectors.
45970-4130 BULK	One or more individual connectors.

Note These recommended connectors are available only from TTI, Inc. distribution centers located in the United States but can be shipped internationally. Customers outside the U.S. should contact a U.S.-based distribution center and request international shipping.

Note Online pricing might not reflect negotiated pricing.

Selecting Appropriate Standoffs

The Molex 45970 series and Samtec SEAM series connectors are available in multiple heights. The height of the mating connector you select determines the height of the standoffs you need.

To prevent over-insertion, the SEARAY connector design requires that standoffs never be less than the stack height. Because standard nominal tolerances might result in a standoff being shorter than the stack height, NI requires that you use standoffs that are 0.15 mm (0.006 in.) taller than the combined height of the J1 connector on the sbRIO-9651 SOM and the mating SEARAY connector. Therefore, to determine the required standoff height, you must add the heights of the mated connectors plus an additional 0.15 mm (0.006 in.). Refer to Samtec documentation for more information about SEARAY standoff requirements.

Table 4-3 provides an example standoff height calculation using a Molex 45970-4130 mating connector.

Table 4-3. Example Connector Configuration and Calculated Standoff Height

Component	Manufacturer, Part Number	Height
J1 connector on the sbRIO-9651 SOM	Molex, 45971-4185	5.00 mm (0.197 in.)
Mating connector	Molex, 45970-4130	2.00 mm (0.079 in.)
Required additional standoff height	—	0.15 mm (0.006 in.)
Total calculated standoff height	—	**7.15 mm (0.281 in.)**

NI Custom Standoffs

NI offers a custom standoff that is an exact fit with the recommended or other compatible 7-mm stack height mating connectors listed in Table 4-1. This custom M3 × 7.15 mm (0.281 in.) is made from 4.5 mm (0.177 in.) stainless steel hex stock and includes a nylon threadlock patch. The external threads extend 4.78 mm (0.188 in.) and the internal threads are 5 mm (0.197 in.) deep. Table 4-4 lists orderable quantities of this custom standoff.

Table 4-4. Custom M3 × 7.15 mm (0.281 in.) Standoff Kits

Quantity	Manufacturer, Part Number
20	NI, 157543-020
500	NI, 157543-500

NI recommends that you use stainless steel fasteners for good corrosion resistance and strength. Tighten M3 fasteners to a torque of 0.76 N · m (6.70 lb · in), unless otherwise noted or required by your specific design constraints.

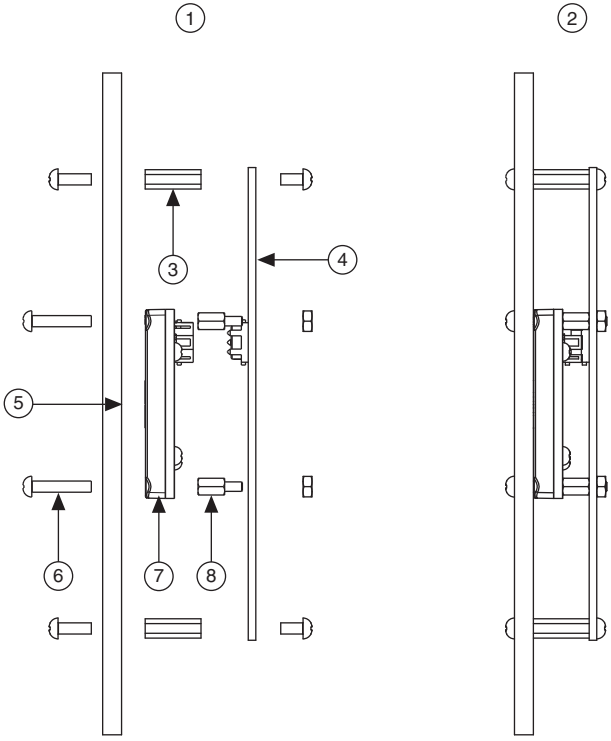
Mounting Direction Options

Figures 4-1 through 4-3 show possible mounting configurations and associated fastener types.

Mounting on a Panel or Plate (Recommended)

If possible, NI recommends that you mount the sbRIO-9651 SOM on a panel or plate, as shown in Figure 4-1.

Figure 4-1. Mounting on a Panel or Plate



1	Exploded view of all mounting components	5	Mounting surface
2	Complete assembled and mounted view	6	Mounting screw, panel thickness + 12.00 mm (0.472 in.)
3	Standoff, 15.00 mm (0.591 in.)	7	sbRIO-9651 SOM
4	Carrier board	8	Standoff, 7.15 mm (0.281 in.)

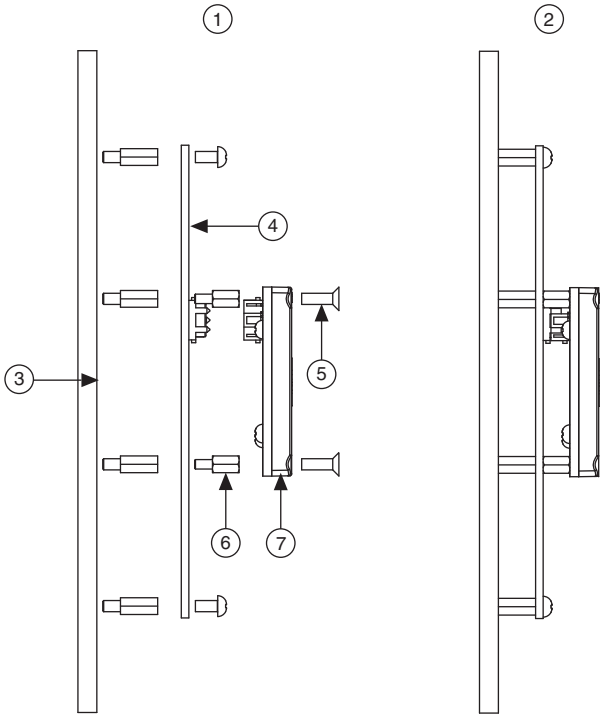
The sbRIO-9651 SOM was designed so that you can use the 15.00 mm (0.591 in.) standoffs between the carrier board and the base panel when the 7.15 mm (0.281 in.) standoffs are used between the carrier board and the sbRIO-9651 SOM, as shown in Figure 4-1.

This method accommodates a layer of thermal grease that is 0.08 mm (0.003 in.) thick between the aluminum heat spreader of the sbRIO-9651 SOM and the metal base panel. However, thicker thermal interface materials may require different lengths of standoffs or mounting bosses. The direction of fastening may also require custom lengths or types of fasteners and might impact ease of assembly.

Mounting on a Panel or Plate with Flathead Screws

Alternatively, use flathead screws when mounting on a panel or plate, as shown in Figure 4-2.

Figure 4-2. Mounting on a Panel or Plate with Flathead Screws

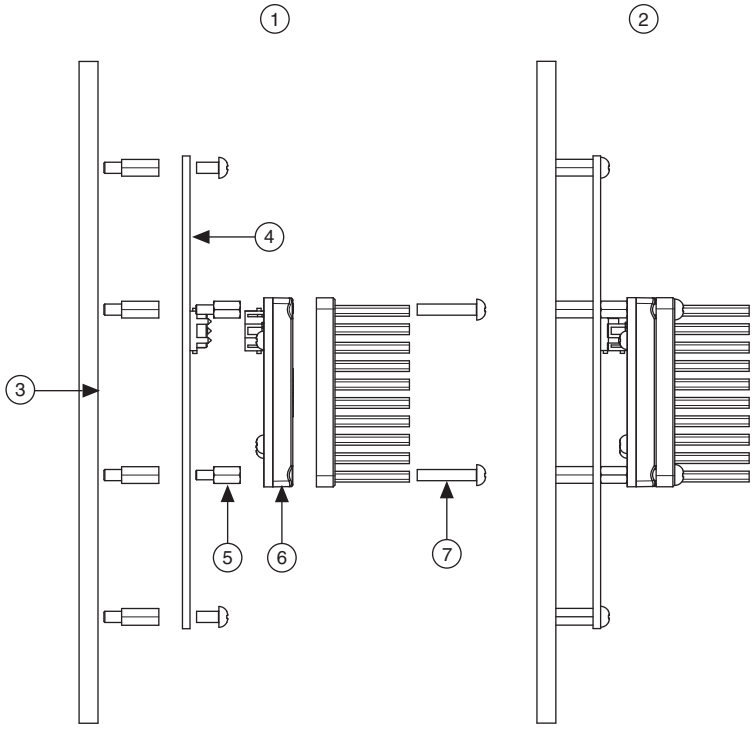


1	Exploded view of all mounting components	5	Mounting screw, 12.00 mm (0.472 in.)
2	Complete assembled and mounted view	6	Standoff, 7.15 mm (0.281 in.)
3	Mounting surface	7	sbRIO-9651 SOM
4	Carrier board		

Mounting on a Panel or Plate with an Attached Heat Sink

Your system design might require you to attach a heat sink or other thermal solution described in the *Mounting Recommendations for Maximizing Thermal Performance* section of this chapter. Figure 4-3 shows standoffs and fasteners that are compatible with the AlphaNovatech S01LZZ0E-A heat sink that is included in the sbRIO-9651 SOM development kit.

Figure 4-3. Mounting on a Panel or Plate with an Attached Heat Sink



1	Exploded view of all mounting components	5	Standoff, 7.15 mm (0.281 in.)
2	Complete assembled and mounted view	6	sbRIO-9651 SOM
3	Mounting surface	7	Mounting screw, 16.00 mm (0.630 in.)
4	Carrier board		

Managing Thermal Conditions

Due to the compact size of the sbRIO-9651 SOM, it is very important to appropriately dissipate the heat generated during operation. You must plan for the thermal conditions of your application throughout development and validation. This section provides design recommendations and validation tools and methods for maximizing the thermal performance of the system.

Designing a Suitable Enclosure

NI sbRIO devices operate as components in a higher-level system and may require an enclosure to protect the internal circuit card assembles and dissipate heat. For the sbRIO-9651 SOM, the system integrator is responsible for designing an enclosure that meets the thermal requirements of your specific application.

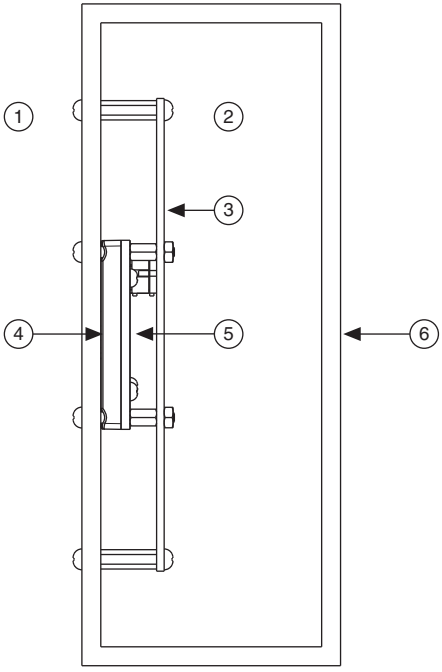
NI sbRIO devices integrated into an enclosure or system with proper thermal dissipation can be deployed in high- and low-temperature environments. However, the 85 °C local ambient operating temperature rating of the sbRIO-9651 SOM does not mean that the external temperature of the natural convection environment such as a room or larger enclosure can be 85 °C. In this way, properly designed NI sbRIO devices may still require an external ambient temperature of 70 °C or less and may still require specific mounting requirements to ensure that the local ambient and thermally-relevant component maximum operating temperatures are within specification.

Understanding Thermal Specifications

A deployed system has several temperature measurement locations that indicate the thermal performance of the system and the devices the system contains. For example, in a natural convection system, the temperature of a critical component will be higher than the temperature of the air in the immediate vicinity of the component. This local air temperature will also be higher inside an enclosure than in the room ambient that surrounds the enclosure.

Figure 4-4 identifies these types of ambient temperatures.

Figure 4-4. Ambient Temperatures



1	External ambient temperature	4	sbRIO-9651 SOM
2	Internal/enclosure ambient temperature	5	Local ambient temperature
3	Carrier board	6	Enclosure

- **External ambient**—The maximum air temperature of the room or installation location that surrounds the system.
- **Internal/enclosure ambient**—The maximum air temperature inside the enclosure. This can be measured at various locations within the enclosure and is highly influenced by the proximity and dissipation of devices inside the enclosure.
- **Local ambient**—The maximum air temperature as specified directly adjacent to the NI sbRIO device. This is measured on all sides of a device that has exposed circuitry. Because the sbRIO-9651 SOM has an integrated heat spreader on the primary side, only the secondary side needs to be measured.

Because the system integrator may use any number of enclosure sizes, materials, thermal solutions, and room conditions when designing an enclosure for a specific application, NI sbRIO devices are specified in a manner that removes most of these external variables. Therefore, the sbRIO-9651 SOM thermal performance is not determined by measuring the external ambient or internal/enclosure ambient temperatures, but by measuring the local ambient and specific component temperatures. NI provides digitally reported temperatures to help you accurately measure these critical temperatures.

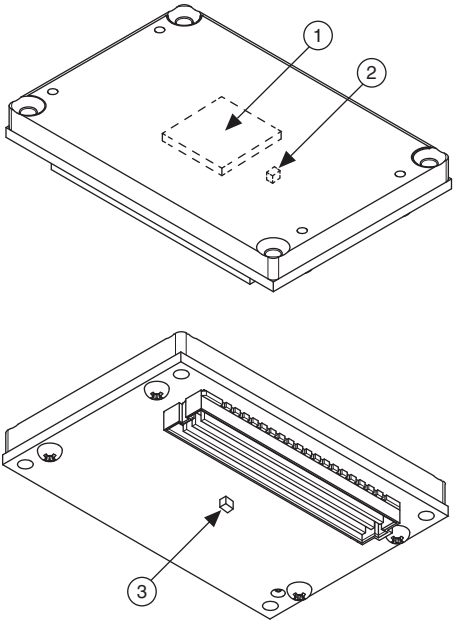
Validating the System

NI recommends that you use a validation system for an extended period of time in a test environment with the same thermal, environmental, and functional utilization characteristics as the target deployment environment. You are responsible for final validation of your application.

Validating Temperature Measurements

The sbRIO-9651 SOM includes three onboard temperature-monitoring sensors to simplify validation of a thermal solution, as shown in Figure 4-5. The sensors provide an indication of thermal performance and are used to validate the system along with the local ambient operating temperature.

Figure 4-5. Onboard Temperature-Monitoring Sensors



1	CPU/FPGA sensor	2	Primary System sensor	3	Secondary System sensor

- **CPU/FPGA sensor**—Digitally reports the die junction temperature of the Xilinx Zynq SoC.
- **Primary System sensor**—Digitally reports the temperature on the Xilinx Zynq SoC side of the circuit card assembly underneath the integrated heat spreader. This value is an approximation of the local ambient temperature inside the heat spreader.
- **Secondary System sensor**—Digitally reports the temperature on the SEARAY side of the circuit card assembly. This value is a conservative approximation of the local ambient temperature on that side of the circuit card assembly.

To meet the thermal specifications described in the *NI sbRIO-9651 System on Module OEM Device Specifications*, you must record the following measurements:

- The CPU/FPGA reported temperature, which must not exceed 98 °C
- The Primary System reported temperature, which must not exceed 85 °C
- The local ambient operating temperature near the device, which must not exceed 85 °C

Measure the local ambient temperature by placing a thermocouple near the center of the printed circuit board 5 mm (0.2 in.) from the board surface. Alternatively, you can rely on the reported Secondary System temperature to provide a conservative estimate of the local ambient

temperature. This alternative method provides a completely digital validation scheme that does not require using a thermocouple and allows you to validate the sbRIO-9651 SOM as part of every deployment.

In addition to being useful for system validation, digitally reported temperatures also provide feedback about system health and can be used as triggers or set points. The TEMP_ALERT signal from the J1 connector on the sbRIO-9651 SOM asserts when the CPU/FPGA or Primary System reported temperatures exceed specification. However, you should not use the TEMP_ALERT signal in place of proper system validation because the TEMP_ALERT signal does not monitor the Secondary System or local ambient temperatures. Refer to the *Temp Alert* section of Chapter 1, *Fixed Behavior Signals*, for more information about the TEMP_ALERT signal.

NI recommends that you monitor the digitally reported temperatures on deployed systems, especially if the temperatures approach the maximum thermal specifications during system validation testing. Monitoring allows individual systems to identify adverse thermal changes caused by differences in environmental, operating, or process conditions.

For more information about how to access and use the digitally reported temperature sensor measurements, visit `ni.com/info` and enter the Info Code `sbriosensors`.

Managing Power and Feature Utilization

An sbRIO-9651 SOM that heavily utilizes all of its performance and features consumes and dissipates substantially more power than when the device is idle. Certain features, such as LVDS outputs, can greatly increase the power that the Xilinx Zynq SoC dissipates and therefore also quickly raise the die junction temperature.

Consider the following options for reducing the die junction temperature:

- Design for additional thermal cooling that can appropriately dissipate power
- Reduce device feature utilization

Note Your final validation must consider software and hardware utilization that is representative of the final deployment conditions.

Note Refer to the *Input Power Requirements* section of the *NI sbRIO-9651 System on Module OEM Device Specifications* for specifications that approximate the maximum power requirement for each input rail on an sbRIO-9651 SOM with worst-case silicon manufacturing process and maximum junction temperatures. For a more accurate estimate of the power consumption for a specific application, NI recommends that you directly measure the power the sbRIO-9651 SOM consumes when running your application in an environment that is representative of the intended use case. You can use the Xilinx Power Estimator to calculate the VIO_BANK input rail power for a given configuration.

Mounting Recommendations for Maximizing Thermal Performance

The sbRIO-9651 SOM includes an integrated heat spreader that uses a thermal gap filler material to effectively conduct into the spreader the heat that the circuit card assembly components generate. NI recommends the following mounting procedures for maximizing the thermal performance of your application:

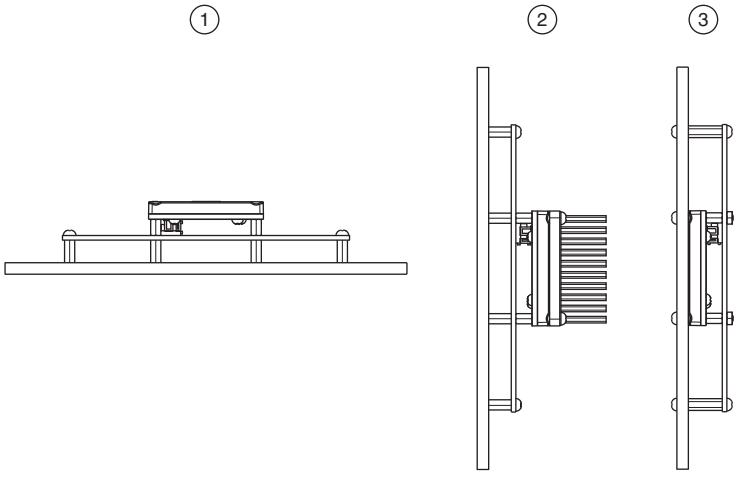
- Directly mount the flat and smooth exterior surface of the integrated heat spreader to a thermally-conductive surface, such as a metal enclosure wall or plate, as shown in Figure 4-1. An interface material such as thermal grease should be used to maximize the heat transfer from the integrated heat spreader to the enclosure or plate. The enclosure or plate conducts and convects the heat to the external ambient environment.

  If design limitations prevent this solution, you can alternatively attach a heat sink or other thermal solution to the integrated heat spreader, as shown in Figure 4-3. This solution takes advantage of natural convection or forced convection cooling provided by a fan.
- Mount the sbRIO-9651 SOM vertically with respect gravity to take advantage of natural convection cooling.
- Mount the sbRIO-9651 SOM below and away from other heat-dissipating components.

Note Placing the sbRIO-9651 SOM within a system or enclosure will also influence thermal performance.

Figure 4-6 shows good, better, and best thermal mounting solutions for the sbRIO-9651 SOM.

Figure 4-6. Thermal Mounting Solutions Comparison



1 **Good**—Horizontal mounting with no additional thermal provisions
2 **Better**—Vertical mounting with an attached heat sink, as described in Figure 4-3
3 **Best**—Vertical mounting directly to a thermally-conductive wall or plate, as described in Figure 4-1

Additional Resources for Managing Thermal Conditions

Visit `ni.com/info` and enter the Info Code `sbriocooling` for the following additional information to help you manage thermal conditions:

- Examples regarding the effect of the design factors discussed in this chapter
- Case study examples to help you estimate the achievable external ambient temperature for a representative system

Shock and Vibration

The mounting method you use, components you select, and assembly techniques you use influence the ability of the system to resist fretting corrosion and other damage caused by exposure to shock and vibration. Consider the following factors when designing your sbRIO-9651 SOM system to account for shock and vibration:

- In general, shorter SEARAY stack heights perform better than taller stack heights.
- Directly mounting the sbRIO-9651 SOM heat spreader to a rigid surface provides the best performance. If this method is not feasible for your design, minimize the amount of extra mass that only the sbRIO-9651 SOM supports, such as a heat sink or other thermal solution, that is fastened to the four standoffs. If you require substantial thermal solutions, provide additional structural support.
- NI recommends that you use connectors that provide the following benefits:
  - Positive locking
  - Provisions for strain relief
  - Substantial gold plating on pins
- The connectors on the reference carrier board are representative of connectors that NI has used and validated for high shock and vibration environments. The connectors and the sbRIO-9651 SOM have been tested to industry specifications and are recommended, where possible, for rugged environments.

  Exceptions to this recommendation are the barrel jack and Peripheral Module (Pmod) headers, which have designs that are not positive-locking or do not provide strain relief.
- NI offers a variety of cable assemblies and other connectivity accessories to complete your system design. Typically, these accessories include the best available designs, materials, and plating to maximize performance and longevity in rugged environments.

A

Reference Carrier Board Specifications and User Guide

This appendix provides pinouts, connectivity information, and specifications for the reference carrier board included with the sbRIO-9651 SOM development kit.

The reference carrier board provides the following:

- A hardware environment for developing and evaluating designs that target the sbRIO-9651 SOM.
- Access to most of the onboard peripherals available on the sbRIO-9651 SOM, including Ethernet, serial RS-232 and RS-485, USB Device, USB Host, SD card, and FPGA I/O.
- Additional supported capability through five Pmod connectors on the breadboard circuit prototyping area.

Note Visit `ni.com` and search for `9651` for the reference carrier board schematic and PCB gerber files.

Parts Locator Diagram and Block Diagram

Refer to the *NI sbRIO-9651 System on Module Development Kit Quick Start Guide* for the reference carrier board parts locator diagram and hardware block diagram.

Specifications

The following specifications are typical and not guaranteed.

Note Refer to the *NI sbRIO-9651 System on Module OEM Device Specifications* for complete specifications for each interface the sbRIO-9651 SOM supports. The specifications listed in this section pertain only to the interfaces implemented on the reference carrier board.

Ethernet

The reference carrier board includes the following tri-mode Ethernet ports:

- **Ethernet0**—Utilizes the primary Ethernet (GBE0) fixed behavior interface from the sbRIO-9651 SOM.
- **Ethernet1**—Implemented from the secondary Ethernet user-defined FPGA interface.

Serial

Number of ports	
TX/RX-only RS-232	1 (Serial1)
Full-modem RS-232	1 (Serial2)
RS-485	1 (Serial5)

CAN

Number of CAN ports	1 (CAN0)

SD Card

Number of full-size SD card sockets	1 (J2)

Refer to SanDisk Corporation or SD Association websites for information about SD I/O card specifications.

USB

Number of ports	
USB Device	1 (USB0)
USB Host	1 (USB1)
USB Host maximum current	900 mA (supports USB3 Vision cameras)

Pmod

The Pmod standard is defined by Digilent, Inc. and is used for small I/O interface boards that extend the capabilities of FPGA control boards. Pmods communicate with system boards via 6- or 12-pin connectors. The reference carrier board provides Pmod-compatible connectors to support quick connectivity to the Pmod ecosystem for prototyping and evaluating sensors, converters, connectors, and other devices.

Note Refer to the Digilent website at `www.digilentinc.com` for more information about Pmods.

Number of ports	
Pmod 12-pin	4 (Pmod1, Pmod2, Pmod3, Pmod4)
Pmod I^2C	1 (Pmod5)
Pmod Vcc	
Voltage	3.3 V
Current	100 mA

Pmod Signal Definitions on the Reference Carrier Board

Table A-1 describes the pins and signals on the sbRIO-9651 SOM connector used to implement four Pmod 12-pin connectors.

Note Refer to the *Pmod 12-Pin Connector Pinout* section of this chapter for more information about the Pmod 12-pin connector pins and signals on the reference carrier board.

Table A-1. Pmod 12-pin Connector Signal Definitions

Signal Name*	Pin #	DIO Signal	Signal Name*	Pin #	DIO Signal
PMOD1_PIN1	114	DIO_20_N	PMOD2_PIN1	164	DIO_28_N
PMOD1_PIN2	90	DIO_19_N	PMOD2_PIN2	131	DIO_23
PMOD1_PIN3	122	DIO_20	PMOD2_PIN3	172	DIO_28
PMOD1_PIN4	98	DIO_19	PMOD2_PIN4	139	DIO_23_N
PMOD1_PIN7	138	DIO_21_N	PMOD2_PIN7	107	DIO_22
PMOD1_PIN8	146	DIO_21	PMOD2_PIN8	155	DIO_24
PMOD1_PIN9	153	DIO_18	PMOD2_PIN9	115	DIO_22_N
PMOD1_PIN10	161	DIO_18_N	PMOD2_PIN10	163	DIO_24_N
PMOD3_PIN1	148	DIO_27	PMOD4_PIN1	135	DIO_37_MRCC
PMOD3_PIN2	116	DIO_26_N	PMOD4_PIN2	111	DIO_36_SRCC
PMOD3_PIN3	140	DIO_27_N	PMOD4_PIN3	143	DIO_37_N
PMOD3_PIN4	124	DIO_26	PMOD4_PIN4	119	DIO_36_N
PMOD3_PIN7	92	DIO_25_N	PMOD4_PIN7	159	DIO_38_MRCC
PMOD3_PIN8	109	DIO_29	PMOD4_PIN8	167	DIO_38_N
PMOD3_PIN9	100	DIO_25	PMOD4_PIN9	142	DIO_34_N
PMOD3_PIN10	117	DIO_29_N	PMOD4_PIN10	150	DIO_34

* All signals have both I/O directions and comply with the LVTTL I/O standard.

Table A-2 describes the specific pins and signals on the sbRIO-9651 SOM connector used to implement a Pmod I²C connector.

Note Refer to the *Pmod I²C Connector Pinout* section of this chapter for more information about the Pmod I²C connector pins and signals on the reference carrier board.

Table A-2. Pmod I²C Connector Signal Definitions

Signal Name*	Pin #	DIO Signal
PMOD_I2C_SCL1 PMOD_I2C_SCL2	105 129	DIO_16 DIO_17
PMOD_I2C_SDA1 PMOD_I2C_SDA2	113 137	DIO_16_N DIO_17_N
* All signals have both I/O directions and comply with the LVTTL I/O standard.		

RTC Battery

The reference carrier board provides a battery backup for the RTC on the sbRIO-9651 SOM.

Support Signals

The reference carrier board implements support signals in the following ways:

- STATUS_LED and TEMP_ALERT signals are routed to user-visible LEDs.
- SYS_RST# is connected to a Reset push button.

Connector Pinouts

RS-232, RS-485, and CAN Connector Pinouts

The RS-232, RS-485, and CAN connectors on the reference carrier board use the port shown in Figure A-1. Table A-3 describes the pins and signals on each port.

Figure A-1. RS-232, RS-485, and CAN Port Pin Locations

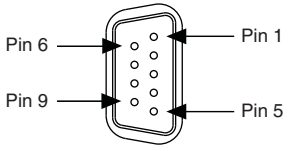


Table A-3. RS-232, RS-485, and CAN Port Pins and Signals

TX/RX-only RS-232		Full-modem RS-232		RS-485		CAN	
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	NC	1	DCD	1	GND	1	NC
2	RXD	2	RXD	2	NC	2	CANL
3	TXD	3	TXD	3	NC	3	GND
4	NC	4	DTR	4	RXP	4	NC
5	GND	5	GND	5	RXN	5	SHIELD
6	NC	6	DSR	6	NC	6	GND
7	NC	7	RTS	7	NC	7	CANH
8	NC	8	CTS	8	TXP	8	NC
9	NC	9	RI	9	TXN	9	NC

Pmod 12-Pin Connector Pinout

The Pmod 12-pin connectors on the reference carrier board use the port shown in Figure A-2. Table A-4 describes the pins and signals on the port.

Figure A-2. Pmod 12-Pin Port Pin Locations

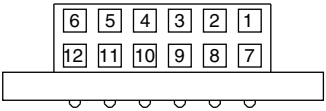


Table A-4. Pmod 12-Pin Port Pins and Signals

Pin	Signal	Pin	Signal
1	PMOD*x*_PIN1	7	PMOD*x*_PIN7
2	PMOD*x*_PIN2	8	PMOD*x*_PIN8
3	PMOD*x*_PIN3	9	PMOD*x*_PIN9
4	PMOD*x*_PIN4	10	PMOD*x*_PIN10
5	GND	11	GND
6	3.3 V power	12	3.3 V power

Pmod I2C Connector Pinout

The Pmod I2C connector on the reference carrier board uses the port shown in Figure A-3. Table A-5 describes the pins and signals on the port.

Figure A-3. Pmod I2C Port Pin Locations

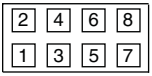


Table A-5. Pmod I2C Port Pins and Signals

Pin	Signal	Pin	Signal
1	PMOD5_SCL1	5	GND
2	PMOD5_SCL2	6	GND
3	PMOD5_SDA1	7	3.3 V power
4	PMOD5_SDA2	8	3.3 V power

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Minimize Our Environmental Impact* web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

Battery Replacement and Disposal

Battery Directive This device contains a long-life coin cell battery. If you need to replace it, use the Return Material Authorization (RMA) process or contact an authorized National Instruments service representative. For more information about compliance with the EU Battery Directives 2006/66/EC about Batteries and Accumulators and Waste Batteries and Accumulators, visit `ni.com/environment/batterydirective`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。 (For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

B

Revision History

Table B-1 lists changes to this document since its first iteration.

Table B-1.

Revision	Edition Date	Changes
B	August 2015	• Added information about eliminating the effects of contact bounce to the *Eliminating the Effects of Contact Bounce* section of Chapter 1, *Fixed Behavior Signals*. • Added more information about ordering the recommended mating connector (Molex, 45970-4130) from TTI, Inc. to the *Ordering the Recommended Mating Connector* section of Chapter 4, *Mechanical Considerations*.
A	December 2014	—

C

NI Services

National Instruments provides global services and support as part of our commitment to your success. Take advantage of product services in addition to training and certification programs that meet your needs during each phase of the application life cycle; from planning and development through deployment and ongoing maintenance.

To get started, register your product at ni.com/myproducts.

As a registered NI product user, you are entitled to the following benefits:

- Access to applicable product services.
- Easier product management with an online account.
- Receive critical part notifications, software updates, and service expirations.

Log in to your National Instruments ni.com User Profile to get personalized access to your services.

Services and Resources

- **Maintenance and Hardware Services—**NI helps you identify your systems' accuracy and reliability requirements and provides warranty, sparing, and calibration services to help you maintain accuracy and minimize downtime over the life of your system. Visit ni.com/services for more information**.**
  - **Warranty and Repair—**All NI hardware features a one-year standard warranty that is extendable up to five years. NI offers repair services performed in a timely manner by highly trained factory technicians using only original parts at a National Instruments service center.
  - **Calibration—**Through regular calibration, you can quantify and improve the measurement performance of an instrument. NI provides state-of-the-art calibration services. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.

- **Training and Certification**—The NI training and certification program is the most effective way to increase application development proficiency and productivity. Visit ni.com/training for more information.
  - The Skills Guide assists you in identifying the proficiency requirements of your current application and gives you options for obtaining those skills consistent with your time and budget constraints and personal learning preferences. Visit ni.com/skills-guide to see these custom paths.
  - NI offers courses in several languages and formats including instructor-led classes at facilities worldwide, courses on-site at your facility, and online courses to serve your individual needs.
- **Technical Support**—Support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—Visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Software Support Service Membership**—The Standard Service Program (SSP) is a renewable one-year subscription included with almost every NI software product, including NI Developer Suite. This program entitles members to direct access to NI Applications Engineers through phone and email for one-to-one technical support, as well as exclusive access to online training modules at ni.com/self-paced-training. NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit ni.com/ssp for more information.
- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.

You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.