PCIe-5763 Specifications

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Contents

PCIe-5763 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- ***Typical*** specifications describe the performance met by a majority of models.
- ***Nominal*** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- ***Measured*** specifications describe the measured performance of a representative model.

Specifications are ***Typical*** unless otherwise noted.

Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5.0 V Power	±5%, 50 mA maximum, nominal

Table 1. Digital I/O Signal Characteristics

Signal	Type	Direction
MGT Tx± <3..0>*	Xilinx UltraScale GTH	Output
MGT Rx± <3..0>*	Xilinx UltraScale GTH	Input
DIO <7..0>	Single-ended	Bidirectional

Signal	Type	Direction
5.0 V	DC	Output
GND	Ground	—

* Multi-gigabit transceiver (MGT) signals are available on devices with KU040 and KU060 FPGAs only.

Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 kΩ, nominal
Output impedance	50 Ω, nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 µA load, nominal

Table 2. Digital I/O Single-Ended DC Signal Characteristics[1]

Voltage Family (V)	V_{IL} (V)	V_{IH} (V)	V_{OL} (100 µA Load) (V)	V_{OH} (100 µA Load) (V)	Maximum DC Drive Strength (mA)
3.3	0.8	2.0	0.2	3.0	24
2.5	0.7	1.6	0.2	2.2	18
1.8	0.62	1.29	0.2	1.5	16
1.5	0.51	1.07	0.2	1.2	12
1.2	0.42	0.87	0.2	0.9	6

Digital I/O High-Speed Serial MGT

Note For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

Note MGTs are available on devices with KU040 and KU060 FPGAs only.

Data rate	500 Mb/s to 16.375 Gb/s, nominal
Number of Tx channels	4
Number of Rx channels	4
I/O AC coupling capacitor	100 nF

MGT TX± Channels

Minimum differential output voltage[2]	170 mV peak-to-peak into 100 Ω, nominal

1. Voltage levels are guaranteed by design through the digital buffer specifications.
2. 800 mV peak-to-peak when transmitter output swing is set to the maximum setting.

I/O coupling	AC-coupled, includes 100 nF capacitor

MGT RX± Channels

Differential input voltage range	
≤ 6.6 Gb/s	150 mV peak-to-peak to 2000 mV peak-to-peak, nominal
> 6.6 Gb/s	150 mV peak-to-peak to 1250 mV peak-to-peak, nominal

Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor

Reconfigurable FPGA

PCIe-5763 modules are available with multiple FPGA options. The following table lists the FPGA specifications for the PCIe-5763 FPGA options.

Table 3. Reconfigurable FPGA Options

	KU035	**KU040**	**KU060**
LUTs	203,128	242,200	331,680
DSP48 slices (25 × 18 multiplier)	1,700	1,920	2,760
Embedded Block RAM	19.0 Mb	21.1 Mb	38.0 Mb
Default timebase	80 MHz		
Timebase reference sources	Onboard 100 MHz oscillator		
Data transfers	DMA, interrupts, programmed I/O	DMA, interrupts, programmed I/O, multi-gigabit transceivers	
Number of DMA	60		

	KU035	KU040	KU060
channels			

Note The Reconfigurable FPGA Options table depicts the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Note For FPGA designs using the majority of KU040 or KU060 FPGA resources while running at clock rates over 150 MHz, the module may require more power than is available. If the module attempts to draw more than allowed per its specification, the module protects itself and reverts to a default FPGA personality. Refer to the getting started guide for your module or contact NI support for more information.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Analog Input

Notice The maximum input signal levels are valid only when the module is powered on. To avoid permanent damage to the PCIe-5763, do not apply a signal to the device when the module is powered down.

General Characteristics

Number of channels	4, single-ended, simultaneously sampled
Connector type	SMA
Input impedance	50 Ω
Input coupling	AC or DC[3]
Sample Rate	
Internal Sample Clock	500 MHz
External Sample Clock	500 MHz [4]

Analog-to-digital converter (ADC)	ADS54J69, 16-bit resolution

Typical Specifications

Full-scale input range (normal operating conditions)

3. Only one analog input path type is populated.
4. You must provide a 1 GHz clock at the CLK/REF IN front panel connector to enable this rate.

AC-coupled	2.03 V_{pp} (10.15 dBm) at 10 MHz
DC-coupled	1.97 V_{pp} (9.87 dBm)
Gain accuracy	
AC-coupled	±0.1 dB at 10 MHz
DC-coupled	±1% at DC
DC Offset	
AC-coupled	±41 µV
DC-coupled	±225 µV
Bandwidth (-3 dB)[5]	
AC-coupled	0.07 MHz to 225 MHz
DC-coupled	DC to 225 MHz[6]

Table 4. Single-Tone Spectral Performance

	AC-Coupled		**DC-Coupled**	
	Input Frequency		**Input Frequency**	
	10.1 MHz	**123.1 MHz**	**10.1 MHz**	**123.1 MHz**
SNR* (dBFS)	73.7	71.8	71.7	70.6

5. Normalized to 10 MHz.
6. Upper -3 dB bandwidth limited by ADC decimation filter.

	AC-Coupled		DC-Coupled	
	Input Frequency		Input Frequency	
	10.1 MHz	123.1 MHz	10.1 MHz	123.1 MHz
SINAD* (dBFS)	73.5	71.7	70.7	70.5
SFDR (dBc)	-85.6	-87.7	-77.2	-86.1
ENOB† (bits)	11.9	11.6	11.5	11.4

* Measured with a -1 dBFS signal and corrected to full-scale. 1 kHz resolution bandwidth.

† Calculated from SINAD and corrected to full scale.

Table 5. Noise Spectral Density

Module	nV/rt (Hz)	dBm/Hz	dBFS/Hz
AC-coupled	9.5	-147.4	-157.5
DC-coupled	11.8	-145.6	-155.4

Note Noise spectral density is verified using a 50 Ω terminator connected to the input.

Figure 1. AC-Coupled Single Tone Spectrum (10.1 MHz, -1 dBFS, 1 kHz RBW), Measured

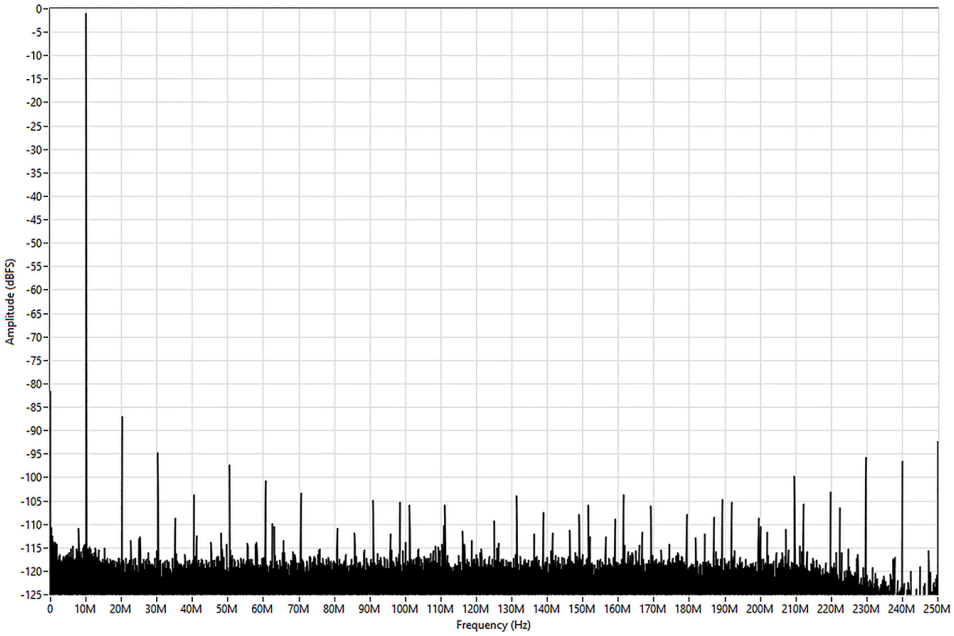


Figure 2. AC-Coupled Single Tone Spectrum (123.1 MHz, -1 dBFS, 1 kHz RBW), Measured

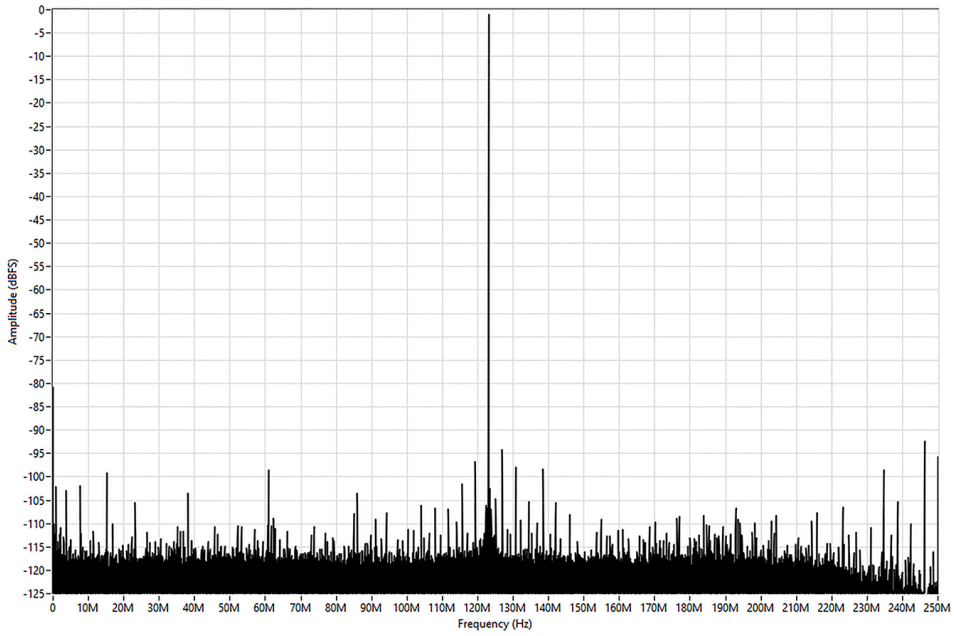


Figure 3. DC-Coupled Single Tone Spectrum (10.1 MHz, -1 dBFS, 1 kHz RBW), Measured

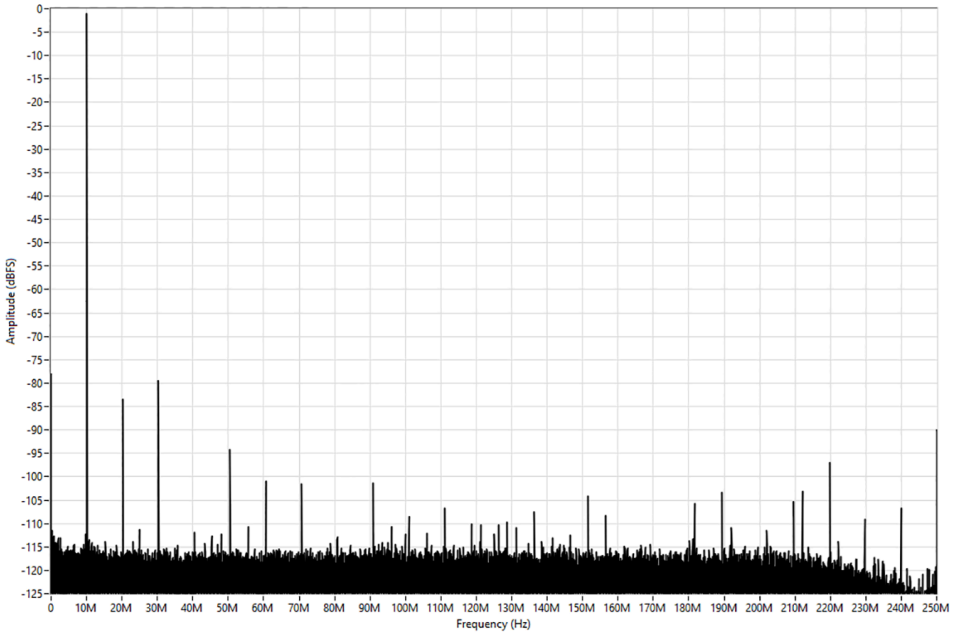
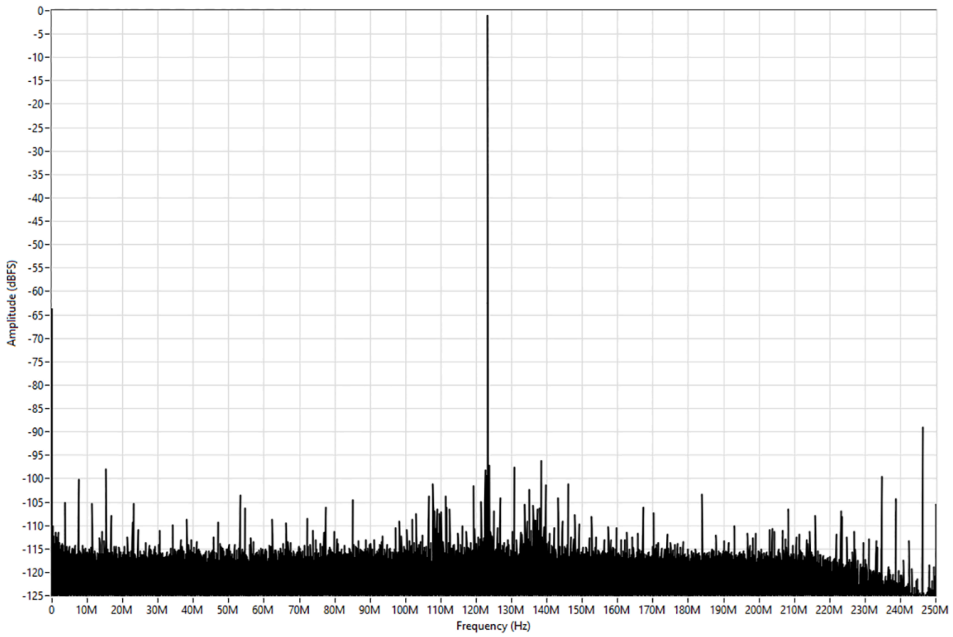


Figure 4. DC-Coupled Single Tone Spectrum (123.1 MHz, -1 dBFS, 1 kHz RBW), Measured



Channel-to-channel crosstalk AC-coupled, characteristic	
10 MHz	-87 dB
100 MHz	-89 dB

225 MHz	-85 dB
Channel-to-channel crosstalk DC-coupled, characteristic	
1 MHz	-94 dB
100 MHz	-83 dB
225 MHz	-78 dB

Figure 5. AC-Coupled Frequency Response, Measured

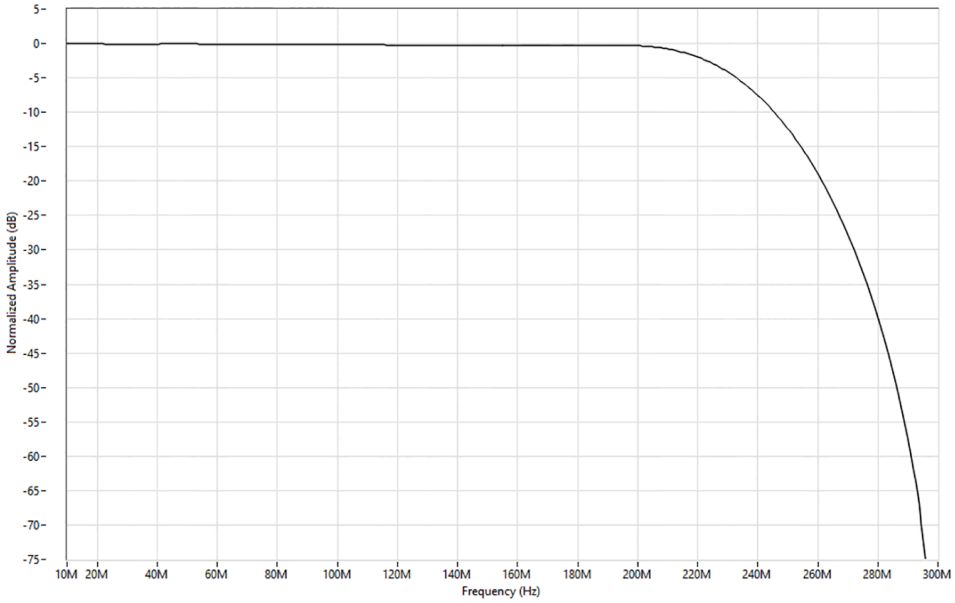


Figure 6. AC-Coupled Frequency Response Zoomed In, Measured

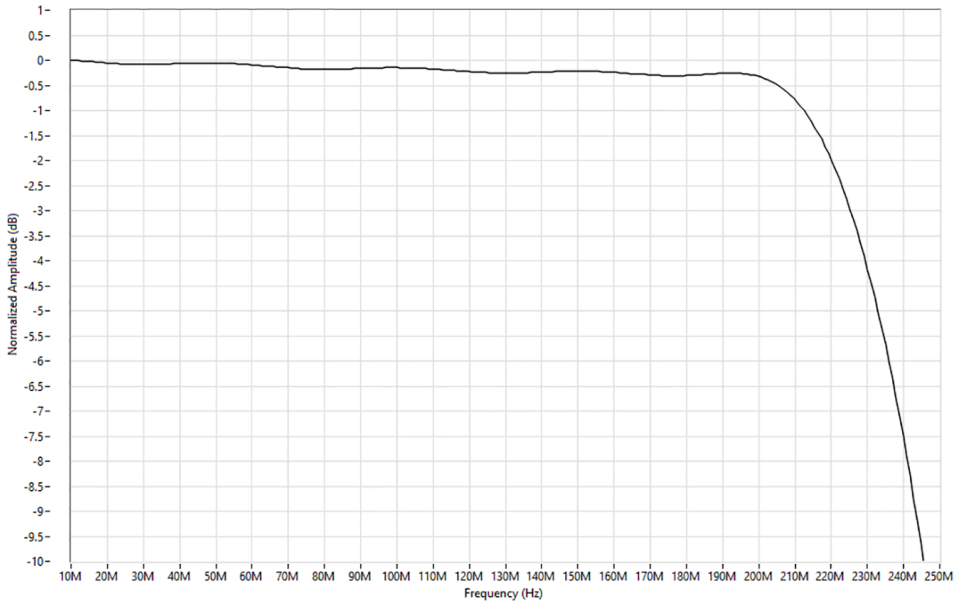


Figure 7. DC-Coupled Frequency Response, Measured

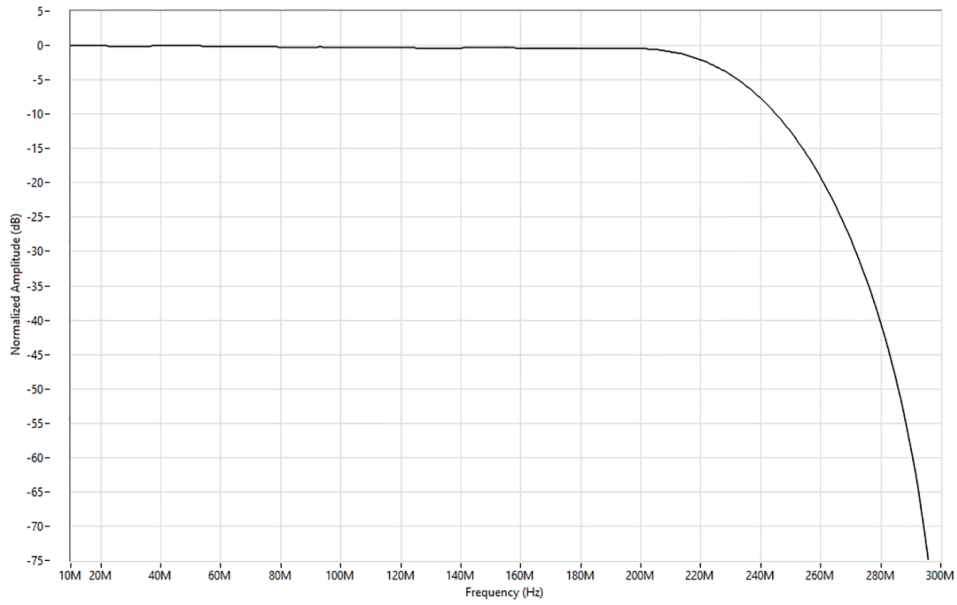


Figure 8. DC-Coupled Frequency Response Zoomed In, Measured

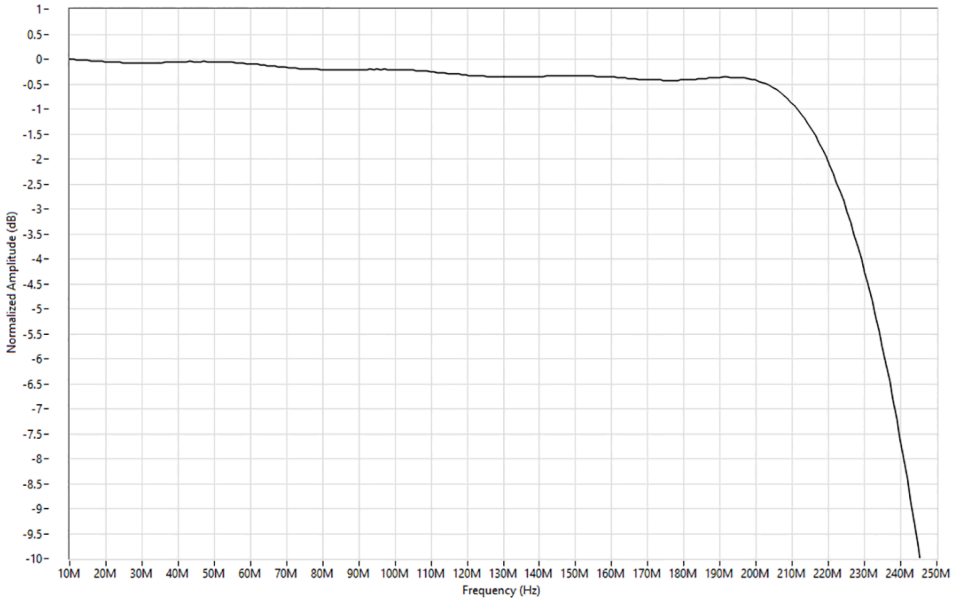
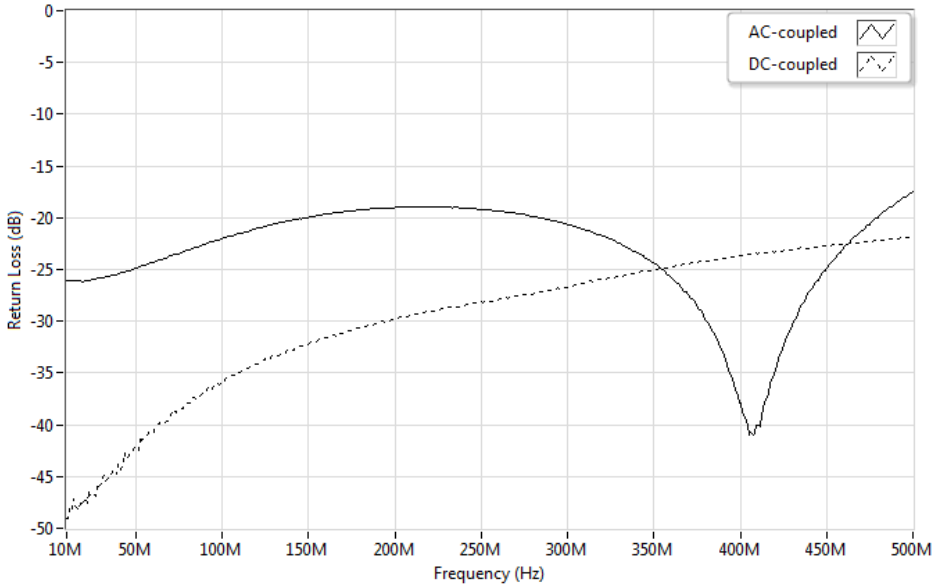


Figure 9. Input Return Loss, Measured



REF/CLK IN

General Characteristics

Connector type	SMA

Input impedance	50 Ω
Input coupling	AC
Reference input voltage range	0.3 V_{pp} to 4 V_{pp}
Sample Clock input voltage range	0.3 V_{pp} to 4 V_{pp}
Absolute maximum voltage	±12 V DC, 4 V_{pp} AC
Duty cycle	45% to 55%
Onboard reference timebase stability	±0.7 ppm
Sample Clock jitter[7]	
AC-coupled	135 fs RMS
DC-coupled	142 fs RMS

Table 6. Clock Configuration Options

Clock Configuration	External Clock Type	External Clock Frequency	Description
Internal Reference Clock*	—	—	The internal Sample Clock locks to an onboard voltage-controlled temperature

7. Integrated from 1 kHz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter. Excludes trigger jitter.

Clock Configuration	External Clock Type	External Clock Frequency	Description
			compensated crystal oscillator (VCTCXO).
Internal Baseboard Reference Clock	—	10 MHz	The internal Sample Clock locks to the 10 MHz Reference Clock provided from the FPGA baseboard.
External Reference Clock (REF/CLK IN)	Reference Clock	10 MHz†	The internal Sample Clock locks to an external Reference Clock, which is provided through the REF/CLK IN front panel connector.
External Sample Clock (REF/CLK IN)	Sample Clock	1 GHz‡	An external Sample Clock can be provided through the REF/CLK IN front panel connector.

* Default clock configuration.

† The PLL Reference Clock must be accurate to ±25 ppm.

‡ The ADC sample rate is 500 MS/s with a 1 GHz clock.

Figure 10. AC-Coupled Phase Noise with 182.6 MHz Input Tone, Measured

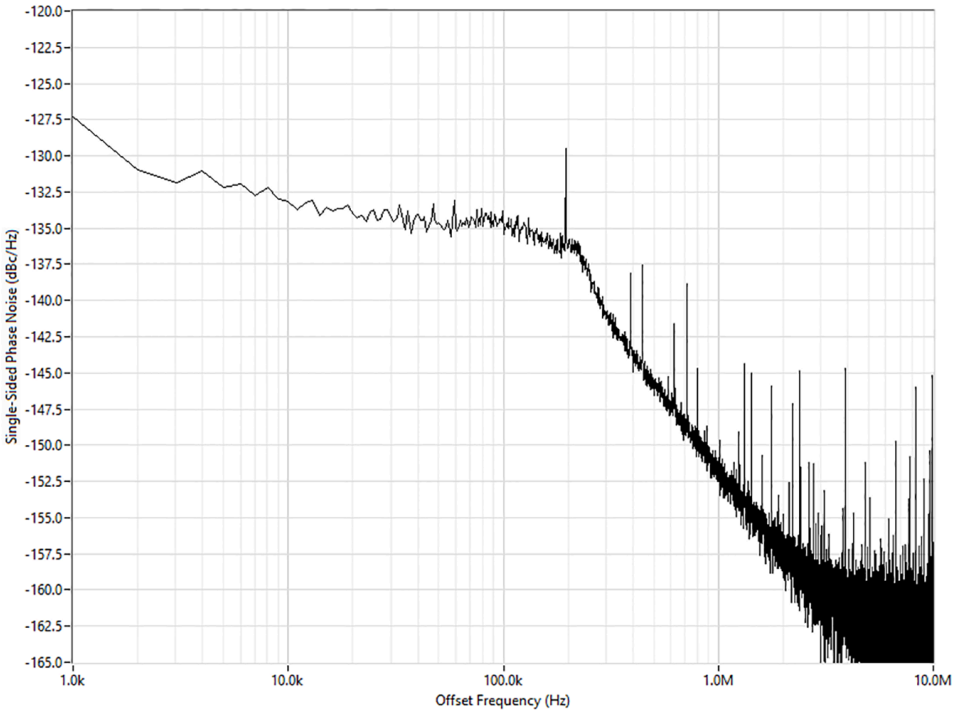
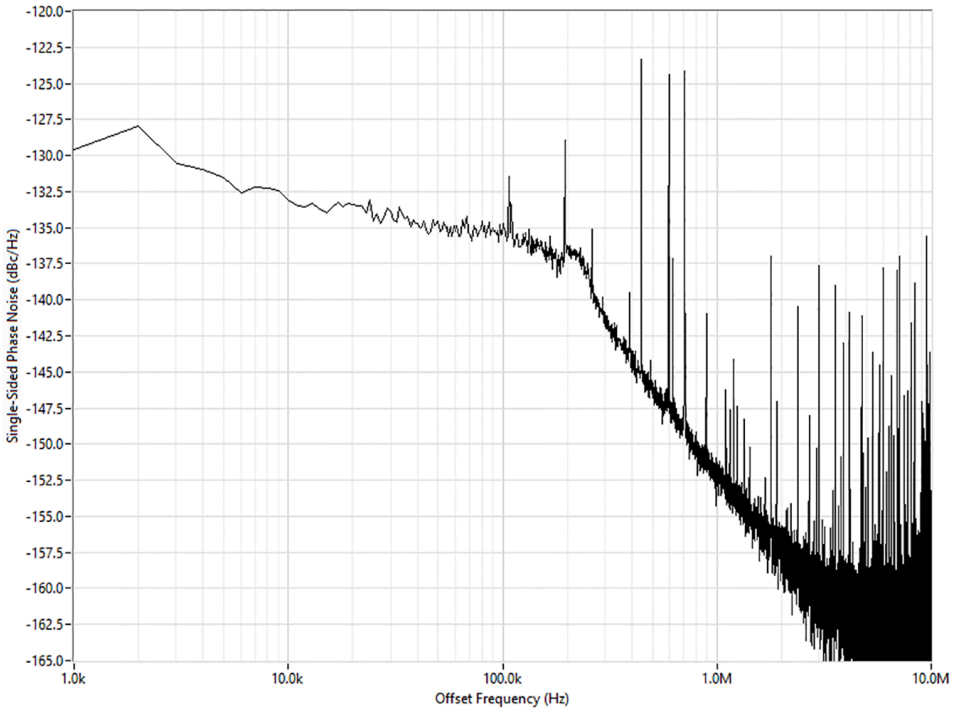


Figure 11. DC-Coupled Phase Noise with 182.6 MHz Input Tone, Measured



Bus Interface

Card edge form factor	PCI Express Gen-3 x8
Slot compatibility	x8 and x16 PCI Express

Maximum Power Requirements

Note Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	4.5 A
+12 V	5 A
Maximum total power	75 W

Physical

Dimensions (including I/O bracket, not including connectors)	12.6 cm × 26.3 cm × 4 cm (5.0 in. × 10.4 in. × 1.6 in.)
Weight	990 g (35 oz)
PCI Express mechanical form factor	Standard height, three-quarter length, double slot

Integrated air mover (fan)	Yes
Maximum rear panel exhaust airflow	84 m^3/h (50 CFM) (without any chassis impedance)

Environmental

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution degree	2

Indoor use only.

Operating Environment

Operating temperature, local[8]	0 °C to 45 °C
Operating humidity	10% to 90% RH, noncondensing

Storage Environment

Ambient temperature range	-20 °C to 70 °C
Relative humidity range	5% to 95% RH, noncondensing

8. For PCI Express adapter cards with integrated air movers, NI defines the local operational ambient environment to be at the fan inlet. For cards without integrated air movers, NI defines the local operational ambient environment to be 25 mm (1 in.) upstream of the leading edge of the card.