PXIe-1489 Specifications

Contents

PXIe-1489 Specifications

Introduction

This document lists the specifications for the following variants of the PXIe-1489:

- PXIe-1489 FlexRIO GMSL3 Deserializer
- PXIe-1489 FlexRIO GMSL3 Serializer
- PXIe-1489 FlexRIO GMSL3 SerDes

Note If you purchased the PXIe-1489 as part of an NI system, refer to your system documentation for application-specific specifications.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C
- Installed in chassis with slot cooling capacity ≥58 W[1]

Serial Device Compatibility

Refer to the following information to verify that the PXIe-1489 module chip set is compatible with your serial device or camera.

Chip set brand	Maxim Integrated
Module deserializer	MAX96792A
Module serializer	MAX96793

Note Contact the manufacturer of your serial device or camera for details on compatibility with the PXIe-1489 module.

Variant Mode Support

Refer to the following to verify whether your PXIe-1489 variant supports Pixel or Tunneling Mode.

PXIe-1489 Variant	Serializer	Deserializer	Mode Supported
GMSL3 Interface Module, 4 In, MAX96792A Deserializers	N/A	MAX96792A	Tunneling and Pixel
GMSL3 Interface Module, 4 Out, MAX96793 Serializers	MAX96793	N/A	Tunneling and Pixel
GMSL3 Interface Module, 2 In 2 Out,	MAX96793	MAX96792A	Tunneling and Pixel

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[1] The PXIe-1489 SerDes module can operate in a chassis with a slot cooling capacity of <58 W in a restricted user mode.

PXIe-1489 Variant	Serializer	Deserializer	Mode Supported
MAX96793/MAX96792A SerDes			

Bus Interface

Form factor	PCI Express Gen-3 x8

Reconfigurable FPGA

The following table lists the specifications for the PXIe-1489 FPGA.

FPGA	KU11P
LUTs	298,560
DSP48 slices (25 × 18 multiplier)	2,928
Embedded Block RAM	21 Mb
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)
Data transfers	DMA, interrupts, programmed I/O
Embedded UltraRAM™	22 Mb
Number of DMA channels	60

Note These values reflect the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP

for PCI Express, device configuration, and various board I/O. For more information, contact NI support.

Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank
Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)

Serial I/O Characteristics

Input Channels

Connector label	SI
Connector type	FAKRA Male Code Z, coaxial
Power over Coax (PoC) output range, AUX power maximum	6 V to 32 V, 800 mA per channel

PoC Output Range, Internal Power Supply

Nominal voltage	12 V

Maximum current	400 mA per channel

I/O standard	GMSL3 with PoC
Maximum data rate	12 Gb/s

Output Channels

Connector label	SO
Connector type	FAKRA Male Code Z, coaxial

PoC Input Range

Nominal voltage	6 V to 32 V
Maximum current	800 mA per channel

I/O standard	GMSL3 with PoC
Maximum data rate	12 Gb/s

AUX Power Channels

Power sink or source maximum voltage	6 V to 32 V
Power sink or source maximum current	800 mA per channel

Power connector type	Conn Terminal Block, Weidmuller part number 2439690000

Power Connector Wiring

Gauge	0.08 mm to 0.5 mm (28 AWG to 20 AWG)
Wire strip length	8 mm
Terminal connection type	Tension clamp
Retention	External strain relief of AUX power connections recommended

PXIe-1489 Deserializer

Input channels	4
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	D-PHY, 1, 2, or 4 lanes, 600 Mb/s to 2,500 Mb/s per lane, no lane swaps or inversions

PXIe-1489 Serializer

Output channels	4
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2

CSI-2 interface	D-PHY, 1, 2, or 4 lanes, 600 Mb/s to 2,500 Mb/s per lane, no lane swaps or inversions

PXIe-1489 SerDes

Input channels	2
Output channels	2
Maximum Tap pairs per module	2
Communication	I2C Configuration, I2C Backchannel, GPIO Communication, CSI-2
CSI-2 interface	D-PHY, 1, 2, or 4 lanes, 600 Mb/s to 2,500 Mb/s per lane, no lane swaps or inversions

Power Requirements

Note Power requirements are dependent on the contents of the LabVIEW FPGA VI used in your application.

Note Do not position product so that it is difficult to disconnect power.

Note If you are powering the PXIe-1489 using your PXIe chassis backplane, refer to the chassis specifications for detailed information about your internal power supply.

Backplane Power Source

3.3 V	3.0 A, maximum
12 V	6.0 A, maximum

Backplane Power

Total power	82 W, maximum

Power over Coax (PoC) Source, External Power Supply

Voltage range	6 V to 32 V
Maximum current	800 mA per channel, up to 8 channels

Power over Coax (PoC) Source, Internal Power Supply

Nominal voltage	12 V
Maximum current	400 mA per channel

Diagnostic PoC Current Measurement

Current measurement range	50 mA to 800 mA
Current measurement accuracy	50 mA to 100 mA: ±20% 100 mA to 800 mA: ±15%

Diagnostic PoC Voltage Measurement

Voltage measurement range	6 V to 32 V
Voltage measurement accuracy[2]	±2.5%

Environmental Characteristics

Operating temperature	0 °C to 55 °C[3]
Storage temperature	-40 °C to 71 °C
Operating humidity	10% to 90%, noncondensing
Storage humidity	5% to 95%, noncondensing

Pollution degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)

Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

[2] Due to resistive (IR drop) losses in the circuit, actual voltage measurement accuracy depends on the load of the PoC circuit.

[3] The PXIe-1489 requires a chassis with slot cooling capacity ≥58 W. Not all chassis with slot cooling capacity ≥58 W can achieve this ambient temperature range. Refer to PXI chassis specifications on ni.com/docs to determine the ambient temperature ranges your chassis can achieve.

Physical

Dimensions	3U, one-slot PXI Express module, 21.6 cm x 2.0 cm x 13.0 cm (8.5 in. x 0.8 in. x 5.1 in.)
Weight	472 g (16.7 oz)

Timing and Synchronization

Timebase	100 MHz, shared by all ports, disciplined by PXI_Clk100
Trigger I/O source	PXI_Trig <0:7>