PXIe-5673/ 5673E Device Help

2024-06-19

Contents

PXIe-5673/5673E Overview

The PXIe-5673/5673E has the following basic characteristics and features:

- 85 MHz to 6.6 GHz frequency range
- 100 MHz instantaneous bandwidth
- 156 dB compression-to-noise dynamic range
- -144 dBm/Hz typical noise density (0 dBm output level)
- AWG module onboard waveform memory (memory size varies by AWG module)
- NI-RFSG instrument driver software transparently operates all modules as a single unit
- Four-slot wide PXI/3U CompactPCI form factor

The PXIe-5673/5673E follows industry-standard Plug&Play specifications for the PXI/PXI Express bus and allows seamless integration with compliant systems.

Note Refer the ***PXIe-5673 Specifications*** and ***PXIe-5673E Specifications*** documents for the latest module specifications.

PXIe-5673

The PXIe-5673 is an RF vector signal generator consisting of the following PXI/PXI Express hardware modules:

- PXI-5650/5651/5652—1.3 GHz, 3.3 GHz, or 6.6 GHz local oscillator (LO) source PXI module
- PXIe-5450/5451—16 bit, 400 megasample per second (MS/s) arbitrary waveform generator (AWG) PXI Express module
- PXIe-5611—6.6 GHz I/Q modulator PXI Express module; NI-RFSG also refers to this module as the Upconverter

Note There is no physical device labeled "PXIe-5673." The PXIe-5673 is the instrument comprised of the PXIe-5611 I/Q modulator module, the

> PXIe-5450/5451 AWG module, and the PXI-5650/5651/5652 LO source module. The PXIe-5673 is operated by the NI-RFSG instrument driver.

The hardware modules interconnect using SMA-SMA coaxial cables. Refer to the getting started guide for information about interconnecting hardware modules.

PXIe-5673E

The PXIe-5673E is an RF vector signal generator consisting of the following PXI Express hardware modules:

- PXIe-5650/5651/5652—1.3 GHz, 3.3 GHz, or 6.6 GHz local oscillator (LO) source PXI Express module
- PXIe-5450/5451—16 bit, 400 megasample per second (MS/s) arbitrary waveform generator (AWG) PXI Express module
- PXIe-5611—6.6 GHz I/Q modulator PXI Express module; NI-RFSG also refers to this module as the Upconverter

> **Note** There is no physical device labeled "PXIe-5673E." The PXIe-5673E is the instrument comprised of the PXIe-5611 I/Q modulator module, the PXIe-5450/5451 AWG module, and the PXIe-5650/5651/5652 LO source module. The PXIe-5673E is operated by the NI-RFSG instrument driver.

The hardware modules interconnect using SMA-SMA coaxial cables. Refer to the getting started guide for more information about interconnecting hardware modules.

Related information:

- PXIe-5673 Specifications
- PXIe-5673E Specifications
- PXIe-5673E Getting Started

Features Supported on PXIe-5673/5673E Modules

The following tables show the features supported by the different device variations of

the PXIe-5673/5673E according to which AWG module you have.

Number	Feature
1	RF list mode
2	Improved tuning time
3	Additional REF OUT2 connector and improved harmonics
4	Peer-to-peer streaming

Revision	PXI-5650/5651/5652	PXIe-5650/5651/5652
PXIe-5450 Module Revision A	No new features	2, 3
PXIe-5450 Module Revision B or Later	No new features	1, 2, 3, 4
PXIe-5451 Module, All Revisions	No new features	1, 2, 3, 4
Using the PXIe-5611 revision F or later adds improved amplitude settling time to all PXIe-5673/5673E devices.		

PXIe-5673/5673E Block Diagram

Refer to the PXI/PXIe-5650/5651/5652, PXIe-5611, and PXIe-5450/5451 block diagram topics for more information about the block diagrams for the individual modules that comprise the PXIe-5673/5673E.

Figure 1. PXIe-5673 Block Diagram

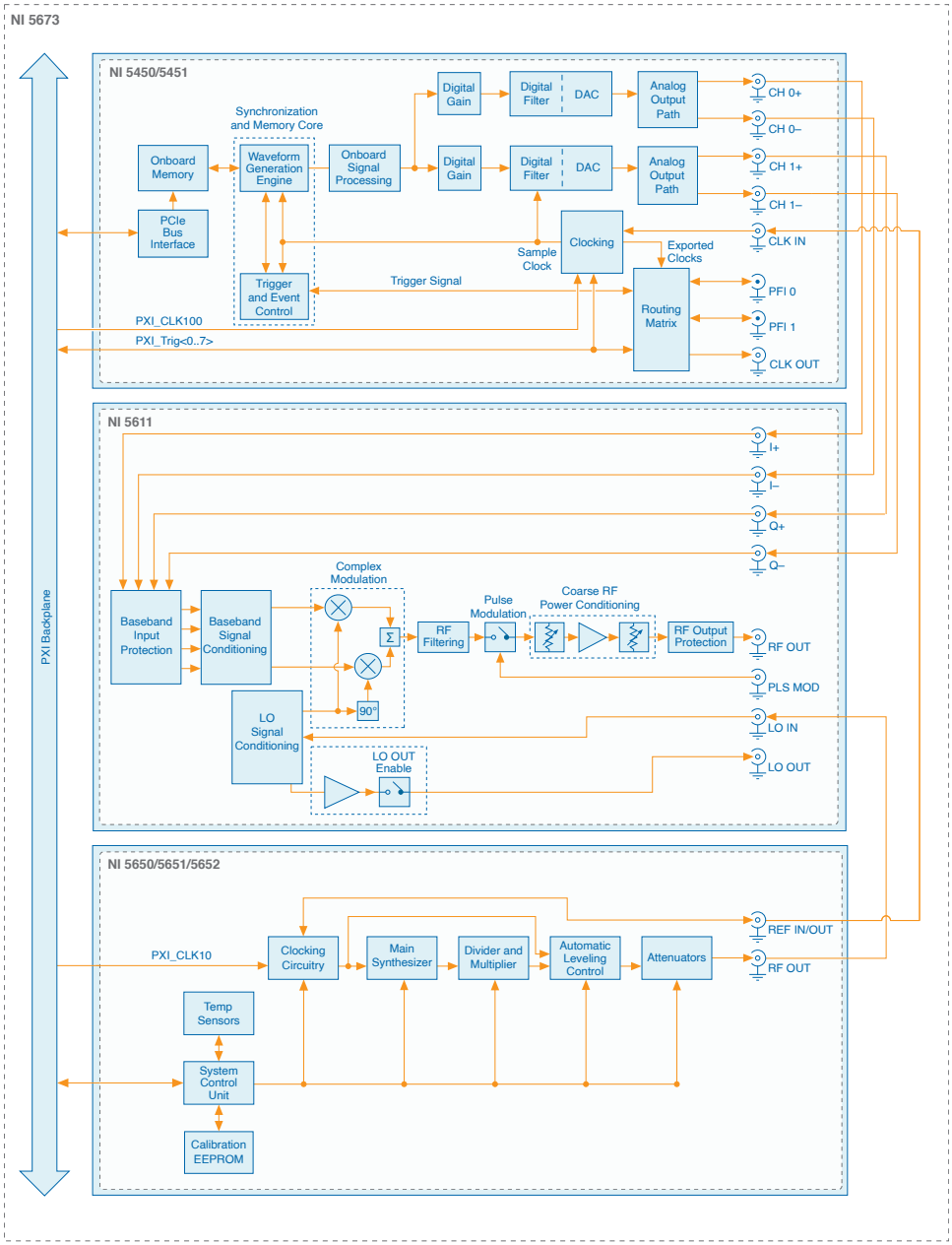
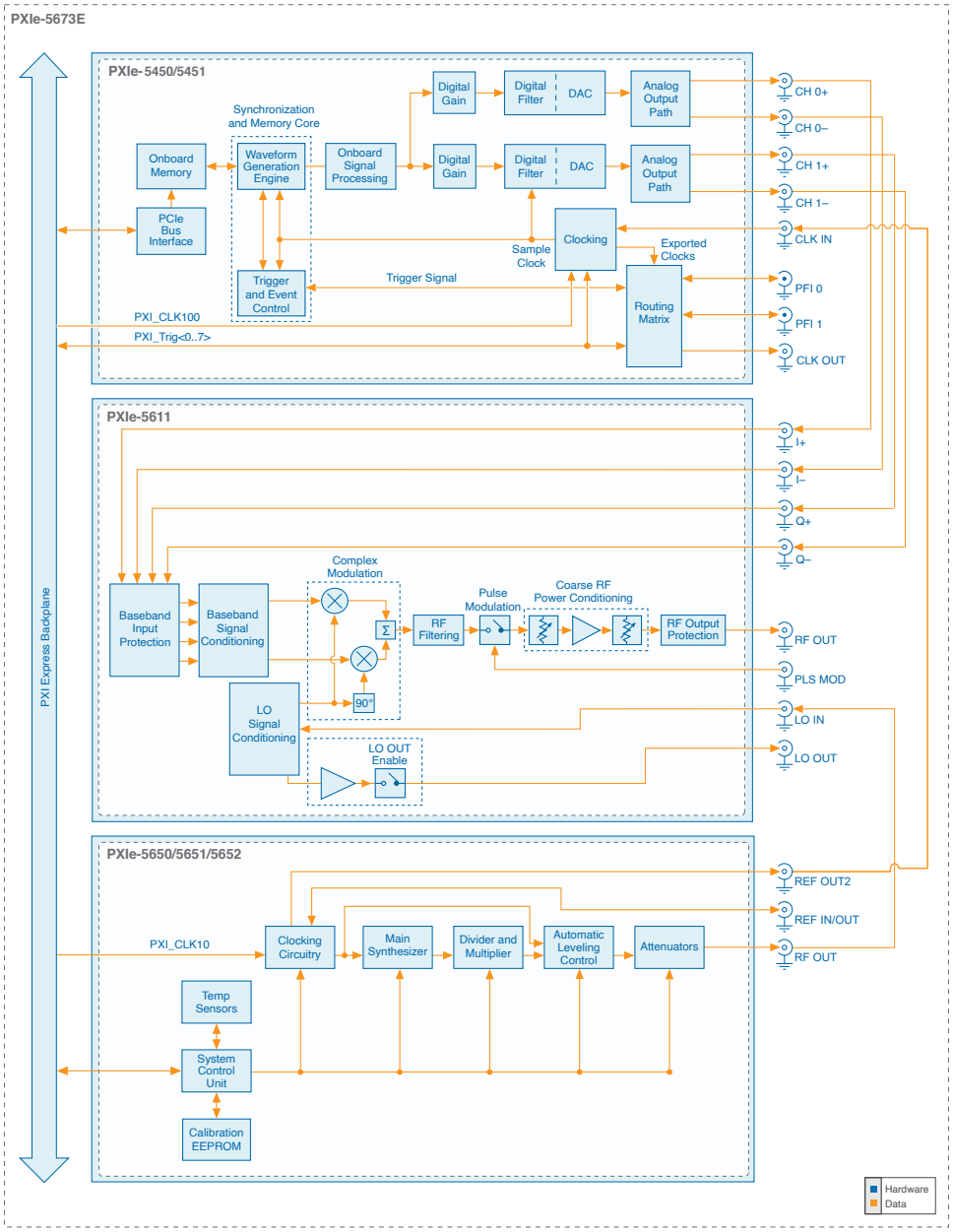


Figure 2. PXIe-5673E Block Diagram

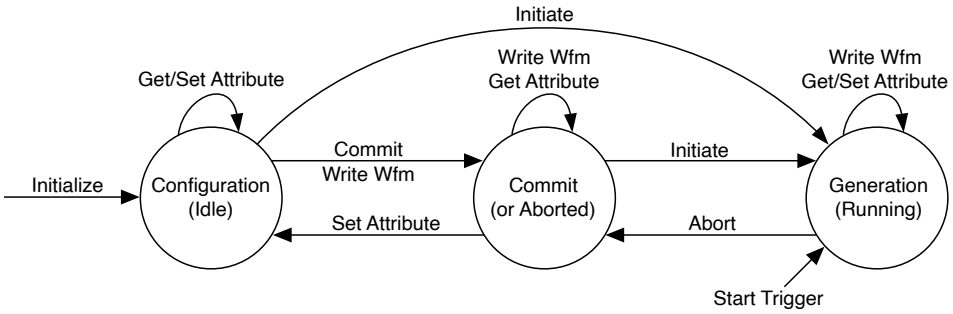


Related reference:

- PXI/PXIe-5650/5651/5652 Block Diagram
- PXIe-5611 Block Diagram
- PXIe-5450/5451 Block Diagram

Hardware State Diagram

The following diagram shows the hardware states of the vector signal generator.



- ***Configuration (Idle)***- The device is not generating a waveform. All session properties or attributes can be programmed in the Configuration state. In the Configuration state, the properties or attributes have not necessarily been applied to hardware, and the hardware configuration of the device may not match the session property or attribute values. The device remains configured as it was the last time a session was committed. If the computer has just been powered on, reset, or the niRFSG Reset Device VI or the niRFSG_ResetDevice function has just been called, the device is in the default hardware state.
- ***Commit (or Aborted)***- Applies the device's properties or attributes to the hardware. This state also generates an LO signal for the current settings, commits the AWG, and locks Reference Clocks on only the PXIe-5673/5673E Vector Signal Generator.
- ***Generation***- In the Generation state, the device is generating a waveform as specified by the session properties or attributes configured. Dynamic (or on-the-fly) properties and attributes are applied immediately to hardware. Started Event trigger is generated as the device recognizes triggers. Depending on the configured trigger mode, the device may stay in the Generation state until the generation is aborted.

PXI Trigger Lines

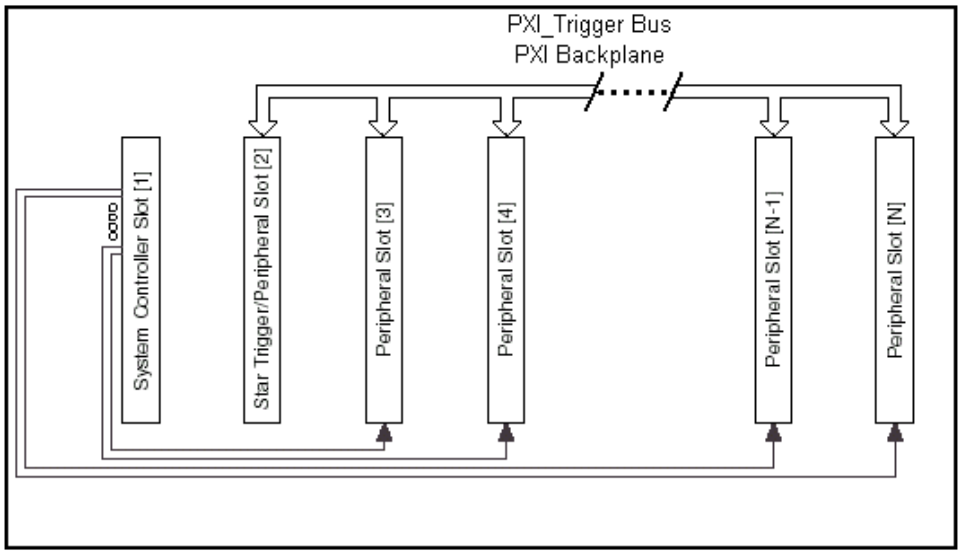
The PXI trigger bus features eight PXI trigger lines.

You can use these flexible lines in a variety of ways:

- To synchronize the operation of several different PXI peripheral devices
- To use one device to control carefully timed sequences of operations performed on other devices in the system

- To pass triggers between devices, allowing precisely timed responses to asynchronous external events that are being monitored or controlled

The number of triggers that an application requires varies with the complexity and number of events involved.



The PXI Specification is implemented with the RTSI bus through the PXI trigger lines. PXI Specification requires eight lines, PXI_Trig<0..7>, on the P2/J2 connector of the PXI chassis for the trigger lines.

System Reference Clock

The PXI chassis supplies the PXI 10 MHz system Reference Clock signal (PXI_CLK10) and the PXI 100 MHz system Reference Clock signal (PXIe_CLK100), which is phase synchronous with the PXI_CLK10 signal, independently to each peripheral slot.

An independent buffer drives the clock signal to each peripheral slot. The buffer has a source impedance matched to the backplane and a skew ranging from less than 1 ns to better than 250 ps between slots. You can use this common Reference Clock signal to synchronize multiple devices in a measurement or control system. You can drive PXI_CLK10 from an external source through the PXI_CLK10_IN pin on the P2 connector of the PXI star trigger slot, which is Slot 2. Sourcing an external clock on this pin automatically disables the 10 MHz source on the backplane. You can synchronize

multiple chassis that have connectors on the back panel for 10 MHz reference in and 10 MHz reference out. Refer to your PXI chassis documentation for more information.

Note The PXI_CLK10 Reference Clock signal cannot be driven by a device in Slot 2 in a PXI Express chassis, but the PXI_CLK10 Reference Clock signal can be driven from a PXI Express system timing module in Slot 10 of a PXI Express chassis.

PFI Lines

PFI lines are multipurpose programmable function input/output lines. These lines serve as connections to virtually all internal timing signals. NI RF signal generators have up to six digital lines that can accept or generate a trigger, generate a marker, accept or generate a Reference Clock. The function of each PFI line is independent.

Note Lines PFI 2, PFI 3, PFI 4, and PFI 5 are supported on only the PXI-5670/5671.

Routing Signals

To export signals to the PFI lines on the device front panel, you must specify a trigger, clock, or event using the `signal` parameter of the niRFSG Export Signal VI or the niRFSG_ExportSignal function.

To import signals, you must select a trigger using a polymorphic instance of the niRFSG Configure Trigger VI and specify a PFI line as the source terminal.

Notice If you enable a PFI line for output, do not connect any external signal source to it; doing so can damage the device, the computer, and the connected equipment.

Power On and Reset Conditions

The PXIe-5673/5673E hardware is in the following state after powering on or restarting

the system and allowing the PC operating system and NI-RFSG to fully load. These conditions are also true after a device reset that you perform directly from NI Measurement & Automation Explorer (MAX).

- PXIe-5611 I/Q modulator module is powered on.
- All module front panel ACCESS LEDs are green.
- LO OUT front panel connector is disabled.
- All attenuators are asserted.
- All module front panel ACTIVE LEDs are off.
- RF output power is set to <-140 dBm, minimum.
- Warmup begins (if applicable).

PXIe-5673/5673E Front Panel Connectors and Indicators

This section describes the connectors and LED indicators on the front panels of the PXI or PXI Express hardware modules comprising the PXIe-5673/5673E Vector Signal Generator.

Figure 3. PXIe-5673 Front Panel

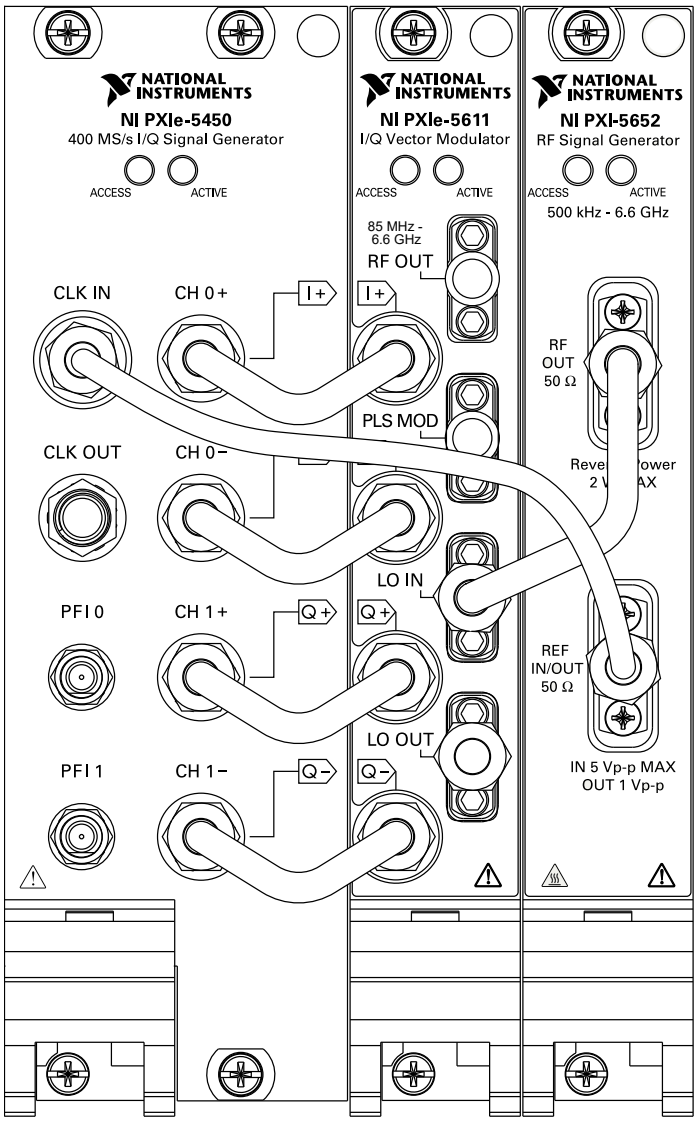
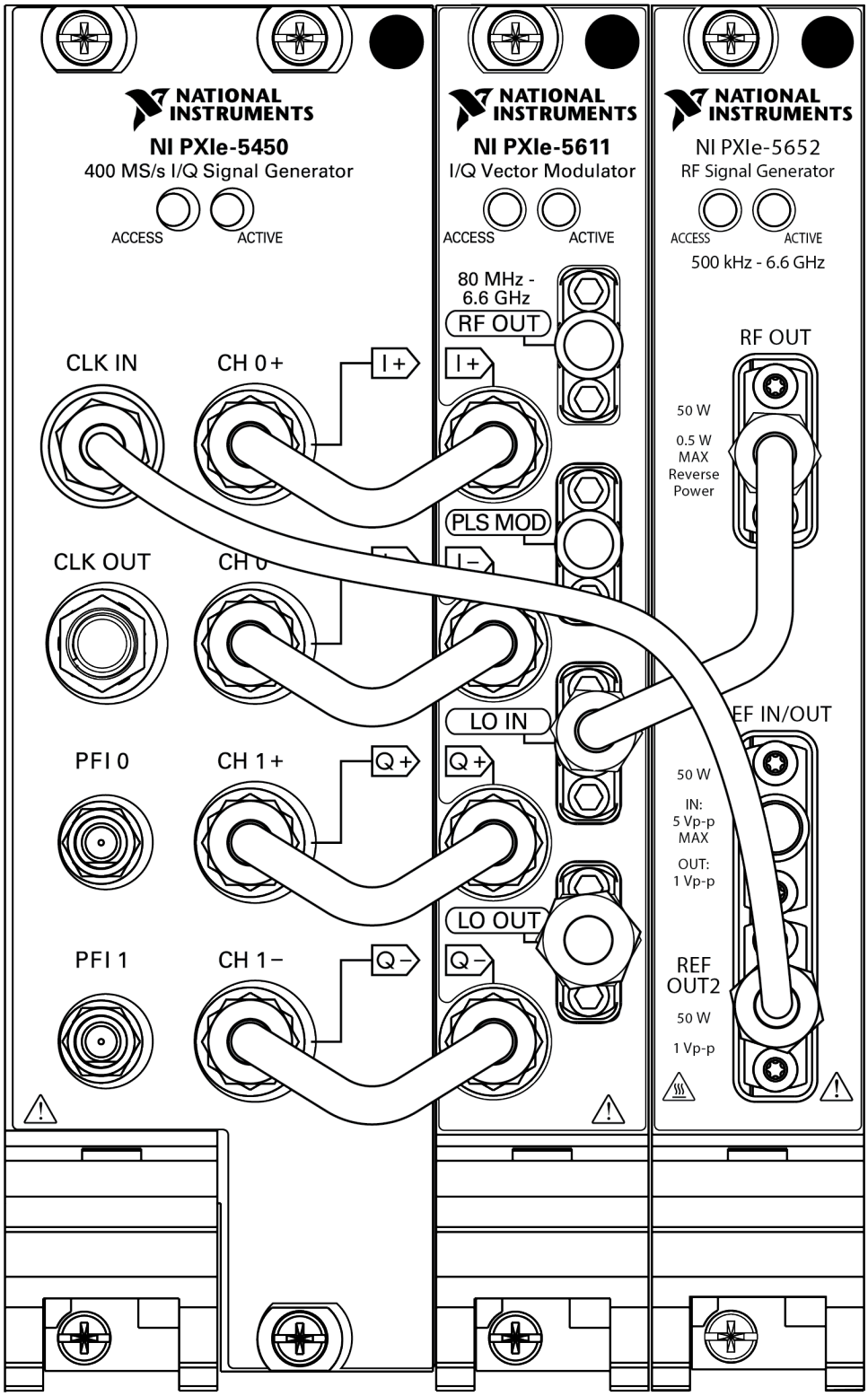


Figure 4. PXIe-5673E Front Panel



PXIe-5450/5451 Front Panel and LEDs

The following figure shows the PXIe-5450/5451 Waveform Generator front panel, which contains eight connectors and two multicolor LEDs.

Figure 5. PXIe-5450 Front Panel

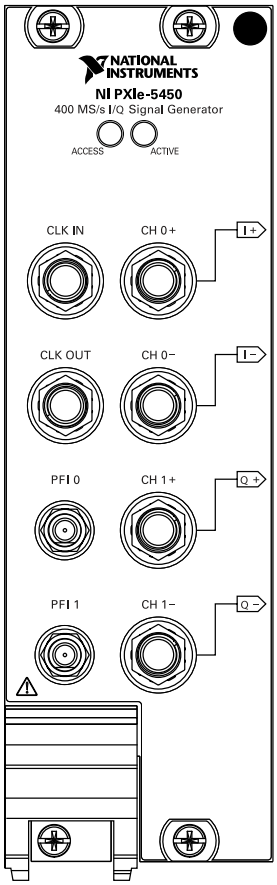
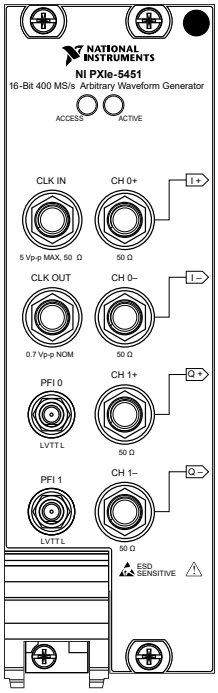


Figure 6. PXIe-5451 Front Panel



The following table provides connector and use information for the PXIe-5450/5451 front panel connectors.

Table 1. General Connector Descriptions

Connector	Use
CLK IN	Accepts a Reference Clock from an external source that can frequency lock the Sample Clock timebase to the external Reference Clock. The signal received at this connector can also be used as a Sample Clock source, and the signal level on this connector is 500 mV_{pk-pk} to 5 V_{pk-pk} for a 50% duty cycle, and 550 mV_{pk-pk} to 4.5 V_{pk-pk} This connector is AC-coupled.Connect to the REF IN/OUT connector on the PXI/PXIe-5650/5651/5652 RF Analog Signal Generator.
CLK OUT	Provides a clock signal that can be shared by other devices. This connector is AC-coupled. The signal level on this connector is 0.7 V_{pk-pk}, typical.
PFI 0	Accepts a trigger from an external source that can start or step through waveform generation or can route signals from several clock, event, and trigger sources. The signal level on this connector is 1.5 V low and 1.8 V high. This connector is AC-coupled. Can be connected to the CLK OUT connector on an additional PXIe-5450/

Connector	Use
	5451 front panel.
PFI 1	Accepts a trigger from an external source that can start or step through waveform generation or can route signals from several clock, event, and trigger sources.
CH 0+ / I+	Provides differential waveform output. The signal level on this connector is 1 V_{pk-pk}, maximum. Connect to the I+ connector on the PXIe-5611 I/Q Modulator front panel.
CH 0- /CH I-	Provides differential waveform output. The signal level on this connector is 1 V_{pk-pk}, maximum.Connect to the I– connector on the PXIe-5611 front panel.
CH 1+ / Q+	Provides differential waveform output. The signal level on this connector is 1 V_{pk-pk}, maximum.Connect to the Q+ connector on the PXIe-5611 front panel.
CH 1- / Q-	Provides differential waveform output. The signal level on this connector is 1 V_{pk-pk}, maximum. Connect to the Q– connector on the PXIe-5611 front panel.

The following table provides LED and indications information for the PXIe-5450/5451 AWG module front panel LEDs.

Table 2. LED Indicators

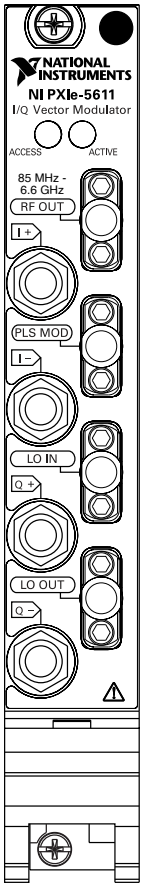
LED	Indications
ACCESS	Indicates the basic hardware status of the PXIe-5450/5451 module. Off—The module is not yet functional or has detected a problem with a power rail. Amber—The module is being accessed. ***Accessed*** means that the device setup registers are being written to in order to control the device or load waveforms. Green—The module is ready to be programmed.

LED	Indications
ACTIVE	Indicates the state of the PXIe-5450/5451 hardware module: Off—The module is not armed or triggered. Amber—The module is armed and waiting for a Start Trigger. Green—The module has received a Start Trigger and is generating a waveform. Red—The device has detected an error. NI-RFSG must access the device to determine the cause of the error. The LED remains red until the error condition is removed. Errors may include the following conditions: • The device has detected an unlocked condition on a previously locked PLL. A PLL that is unlocked while in reset does not show an error. • The device has powered down because the internal temperature exceeded the maximum limit. The over-temperature condition must be corrected and the device reset. For more information about keeping your device cool, refer to the ***Maintain Forced-Air Cooling Note to Users*** included with your device. • The device has detected an error.

PXIe-5611 I/Q Modulator Front Panel and LEDs

The following figure shows the PXIe-5611 I/Q Modulator module front panel, which contains eight connectors and two multicolor LEDs.

Figure 7. PXIe-5611 Front Panel



The following table provides connector and use information for the PXIe-5611 front panel connectors.

Table 3. General Connector Descriptions

Connector	Use
RF OUT	Output connector for RF signals. The input impedance is 50 Ω, nominal. Do not apply more than 5 VDC or reverse power of 1 W to the RF OUT front panel connector or damage can occur. RF OUT has reverse power protection circuitry that is enabled with powers greater than +30 dBm. This connector is AC-coupled.
PLS MOD	Accepts an externally provided pulse signal that is transistor-transistor logic (TTL) compatible. The TTL-compatible signal allows for pulse modulation of the RF output signal observed on the RF OUT front panel connector. The maximum input that should be provided to the PLS MOD front panel connector is –0.5 V to +8 V. This input is DC-coupled.
LO IN	Accepts the RF carrier to the I/Q modulator to produce a single-

Connector	Use
	sideband suppressed carrier waveform to modulate the baseband signal applied to the I/Q inputs.
LO OUT	Routes the local oscillator output used for combining multiple devices with one common LO source (PXI/PXIe-5650/5651/5652 RF Analog Signal Generator). The output impedance is nominally 50 Ω. The LO OUT connector allows for phase coherent operation of multiple devices by allowing the use of a common LO signal when daisy-chaining the signal to other devices.If you are daisy-chaining more than one PXIe-5611 device, check the applied power level. Due to gain tolerances, you may lose a few dB of power when the LO OUT signal is used on a secondary device. Fine amplitude control for a single device is achieved by fine adjustment of the LO source. Due to tolerances over frequency, you may have significantly different power levels after daisy-chaining multiple devices. If the LO IN signal on the secondary device is not within 0.5 dB from the nominal 0 dB power, the secondary device's specification may not be met.When not in use, it is recommended that an external 50 Ω terminator is applied to the LO OUT front panel connector. Output is disabled into an internal load when the LO OUT front panel connector is not in use, but some LO power may leak, and the output should be terminated
I+	Accepts analog in-phase differential signals for the I/Q modulator. The applied signal levels are nominally 0.4 V_{pk-pk} (±0.2 V), single-ended, or 0.8 V_{pk-pk}, differential. The input signal bandwidth is up to 50 MHz. The input impedance is 100 Ω, differential. Do not apply more than ±15 VDC to these inputs or damage may occur. This input is DC-coupled.
I-	
Q-	Accepts analog quadrature-phase differential signals for the I/Q modulator. The applied signal levels are nominally 0.4 V_{pk-pk} (±0.2 V), single-ended, or 0.8 V_{pk-pk}, differential. The input signal bandwidth is up to 50 MHz. The input impedance is 100 Ω, differential. Do not apply more than ±15 VDC to these inputs or damage may occur. This input is DC-coupled.
Q+	

Note The baseband interface between the PXIe-5450/5451 Waveform Generator and the PXIe-5611 is designed to be fully differential. For normal operation, ensure that all four baseband connections (I+, I-, Q+, Q-) are

> properly connected. If one or more of these connections are not correctly made, common-mode errors cause the PXIe-5673/5673E Vector Signal Generator to be uncalibrated.

The following table provides LED and indications information for the PXIe-5611 I/Q modulator module front panel LEDs.

Table 4. LED Indicators

LED	Indications
ACCESS	Indicates the basic hardware status of the PXIe-5611 module. Off—The module is not yet functional or has detected a problem with a power rail, or a thermal shutdown has occurred. Amber—The module is being accessed. Green—The module is ready to be programmed.
ACTIVE	Indicates the state of the PXIe-5611 module: Off—Generation has stopped Amber—The module is being accessed. Accessed means that the device setup registers are being written to in order to control the device or load waveforms. Green—The module is generating a waveform. Red—The module has detected an error state. This indicates one of the following error states: • Reverse power protection fault—The RF OUT connector is disabled in order to protect the device from the power being driven back into the RF OUT connector.

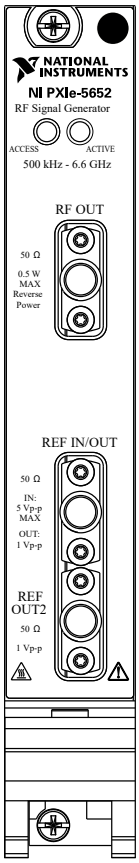
LED	Indications
	• I/Q overvoltage protection fault—The I/Q inputs exceed the maximum voltage. I and Q inputs are disabled in order to protect the device.

PXI/PXIe-5650/5651/5652 Front Panel and LEDs

The PXI/PXIe-5650/5651/5652 RF Analog Signal Generator is available with either two or three front panel connectors.

PXIe-5650/5651/5652

The following figure shows the PXIe-5650/5651/5652 front panel with three connectors and two multicolor LEDs (PXIe-5652 shown).



The following table provides connector and use information for the PXIe-5650/5651/5652 front panel connectors:

Table 5. General Connector Descriptions

Connector	Use
RF OUT	Generates the RF signal at the requested frequency and power level. RF OUT is the main RF output from the PXIe-5650/5651/5652. Output impedance is 50 Ω, nominal. RF OUT covers a frequency range of 500 kHz to 6.6 GHz with a maximum signal level of +10 dBm. RF OUT output is protected against reverse RF power up to –27 dBm and 10 VDC. This connector is AC-coupled.
REF IN/OUT	Routes the reference signal to and from the PXIe-5650/5651/5652. Maximum damaging level is 10 VDC. REF IN/OUT has an input impedance of 50 Ω. NI recommends that a high impedance source is not used to provide a reference signal. A high impedance source can result in high DC transients that can exceed 10 VDC and damage the device. The maximum applied reference signal level is 5 Vpk-pk or damage can occur. As an output, the device returns a 10 MHz reference at 1 Vpk-pk. As a reference input, the device accepts a 10 MHz reference signal.
REF OUT2	Routes the reference signal from the PXIe-5650/5651/5652. This connector has an output impedance of 50 Ω. The device returns a 10 MHz reference at 1 Vpk-pk.

The following table provides information about the PXIe-5650/5651/5652 front panel LEDs and the device states they indicate:

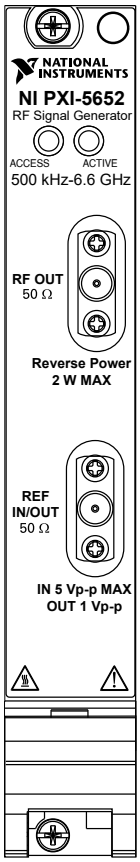
Table 6. LED Indicators

LED	Indications
ACCESS	Indicates the basic hardware status of the PXIe-5650/5651/5652 module. OFF—The module is not yet functional or has detected a problem with a PXI/PXI Express power rail. AMBER—The module is being accessed. ***Accessed*** means that the device setup registers

LED	Indications
	are being written to in order to control the device. GREEN—The module is ready to be programmed.
ACTIVE	Indicates the state of the PXIe-5650/5651/5652 module: Off—The module is not generating a signal. Amber—The module PLLs are attempting to lock. Green—The module is generating a signal; applicable PLLs are locked. Red— The module has detected an error state; this may indicate a PLL lock failure or a thermal shutdown condition.

PXI-5650/5651/5652

The following figure shows the PXI-5650/5651/5652 module front panel with two connectors and two multicolor LEDs (PXI-5652 shown).



The following table provides connector and use information for the PXI-5650/5651/5652 module front panel connectors:

Table 7. General Connector Descriptions

Connector	Use
RF OUT	Generates the RF signal at the requested frequency and power level. RF OUT is the main RF output from the PXIe-5650/5651/5652. Output impedance is 50 Ω, nominal. RF OUT covers a frequency range of 500 kHz to 6.6 GHz with a maximum signal level of +10 dBm. RF OUT output is protected against reverse RF power up to –27 dBm and 10 VDC. This connector is AC-coupled.
REF IN/OUT	Routes the reference signal to and from the PXIe-5650/5651/5652. Maximum damaging level is 10 VDC. REF IN/OUT has an input impedance of 50 Ω. NI recommends that a high impedance source is not used to provide a reference signal. A high impedance source can result in high DC transients that can exceed 10 VDC and damage the device. The maximum applied reference signal level is 5 Vpk-pk or damage can occur. As an output, the device returns a 10 MHz reference at 1 Vpk-pk. As a reference input, the device accepts a 10

Connector	Use
	MHz reference signal.

The following table provides information about the PXI-5650/5651/5652 module front panel LEDs and the device states they indicate:

Table 8. LED Indicators

LED	Indications
ACCESS	Indicates the basic hardware status of the PXI-5650/5651/5652 module. OFF—The module is not yet functional or has detected a problem with a PXI power rail. AMBER—The module is being accessed. ***Accessed*** means that the device setup registers are being written to in order to control the device. GREEN—The module is ready to be programmed.
ACTIVE	Indicates the state of the PXI-5650/5651/5652 module: Off—The module is not generating a signal. Amber—The module PLLs are attempting to lock. Green—The module is generating a signal; applicable PLLs are locked. Red— The module has detected an error state; this may indicate a PLL lock failure or a thermal shutdown condition.

REF IN/OUT Connector

You can program the PXI/PXIe-5650/5651/5652 RF Analog Signal Generator REF IN/OUT connector as an input connector or output connector. Phase-locking to an external source configures the connector as an input connector, and exporting the reference signal configures the connector as an output connector. The ability to export or import the reference signal makes it possible to frequency-lock NI RF devices together using one as the master.

Note Although the devices may be frequency-locked together, their generated RF signals are not phase-synchronized.

Coupling of the external reference signal into the reference circuit is possible, which potentially produces phase-offset spurs in the RF signal. For these reasons, disconnect or turn off any signals connected to the REF IN/OUT connector when REF IN/OUT is not being used.

Refer to your device specifications document for PXI/PXIe-5650/5651/5652 onboard frequency reference specifications.

PXIe-5450/5451 Waveform Generator

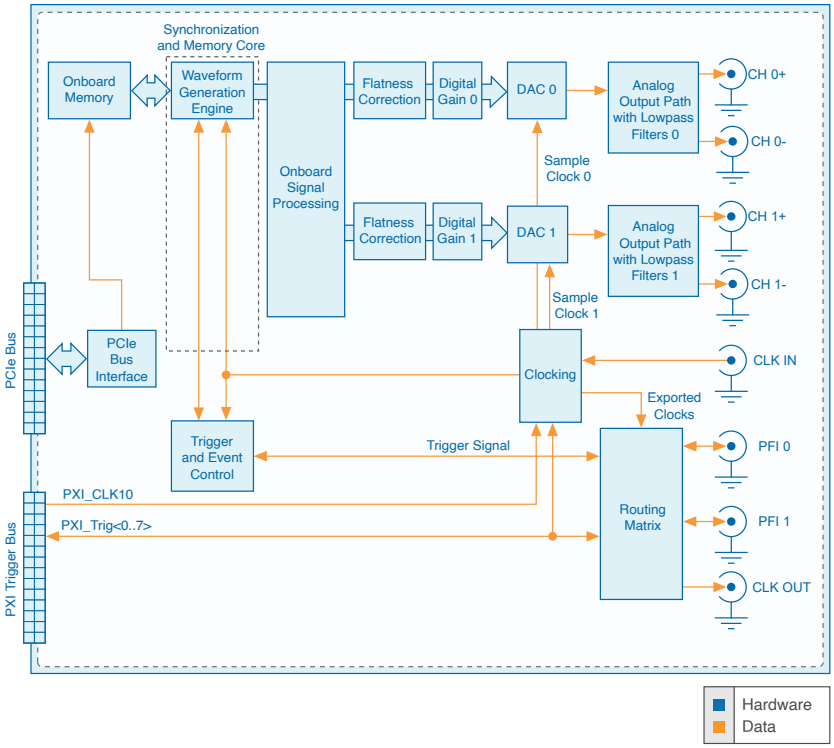
The PXIe-5450/5451 is a dual-channel, 400 MS/s, 16-bit arbitrary waveform generator (AWG) PXI Express module.

This section contains information about the PXIe-5450/5451 AWG module when used with the PXIe-5611 I/Q Modulator and the PXI/PXIe-5650/5651/5652 RF Analog Signal Generator.

PXIe-5450/5451 Block Diagram

This topic contains information about the PXIe-5450/5451 top-level block diagram and descriptions of the individual blocks.

Figure 8. PXIe-5450/5451 Block Diagram



The following list describes the individual blocks:

- ***Onboard Memory*** stores the waveform data and scripts that you load into the device.
- ***Clocking*** allows you to create your Sample Clock and Reference Clock.
- The ***Waveform Generation Engine*** retrieves the waveform data and instructions from the ***Onboard Memory*** using the Sample Clock. The ***Waveform Generation Engine*** also uses this clock to retrieve triggers from ***Trigger and Event Control***.
- The output from the ***Waveform Generation Engine*** is sent to the ***DAC*** device after any digital gain or onboard signal processing is applied.
- The ***DAC*** also contains a selectable ***Digital Filter***, which interpolates and filters the waveform data.
- The waveform data is sent from the ***DAC*** to the ***Analog Output*** path where the waveform data is filtered and amplified.
- The ***Routing Matrix*** allows flexible routing of the PXI Trigger lines and the external PFI lines.

Memory Options

AWG modules are available with various memory size options. Onboard waveform memory size dictates the maximum time duration for which arbitrary waveforms can be generated without repeating the same waveform data.

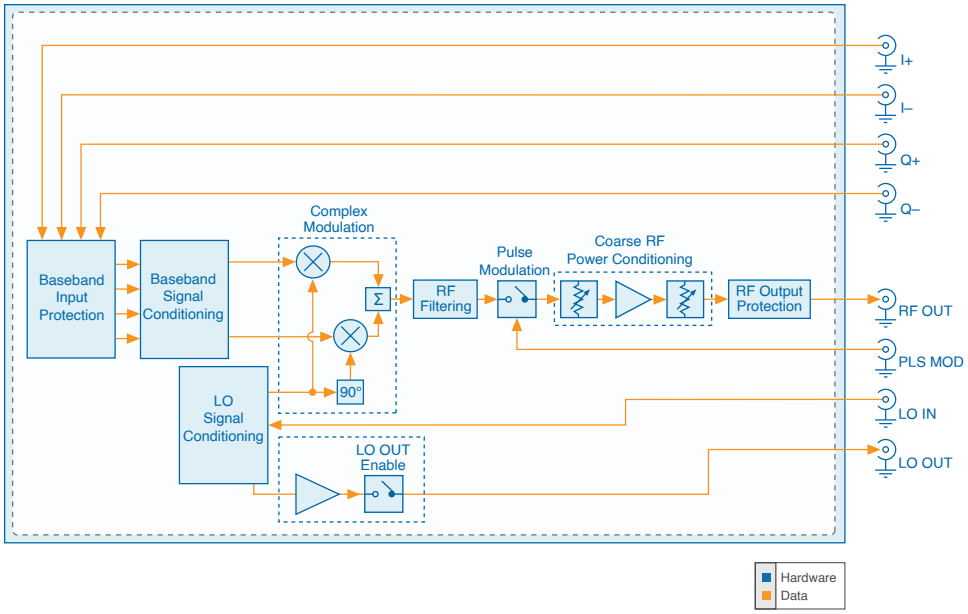
If your application requires arbitrary waveform playback over long time durations without looping, choose a larger AWG module onboard waveform memory option. For example, 256 MB of onboard memory can store approximately 1.28 s of waveform data at an I/Q rate of 100 MS/s.

Note Not all onboard memory is available for waveform storage. A portion of onboard memory stores scripts that specify how the waveforms are generated. These scripts typically require less than 1 KB of onboard memory.

PXIe-5611 Block Diagram

This topic contains information about the PXIe-5611 I/Q Modulator top-level block diagram and descriptions of the individual blocks.

Figure 9. PXIe-5611 Block Diagram



The following list describes the individual blocks:

- ***Baseband input*** protects the baseband input circuit from potential damage.
- ***Baseband signal conditioning*** sets the proper level and bias for complex modulation.
- ***Complex modulation*** is the core function of the I/Q modulator and imparts complex baseband information to the LO IN signal.
- ***RF filtering*** reduces the harmonic content of the RF OUT signal.
- ***Pulse modulation***passes or interrupts the RF OUT signal under hardware control.
- ***Coarse RF power conditioning*** sets the level of the RF OUT signal in 1 dB increments.
- ***RF output protection*** protects the RF output circuit from potential damage.

- ***LO signal conditioning*** the LO IN signal in order to reduce harmonic content, thereby improving complex modulation. LO signal conditioning also level the gain from LO IN to LO OUT and enables or disables the LO OUT signal.

Baseband Input Protection

Baseband input protection, when activated, interrupts the I+, I-, Q+, and Q- front panel connectors. Baseband input protection protects the input stage from potential damage due to the application of high signal levels. Baseband input protection is automatically enabled when input signals of ±2.8 Vpeak (+19 dBm for a CW sinusoidal input) or higher are applied. Subsequently, the front panel connectors are interrupted and do not return to normal function until you remove the offending input signal and reset the device.

Pulse Modulation

Pulse modulation passes or interrupts the RF OUT signal under external (hardware) control. Pulse modulation imparts high-speed on/off modulation to the RF OUT signal, either independently or in conjunction with complex modulation. A 3.3 V TTL signal applied to the PLS MOD front panel connector controls pulse modulation. Pulse modulation provides a means of switching the RF OUT signal on or off independent of complex modulation. When no signal is applied to the PLS MOD connector and pulse modulation is disabled, the RF OUT signal operates normally.

You can use NI-RFSG to enable pulse modulation.

Complex Modulation

Complex modulation is the core function of the PXIe-5611 I/Q Modulator. Complex modulation imparts the complex baseband information present on the I+, I-, Q+, and Q- front panel connectors on the PXIe-5611 module to the LO IN signal to produce the complex-modulated RF OUT signal.

RF Output Protection

RF output protection protects the RF OUT circuit on the PXIe-5611 I/Q Modulator. When this feature is automatically activated, it reflects RF power that is incident on the RF OUT front panel connector. RF output protection protects the RF output stage from potential damage due to the application of high levels of reverse RF power at the RF OUT front panel connector.

This feature is automatically enabled when more than 1 W of reverse RF power is detected. The RF output stage is then internally disconnected from the RF OUT connector. The RF OUT connector does not return to normal function until you remove the offending reverse RF power and reset the module.

RF Filtering

RF filtering filters the RF OUT signal to reduce harmonic content. RF filtering produces a spectrally purer RF OUT signal, but if uncorrected on very broadband modulations, RF filtering may introduce small amounts of amplitude and/or group delay distortion. NI-RFSG automatically selects the appropriate filter.

LO OUT

The PXI/PXIe-5650/5651/5652 RF Analog Signal Generator acts as the LO source for the PXIe-5673/5673E Vector Signal Generator. The PXI/PXIe-5650/5651/5652 RF OUT front panel connector passes the LO signal to the LO IN front panel connector on the PXIe-5611 I/Q Modulator. The PXIe-5611 module filters and adjusts the gain of the LO signal before using the LO signal as the carrier. The PXIe-5611 also provides a copy of the filtered and gain-adjusted signal at the LO OUT front panel connector.

The power levels at the PXIe-5611 LO IN and LO OUT front panel connectors are nominally set to 0 dBm. Refer to the specifications document specific to your device for more information about power levels. The PXIe-5611 LO IN to LO OUT gain is characterized at NI during the manufacturing process or during an annual external calibration. The calibration procedure involves the use of a power meter. When the proper gain is measured, it is stored on the PXIe-5611 where it is used to correct each generated signal.

LO IN to LO OUT calibration is automatically applied to every signal generated by the

PXIe-5673/5673E. The gain varies over carrier frequency, and multiple gain values are stored on the PXIe-5673/5673E. Interpolation is automatically performed when the generated signal frequency does not exactly match a frequency point where the gain is stored. Temperature drift correction is also performed on gain. Each time a session is initialized, the onboard temperature is read and used to correct the stored gain value according to the temperature coefficients stored alongside the gain. Use NI-RFSG to correct for temperature drift without having to reinitialize a session. You can also use NI-RFSG to read the expected output power at the PXIe-5611 LO OUT front panel connector. Multiple-input-multiple-output (MIMO) systems might require further control of LO IN to LO OUT gain and/or PXI/PXIe-5650/5651/5652 output power level.

The amount of gain needed from LO IN to LO OUT front panel connector on the PXIe-5611 is determined by the value of the LO In Power property or NIRFSG_ATTR_LO_IN_POWER attribute. If you select the PXI/PXIe-5652 as the LO source for the PXIe-5673/5673E in MAX, then the LO In Power property or NIRFSG_ATTR_LO_IN_POWER attribute is read-only and is automatically assigned the expected RF OUT power passed out of the PXI/PXIe-5650/5651/5652. If you select an external LO source, the LO In Power property or NIRFSG_ATTR_LO_IN_POWER attribute is read/write.

You can assign the anticipated input power at the PXIe-5611 LO IN front panel connector using NI-RFSG so that the PXIe-5611 returns 0 dBm of power. Refer to the specifications document specific to your device for information about the expected level accuracy. Maintain the power applied at the PXIe-5611 LO IN front panel connector at 0 dBm, ±1 dBm. If the PXIe-5611 does not return 0 dBm (to within its accuracy) for a given LO IN power level, NI-RFSG returns a warning.

LO Signal Conditioning

LO signal conditioning filters the LO IN signal in order to reduce harmonic content. LO signal conditioning sets the proper levels of the internal LO signal and LO OUT signal, and LO signal conditioning also enables or disables the LO OUT signal. LO signal conditioning also improves complex modulation performance by reducing the sensitivity to variations in the LO IN signal. NI-RFSG automatically selects the LO signal conditioning settings.

RF OUT Power Conditioning

RF OUT power conditioning is performed by a set of programmable attenuators. Coarse RF OUT power conditioning sets the level of the RF OUT signal in 1 dB increments. Fine (vernier) control of the RF OUT power within steps of coarse RF power conditioning is realized by the AWG module.

Controlling RF OUT Power Conditioning

You can control this feature by specifying an RF OUT level using the Power Level property or NIRFSG_ATTR_POWER_LEVEL attribute. NI-RFSG then chooses the appropriate attenuator and DSP settings.

Baseband Signal Conditioning

Differential amplifiers and a selectable reference voltage source perform baseband signal conditioning on the PXIe-5611 I/Q Modulator. Baseband signal conditioning sets the proper levels and bias for complex modulation.

Temperature Monitoring

The PXIe-5611 I/Q Modulator includes a temperature sensor located inside the metal enclosure that monitors the RF analog circuitry temperature. NI-RFSG can poll the temperature sensor to correct for amplitude and impairment deviations as the temperature of the metal enclosure changes. The effects of temperature drift are automatically compensated for each time an NI-RFSG VI or function is called that adjusts the configuration of the device.

The PXI/PXIe-5650/5652/5652 RF Analog Signal Generator output power adjusts to compensate for the drift in the PXIe-5611 LO path so that the PXI/PXIe-5650/5651/5652 receives a constant LO power level. The PXIe-5611 output power corrects for temperature drift by adjusting the PXIe-5450/5451 Waveform Generator output power and attenuators in the PXIe-5611 output path, if necessary. Digital signal processing in the PXIe-5450/5451 corrects modulation impairments for temperature.

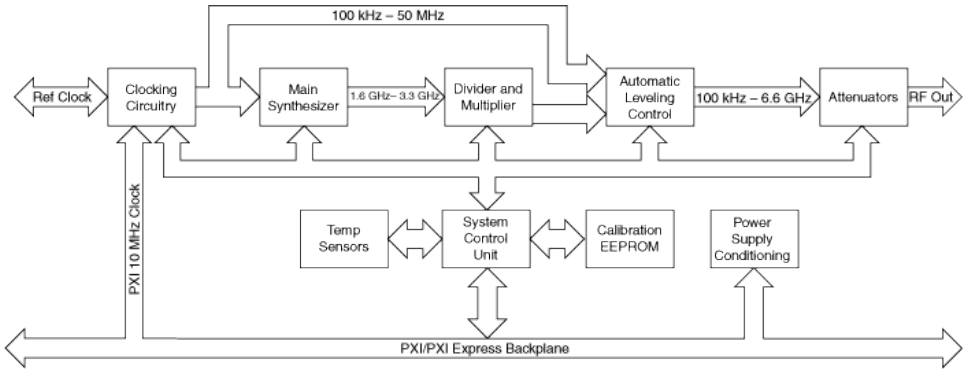
Querying the value of the device temperature using NI-RFSG returns the temperature within the NI 5611 RF enclosure. A second temperature sensor is located outside the RF enclosure, but this sensor is not readable with NI-RFSG. If this sensor reads unsafe temperatures, it shuts down the device power rails to power off the RF enclosure and protects the RF circuitry from damage.

NI-RFSG returns an error after the device powers off, and you must perform a device reset in order to restore power to the RF enclosure.

PXI/PXIe-5650/5651/5652 RF Analog Signal Generators

PXI/PXIe-5650/5651/5652 Block Diagram

This topic contains information about the PXI/PXIe-5650/5651/5652 RF Analog Signal Generator top-level block diagram and descriptions of the individual blocks.



The system control unit manages the control signals and data transferred between the circuit blocks. The system control unit contains all the necessary registers for device control from the host computer. Additionally, the system control unit contains the temperature monitor and modulation components. The following list describes the individual blocks of the PXI/PXIe-5650/5651/5652:

- ***Clocking circuitry*** contains the system clock reference and the direct digital synthesizer (DDS). The system clock is a 200 MHz voltage-controlled crystal oscillator (VCXO) that can be programmed to phase-lock to an external 10 MHz clock signal, present at the REF IN/OUT front panel connector. The DDS clocked by the 200 MHz reference provides signals of up to 10 MHz, with very fine frequency steps. RF signals below 50 MHz come directly from the DDS.
- Above 50 MHz, signal generation occurs inside the ***main synthesizer circuit***. The synthesizer is phase-locked to the DDS output signal as a reference. This DDS reference signal delivers the necessary fine tuning steps of the synthesizer; the synthesized RF frequency steps are typically 1 Hz or less.

- Following the main synthesizer are ***dividers*** and ***multipliers*** to scale the frequency over the range of 50 MHz to the upper frequency limit of the PXI/PXIe-5650/5651/5652. Lowpass or bandpass filters are implemented after the dividers and multipliers that cover every suboctave band. For example, for the PXI/PXIe-5651, a division ratio of 16 results in the octave range of 100 MHz to 200 MHz, and two lowpass filters cover the 100 MHz to 140 MHz and 140 MHz to 200 MHz frequency ranges, respectively. The filters ensure adequate suppression of the second harmonic throughout the band. Similarly, during multiplication, the subharmonics are improved at certain frequencies. The worst-case harmonics are specified in the specifications document for the PXI/PXIe-5650/5651/5652.
- The ***automatic leveling control*** (ALC) loop performs fine amplitude control. The ALC has a very broad frequency response, typically from 100 kHz to over 6.6 GHz. The reference for the ALC is set by a temperature-stable voltage DAC. Additional temperature calibration performed during the manufacturing process makes the ALC very stable over the specified operating temperature.
- The final block of the system includes the attenuators. The attenuators have a typical range of 100 dB. However, at higher frequencies, reduced isolation limits the range. Thus, the lowest achievable power level increases as the frequency increases.

NI-RFSG uses the calibration data stored in the EEPROM to correctly set up the hardware for signal generation. NI-RFSG uses the calibration data to compensate for non-ideal components and temperature variation.

Power On and Reset Conditions

The PXI/PXIe-5650/5651/5652 RF Analog Signal Generator hardware is in the following state after powering on or restarting the system and allowing the PC operating system and NI-RFSG to fully load. These conditions are also true after a device reset that you perform directly from NI Measurement & Automation Explorer (MAX).

- The REF IN/OUT connector is configured as an input.
- The REF OUT2 connector, if applicable, is inactive.
- The VCXO Reference Clock is free running and its frequency is uncalibrated.
- The DDS is inactive.
- The main synthesizer is off.

- The DDS signal path is selected.
- The ALC is set for minimum amplitude.
- All attenuators are fully asserted.
- Thermal shutdown monitoring is activated.

Power Level Adjustment

The automatic leveling control (ALC) loop performs fine amplitude adjustment, and the attenuators perform coarse attenuation. The ALC is calibrated for amplitude and temperature variation and is used to control the upper 10 dB. When possible, NI-RFSG uses only the ALC to get the specified power. However, if more than 10 dB of attenuation is needed at the specified frequency[1], then the attenuators are used. For this reason, signal amplitude has best absolute and relative accuracy at the uppermost 10 dB, which is typically better than specified. Below the first 10 dB of power, the attenuators assert and error increases.

Note Refer to your device specifications document for guaranteed output power ranges.

Modulation Schemes

The PXI/PXIe-5650/5651/5652 RF signal generator can generate the following types of modulation signals:

- Frequency modulated (FM) signals
- Frequency shift keying (FSK) signals
- On-off keying (OOK) signals
- Phase modulated (PM) signals
- Phase-shift keying (PSK) signals

Frequency Modulation (FM)

FM is a form of modulation in which changes in the frequency of the carrier wave

1. Power range varies depending on frequency.

correspond directly with changes in the baseband signal.

You can control the following modulation parameters:

- Internal modulation waveform types: square, sine, triangle
- Modulation waveform frequency
- FM deviation

The valid modulation waveform frequency (modulation rate) range is expressed in the following equation:

Modulation Rate = 50 MHz / n × m

where

- $1 \leq n < 2^{16}$
- $10 \leq m \leq 2{,}038$ or
- $10 \leq m \leq 1{,}020$ (for square modulation waveforms)
- m is the number of samples per waveform, which is optimized by NI-RFSG to produce the most linear waveform for a desired rate. Also, m is always an even number for the FM rate calculation.

Note The maximum recommended waveform frequency is 100 kHz. Higher frequencies are possible but produce degraded modulation accuracy.

Frequency-Shift Keying (FSK)

FSK is a type of frequency modulation that assigns bit values to discrete frequency levels. The PXI/PXIe-5650/5651/5652 is capable of producing a 2-FSK signal.

You can control the following modulation parameters:

- Internal modulation waveform types: user-defined bit stream or pseudorandom bit sequence (PRBS)
- Symbol rate
- FSK deviation

NI-RFSG calculates the exact symbol rate and FSK deviation, which can differ slightly from the input parameters.

For user-defined bit streams, the valid symbol rate range and bit stream length are determined by the following relations:

$1 \le \textbf{\textit{bit stream length}} \le 1{,}022$

Symbol rate = 50 MHz / (n × m)

where

- $5 \le n < 2^{16}$
- $1 \le m \le \text{floor}(1{,}022 / \textbf{\textit{bit stream length}})$

For PRBS: Symbol rate = 10 MHz/n

where

$1 \le n < 2^{16}$

Note The maximum recommended waveform frequency is 100 kHz. Higher frequencies are possible but produce degraded modulation accuracy.

On-Off Keying (OOK)

OOK is a modulation scheme that varies the power level of the carrier signal between two discrete power levels.

You can control the following modulation parameters:

- Internal modulation waveform type: 1,024-bit user-defined bit-stream or PRBS
- Symbol rate

A bit value of 1 sets the carrier signal power to the value configured by the Power Level property or the NIRFSG_ATTR_POWER_LEVEL attribute. A bit value of 0 sets the carrier

signal power to the lowest possible level for this frequency.

During a bit value of 1 (high power level), the PXI/PXIe-5650/5651/5652 bypasses the main attenuators. Therefore, the high power level range is limited by the power level range of the ALC. The supported OOK high power level range is from the maximum specified power level for this frequency to approximately 10 dB lower than the maximum specified power. Refer to the specifications document for your device for minimum and maximum power levels.

For user-defined bit streams, the valid symbol rate range and bit stream length are related in the following equations:

$1 \le \textbf{\textit{bit stream length}} \le 1{,}024$

Symbol rate = 10 MHz / (n × m)

where

- $5 \le n < 2^{16}$
- $1 \le m \le \text{floor}(1{,}022 / \textbf{\textit{bit stream length}})$

For PRBS: Symbol rate = 10 MHz/n

where

$1 \le n < 2^{16}$

The symbol rate is determined by a programmable 16-bit register, as indicated in the following equation:

PRBS symbol rate - 10 MHz/n

where

$1 \le n < 2^{16}$

Note The maximum recommended waveform frequency is 100 kHz. Higher

frequencies are possible but produce degraded modulation accuracy.

Phase Modulation (PM)

PM is a form of modulation in which changes in the phase of the carrier wave correspond directly with changes in the baseband signal.

You can control the following modulation parameters:

- Internal modulation waveform types: square, sine, triangle
- Modulation waveform frequency
- PM deviation

The valid modulation waveform frequency (modulation rate) range is expressed in the following equation:

Modulation Rate = 50 MHz / n × m

where

- $1 \leq n < 2^{16}$
- $10 \leq m \leq 2{,}038$ or
- $10 \leq m \leq 1{,}020$ (for square modulation waveforms)
- m is the number of samples per waveform, which is optimized by NI-RFSG to produce the most linear waveform for a desired rate. Also, m is always an even number for the PM rate calculation.

Note The maximum recommended waveform frequency is 100 kHz. Higher frequencies are possible but produce degraded modulation accuracy.

Phase-Shift Keying (PSK)

PSK in digital transmission refers to a type of angle modulation in which the phase of the carrier is discretely varied to represent data being transmitted-either in relation to a reference phase or to the phase of the immediately preceding signal element. The

PXI/PXIe-5650/5651/5652 is capable of producing a 2-PSK signal.

You can control the following modulation parameters:

- Internal modulation waveform types: user-defined bit stream or pseudorandom bit sequence (PRBS)
- Symbol rate

NI-RFSG calculates the exact symbol rate and PSK deviation, which can differ slightly from the input parameters.

For user-defined bit streams, the valid symbol rate range and bit stream length are determined by the following relations:

$1 \le \textbf{\textit{bit stream length}} \le 1{,}022$

Symbol rate = 50 MHz / (n × m)

where

- $5 \le n < 2^{16}$
- $1 \le m \le \text{floor}(1{,}022 / \textbf{\textit{bit stream length}})$

For PRBS: Symbol rate = 10 MHz/n

where

$1 \le n < 2^{16}$

Note The maximum recommended waveform frequency is 100 kHz. Higher frequencies are possible but produce degraded modulation accuracy.

Modulation Implementation

The main synthesizer has two modes: narrow and wide, corresponding to approximately 20 kHz and 200 kHz loop bandwidths, respectively. By default, during

single tone (sine) generation, NI-RFSG selects the low loop bandwidth for the best possible phase noise performance. The specified phase noise is based on low loop bandwidth. Using NI-RFSG, you can select wide loop bandwidth, which trades off phase noise between 3 kHz to 300 kHz offsets for faster tuning times.

The modulation implemented on the PXI/PXIe-5650/5651/5652 requires that the wide loop bandwidth is used, except for OOK modulation. Choosing wide loop bandwidth increases phase noise from 20 kHz and outward; the phase noise close to the carrier does not change. Loop bandwidths do not affect far out noise density, and the far out noise of the system remains unchanged.

All frequency modulation occurs within the phase-locked loop (PLL) of the main synthesizer circuitry. Changing the direct digital synthesis (DDS) reference frequency directly modulates the generated signal. In effect, controlling the frequency of the DDS controls the frequency of the generated RF signal. The PLL bandwidth of the main synthesizer is set to wide loop bandwidth when modulation is turned on to accommodate high modulation rates. During normal operation, with modulation turned off, the loop bandwidth setting returns to narrow loop bandwidth.

Sinusoidal Tone Versus Modulation Operation

The main synthesizer has two modes: narrow and wide, corresponding to 10 kHz and 200 kHz loop bandwidths, respectively. During single tone (sine) generation, the narrow loop bandwidth is selected for the best possible phase noise performance. The specified phase noise is based on narrow loop bandwidth. Override the loop bandwidth defaults if your application requires it.

Ideally, narrow loop bandwidth should be used when modulation is turned on; however, the modulation implemented on the PXI/PXIe-5650/5651/5652 requires that the wide loop bandwidth is used, except for OOK modulation. Choosing wide loop bandwidth increases phase noise from 20 kHz and greater; the phase noise close to the carrier does not change. Loop bandwidths do not affect far out noise density; that is, the far out noise of the system remains unchanged.

Temperature Monitoring

The PXI/PXIe-5650/5651/5652 hardware module includes two temperature sensors. One sensor is located inside the metal enclosure and monitors the RF analog circuitry temperature. Query this temperature sensor using NI-RFSG. NI-RFSG polls the temperature sensor at defined intervals to correct for amplitude and frequency deviations as the temperature of the metal enclosure changes.

The second temperature sensor is located outside the RF enclosure and monitors the temperature of the digital interface circuitry. This sensor is polled by the PXI/PXIe-5650/5651/5652 system control unit (not the instrument driver). If this sensor reads temperatures above 75 °C, it shuts down the PXI or PXI Express power rails to power off the RF enclosure and protect the RF circuitry from damage. When this sensor reads 75 °C on the digital circuit board, the temperature inside the metal RF enclosure is close to 80 °C.

Querying Device Temperature

Query the value of the Device Temperature property or the NIRFSG_ATTR_DEVICE_TEMPERATURE attribute to return the temperature within the PXIe-5673/5673E RF enclosure.

This metal enclosure contains the RF circuitry.

Note

Serial signals between the sensor and the system control unit could potentially modulate the signal being generated, causing phase spurs. After the device is thoroughly warmed up, its temperature varies only slightly and slowly, so it is not necessary to constantly poll this temperature sensor.

Querying the device temperature returns the previous sensor reading until at least one minute has passed since the previous sensor reading occurred.

Thermal Shutdown

NI-RFSG supports thermal shutdown monitoring for NI RF signal generator modules. This feature allows the module to detect when it has reached a dangerously high temperature and to then power off, preventing damage to the device.

If safe temperature limits are exceeded, the RF enclosure is powered off, and NI-RFSG returns an error.

> **Note** The PXIe-5673/5673E is warm to the touch during normal operation. The device should never reach a temperature high enough to cause thermal shutdown unless the fan or vents on the PXI or PXI Express chassis are blocked or the filters on the fans are excessively dusty.

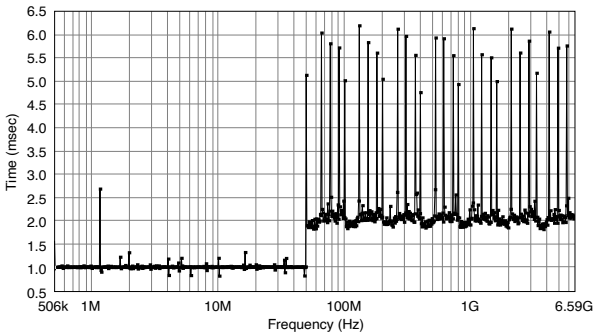
Re-enabling the Device After Thermal Shutdown

Complete the following steps to restore power to the RF enclosure:

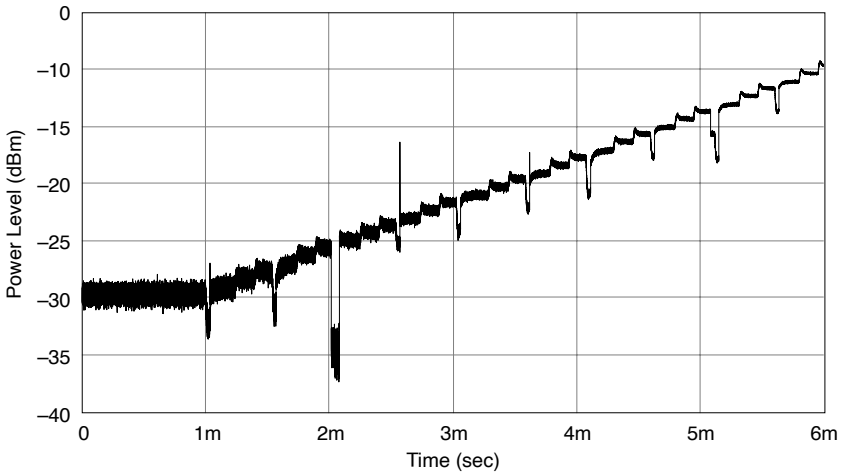
1. Ensure the filters are clean and that you have a clear path for airflow through your PXI or PXI Express chassis.
2. Review the guidelines in the ***Maintain Forced-Air Cooling Note to Users*** that shipped with the device, and make any necessary adjustments to ensure that the chassis can cool the device effectively.
3. Perform a device reset in MAX by selecting the device in the MAX configuration tree and clicking **Reset** from the MAX toolbar.
4. Repeat step 3 for each hardware module.

Frequency Tuning Times

The following plot shows typical PXI/PXIe-5650/5651/5652 frequency sweep tuning times (to within approximately 1 ppm of the requested frequency.



You may experience overshoot or undershoot when changing power level settings, as shown in the following plot. The following plot shows a 1 GHz signal swept from -30 dBm to -10 dBm in 1 dB steps.



PXI/PXIe-5650/5651/5652 Noise Floor and Signal-to-Noise Ratio

Noise floor changes as signal amplitude changes. For instance, the noise floor may be -150 dBm/Hz for a signal level of -5 dBm, and it may increase to -140 dBm/Hz for a signal level of 5 dBm. It may seem that the latter signal has less integrity, but this is not the case because (assuming all other factors are equal) the signal dynamic range is still 145 dBc/Hz. Consequently, the signal-to-noise ratio (SNR) is specified, but the noise floor of the product is not.

While SNR is not the same for all signal levels, it remains relatively constant until the absolute noise density is at or below the theoretical limit of -173.8 dBm/Hz at room temperature. Beyond this limit, the SNR decreases one-to-one with signal level.

PXI/PXIe-5650/5651/5652 Factory Calibration

NI performs calibration of the PXI/PXIe-5650/5651/5652 that is relative to an NIST-traceable standard over the specified operating temperature range. Calibration

consists of two major parts: frequency accuracy calibration and amplitude accuracy calibration.

For frequency accuracy, the 200 MHz system clock is calibrated against an NIST-traceable rubidium clock at room temperature and over the PXI/PXIe-5650/5651/5652 operating temperature range. It is important that the PXI/PXIe-5650/5651/5652 temperature stabilizes before critical frequency accuracy measurements are taken. Although the PXI/PXIe-5650/5651/5652 Reference Clock is sensitive to rapid changes in temperature, it has a slow response because its temperature varies with that of the metal RF enclosure, which has a high thermal inertia and therefore responds slowly to ambient temperature changes.

For amplitude accuracy, the ALC and attenuators are calibrated over the entire specified temperature range. The amplitude accuracy is calibrated against an NIST-traceable power meter for power levels greater than -40 dBm. For power levels below -40 dBm, a signal analyzer is used to make measurements relative to 0 dBm absolute. The accuracy of the power measurement for signals less than -40 dBm is thus dependent upon the relative accuracy of the signal analyzer. The relative accuracy of the signal analyzer is a function of its ADC linearity.

Note Refer to the specifications document for your device for detailed PXI/PXIe-5650/5651/5652 specifications.

Notice Opening the RF enclosure invalidates factory calibration. To preserve guaranteed calibration, do not disassemble the PXI/PXIe-5650/5651/5652 RF enclosure.

Device Warm-Up

NI recommends warming up the PXI/PXIe-5650/5651/5652 hardware for 30 minutes before operation.

The unit is fully functional prior to this time, but frequency, amplitude accuracy, and other specifications are not at warranted levels until the device has fully completed warming up.

Note Warm up begins when the PXI or PXI Express chassis has been powered on and the operating system has completely loaded.

Generation Modes

The PXIe-5673/5673E has the following three available generation modes:

- **CW mode**—NI-RFSG software internally generates a continuous-wave signal (a sine tone). In this mode, a DC signal is returned from the AWG, and the I/Q modulator provides a fixed amplitude and phase adjustment to the LO signal to produce the RF OUT signal. The I data written to the AWG is full-scale binary data, and the Q data written to the AWG is set to zero. The signal passing through the I+, I-, Q+, and Q- connectors depends primarily on the phase offset setting. The signal is also impacted by the factors such as impairment calibration, user-specified impairments, prefilter gain, and requested power level.
- **Arb waveform mode**—User-provided complex I/Q baseband signals are upconverted to RF. In this mode, signal bandwidth, I/Q rate, and digital equalization settings are configurable. Output frequency relates to the center frequency. Power settings relate to the power of the specified arbitrary waveform, depending on the setting of the Power Level Type property or the NIRFSG_ATTR_POWER_LEVEL_TYPE attribute.
- **Script mode**—Scripts specify dynamic waveform generation operations. For example, a script could configure the device to generate waveform A, then wait for the Script Trigger, then generate waveform B.

Peer-to-Peer Data Streaming

The PXIe-5673E Vector Signal Generator supports peer-to-peer (P2P) data streaming using the NI-P2P API. Peer-to-peer streaming exchanges data directly between supported devices, bypassing the host computer memory and making applications that require real-time data transfer between devices possible.

For more information about the following terminology, refer to the ***Understanding the Peer-to-Peer Data Streaming*** topic in the ***NI Peer To Peer Streaming Help***.

- **Stream**—The data path connection between two peer-to-peer endpoints. A peer-to-peer stream is independent of the data generation and consumption of the two peers.
- **Endpoint**—The collection of hardware resources needed to support one end of a peer-to-peer stream. Multiple peer-to-peer endpoints may exist in a single device.
- **Writer Peer**—The peer sending the data over the bus to the reader peer.
- **Reader Peer**—The peer receiving the data over the bus from the writer peer.

NI RF signal generators assume the role of the reader peer endpoint in a peer-to-peer stream because they read data from the writer peer through the peer-to-peer stream and then pass the data to physical channels.

Configuring a Peer-to-Peer Endpoint

Any NI-RFSG property that is associated with an instance of an endpoint is an endpoint-based property.

1. Set the Active Channel property using an appropriate string when configuring endpoint-based properties.
   The syntax "`FIFOEndpointN`" is used to tell NI-RFSG which RF signal generator endpoint is being specified, where N is an integer starting with 0. If the RF signal generator supports multiple endpoints, the first is "`FIFOEndpoint0`", the second

is "`FIFOendpoint1`", and so on.

2. To determine how many endpoints your RF signal generator supports, query the Endpoint Count property.
3. To use peer-to-peer in NI-RFSG, set the Generation Mode property to **Script**. Use the script instruction stream n, where n is an integer number of samples to stream from an endpoint to the RF output channels.
4. To stream continuously until the generation is aborted from the host or by a peer, create a script that nests the `stream n` command in a `repeat forever` loop, as shown in the following example.

```
Script myScript
  repeat forever
    stream 10240
  end repeat
end script
```

Configuring a Peer-to-Peer Stream

To configure a peer-to-peer stream using the NI-P2P API, a writer and reader handle for each endpoint are required.

Use Get Stream Endpoint Handle to generate a reader endpoint handle.

Configuring Flow Control

When streaming data between two peers, the writer peer must have flow control ***credits*** to move data over the bus to the reader peer. The reader peer issues credits to the writer peer through control messages across the bus when there is space available in the configured endpoint for the reader peer.

The RF signal generator issues credits in the following two ways:

- When the stream is initially enabled, the peer issues credits equal to the value of the Data Transfer Permission Initial Credits property or the NIRFSG_ATTR_P2P_DATA_TRANSFER_PERMISSION_INITIAL_CREDITS attribute. If this property or attribute is not set, the RF signal generator issues a default value equal to the depth of the endpoint to the peer to minimize the chance of underflowing the RF signal generator. (Underflow can be caused by heavy bus

traffic.)

- As data flows from the endpoint to the physical channel(s) on the RF signal generator, additional credits are issued to the writer peer. These credits are issued in intervals equal to the value of the Data Transfer Permission Interval property or the NIRFSG_ATTR_P2P_DATA_TRANSFER_PERMISSION_INTERVAL attribute and are issued only when an amount of data greater than or equal to this value is generated at the physical channels on the RF signal generator.

Note The endpoint could already contain data when the initial flow control credits are issued. This scenario could be caused by data written from the host using the niRFSG Write P2P Endpoint (I16) VI or the niRFSG_WriteP2PEndpointI16 function or from a previous streaming operation. In this case, NI-RFSG adjusts the default initial credits to issue, at most, the difference between the endpoint depth and the amount of data already in the endpoint.

1. Configure NI-P2P with information regarding each endpoint to link the endpoints into a stream, using the niP2P Create Peer to Peer Stream VI or the nip2pCreateStream function. You must specify both a reader and writer endpoint handle.
2. Use the niRFSG Get Stream Endpoint Handle VI or the niRFSG_GetStreamEndpointHandle function to get the RF signal generator reader handle and the appropriate handle from the writer peer API.
3. Enable the stream using the niP2P Enable Peer to Peer Stream VI or the nip2pEnableStream function. After you enable the stream, the RF signal generator issues credits to the writer peer.

Starting Peer-to-Peer Generation

If the RF signal generator begins generating data from a peer-to-peer stream immediately after the first sample is received, the device may not have enough data to continue the generation and can underflow at startup. This problem is due to latency across the bus, and it is especially likely when heavy, possibly unrelated, traffic is on the bus. To avoid underflow at startup, prime the endpoint with data before starting generation so the device has a backlog of data to insulate the generation from the bursty nature of data flowing across the bus.

The following three methods are available for preparing the RF signal generator endpoint for startup:

- P2P Endpoint Fullness Start Trigger Level property or NIRFSG_ATTR_P2P_ENDPOINT_FULLNESS_START_TRIGGER_LEVEL attribute—Starts generation after the endpoint receives the specified number of samples. If no number of samples is specified, the driver automatically selects an appropriate value. This method should work for most applications and requires the least amount of configuration. This property or attribute is used when the Start Trigger Type property is set to Digital Edge or the NIRFSG_ATTR_START_TRIGGER_TYPE attribute is set to NIRFSG_VAL_DIGITAL_EDGE.
- niRFSG Write P2P Endpoint (I16) VI or niRFSG_WriteP2PEndpointI16 function—Primes the endpoint with initial data from the host to attempt to give the writer peer enough time to start sending data before the RF signal generator underflows.
- Manual preparation—Configure the application so that the writer peer sends data to the RF signal generator endpoint prior to the RF signal generator initiating generation by completing the following steps:
  1. Configure both peers for peer-to-peer streaming.
  2. Link both peers using the niP2P Create Peer to Peer Stream VI or nip2pCreateAndLinkStream function.
  3. Enable the stream either by setting **enable stream** to TRUE using the niP2P Create Peer to Peer Stream VI or nip2pCreateAndLinkStream function or by calling the niP2P Enable Peer to Peer Stream VI or nip2pEnableStream function.
  4. Start the writer peer first so that it begins sending data to the RF signal generator prior to initiation.
  5. Query the Space Available in Endpoint property or NIRFSG_ATTR_P2P_SPACE_AVAIL_IN_ENDPOINT attribute after starting the writer peer to ensure that sufficient data has been transferred to the RF signal generator.
  6. Call the niRFSG Initiate VI or niRFSG_Initiate function.

Note When using the P2P Endpoint Fullness Start Trigger Level property or NIRFSG_ATTR_P2P_ENDPOINT_FULLNESS_START_TRIGGER_LEVEL attribute

> after calling the niRFSG Initiate VI or niRFSG_Initiate function, approximately 2,300 bytes of the initial data received from the writer peer are routed into an internal data queue in the RF signal generator. If the writer peer writes 8,000 samples to an RF signal generator endpoint that has a size of approximately 32,000 samples, and then you query the Space Available in Endpoint property or NIRFSG_ATTR_P2P_SPACE_AVAIL_IN_ENDPOINT attribute, you receive about 25,000 samples instead of 24,000 because 1,000 samples were routed into the internal data queue. If your application requires starting the RF signal generator after a specific number of samples are received, adjust the P2P Endpoint Fullness Start Trigger Level property or NIRFSG_ATTR_P2P_ENDPOINT_FULLNESS_START_TRIGGER_LEVEL attribute value accordingly.

Stopping Peer-to-Peer Generation

Use either of the following techniques to stop peer-to-peer generation without generating an underflow error:

1. Infinite Generation with Done Notification—RF signal generators with peer-to-peer functionality support automatic Done Notification messages. The following steps occur if the writer peer also supports Done Notification messages:
   a. The RF signal generator automatically configures itself to receive the message when the two peers are linked using the niP2P Create Peer to Peer Stream VI or nip2pCreatePeertoPeerStream function.
   b. When the writer peer finishes sending data and disables the stream, a control message is sent across the bus. This message alerts the RF signal generator that the peer has no more data to send.
   c. The RF signal generator then waits until all data is sent out of the physical channels before it asserts the Done event.
   d. The RF signal generator transitions to the configured Idle Behavior.

   Applications between two NI devices, linked using NI-P2P, automatically use this behavior.

2. Finite Generation (`stream n`)—If the RF signal generator receives the specified number of samples from the writer peer, the NI-RFSG session completes without an underflow error.

In either preceding technique, use the niRFSG Check Generation Status VI or niRFSG_CheckGenerationStatus function to query the `done?` boolean, which specifies whether generation is complete. After generation is done, you can abort the generation using the niRFSG Abort VI or niRFSG_Abort function. When generation aborts, all data in the endpoint is cleared to prepare the device for subsequent generations.

Note When using the NI-P2P API to configure the stream, call the niP2P Flush and Disable Peer to Peer Stream VI or nip2pFlushAndDisableStream function or niP2P Disable Peer to Peer Stream VI or nip2pDisablePeertoPeerStream function and wait for the `done?` boolean parameter from the niRFSG Check Generation Status VI or niRFSG_CheckGenerationStatus to assert before aborting the RF signal generator. Disabling the stream alerts the writer peer to send the Done Notification and allows the RF signal generator to send out all data in the endpoint before transitioning to the Done state. If data is still in the endpoint when the niRFSG Abort VI or niRFSG_Abort function is called, it is cleared to prepare the device for subsequent generations.

Other Methods of Completion

There are other methods to stop generation that are not ideal, but may be suitable for some applications.

- User-Requested Abort—Using the niRFSG Abort VI or niRFSG_Abort function, the NI-RFSG session does not return an error and the niRFSG Check Generation Status VI or niRFSG_CheckGenerationStatus returns TRUE for `Done`. However, if the writer peer is not configured carefully for this event, it may overflow because the RF signal generator is no longer allowing it to send data through the stream.
- Infinite Generation without Done Notification—If the writer peer stops sending data and does not send a Done Notification message, the RF signal generator generates an underflow error after sending out the last of the data received without a configured Done Notification. NI-RFSG does not support determining if the underflow error is genuine or if the RF signal generator receives and sends out all of the expected data from the writer peer. However, if the generation proceeds without an underflow error up until the writer peer stopped sending data, the underflow error can likely be ignored. This method is not recommended, but it may be suitable for applications that cannot send Done Notifications but have a

method to determine if all data was sent.

Reconfiguring a Stream

Consider the following scenarios when reconfiguring an NI-RFSG session for peer-to-peer data streaming.

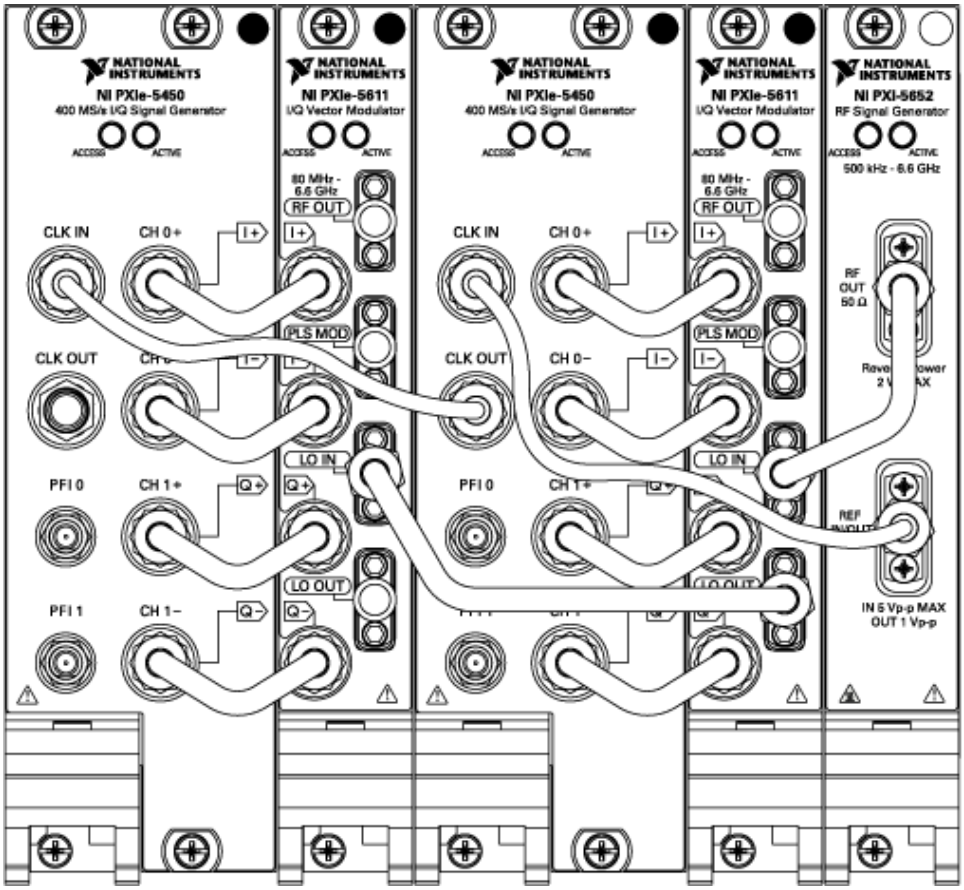
- If the generation from the previous session completed with Done Notification, the stream remains linked, but it is disabled. If you are using the P2P Endpoint Fullness Start Trigger Level property or NIRFSG_ATTR_P2P_ENDPOINT_FULLNESS_START_TRIGGER_LEVEL attribute, re-enable the stream using the P2P Enabled property or NIRFSG_ATTR_P2P_ENABLED attribute and initiate generation. If priming from the host using the niRFSG Write P2P Endpoint (I16) VI or niRFSG_WriteP2PEndpointI16 function, write to the endpoint again to prime it with data before re-enabling the stream and initiating generation.
- If the previous session was aborted, the stream remains intact and enabled. You must disable the stream, stop the writer peer data generation to avoid overflowing the writer peer endpoint, and then proceed as if the previous session completed with Done Notifications.

Advanced PXIe-5673 Configuration

Interconnecting Multiple PXIe-5673 Modules

The NI RF Signal Generators Getting Started Guide explains how to set up one PXIe-5673 Vector Signal Generator. NI-RFSG supports connecting multiple PXIe-5673 modules such as two PXIe-5611 I/Q Modulators and two PXIe-5450 Waveform Generators, as shown in the following figure.

> **Notice** You must install one PXIe-5673 before installing multiple modules. Refer to ***PXIe-5673E Getting Started*** for more information about installing one PXIe-5673.



Complete the following steps to interconnect multiple PXIe-5673 modules:

1. Install an additional PXIe-5611 immediately to the left of the previously installed PXIe-5450.
2. Install an additional PXIe-5450 immediately to the left of the PXIe-5611 installed in step 1.
3. Use Cable A to connect the CH 1-/Q- connector on the PXIe-5450 installed in step 2 to the Q- connector on the PXIe-5611 installed in step 1.
4. Use Cable A to connect the CH 1+/Q+ connector on the PXIe-5450 installed in step 2 to the Q+ connector on the PXIe-5611 installed in step 1.
5. Use Cable A to connect the CH 0-/I- connector on the PXIe-5450 installed in step 2 to the I- connector on the PXIe-5611 installed in step 1.
6. Use Cable A to connect the CH 0+/I+ connector on the PXIe-5450 installed in step 2 to the I+ connector on the PXIe-5611 installed in step 1.
7. Use a flexible cable to connect the CLK OUT connector on the first PXIe-5450 to the CLK IN connector on the PXIe-5450 installed in step 2.
8. Use Cable G to connect the LO OUT connector on the first PXIe-5611 to the LO IN connector on the PXIe-5611 installed in step 1.
9. Connect the 50 Ω terminator to the LO OUT connector on the PXIe-5611 installed in step 1.

After interconnecting multiple PXIe-5673 modules, configure the additional PXIe-5673 to use an External LO.

Related concepts:

- External LO

Related information:

- PXIe-5673E Getting Started

Timing Configurations for PXIe-5673 Modules

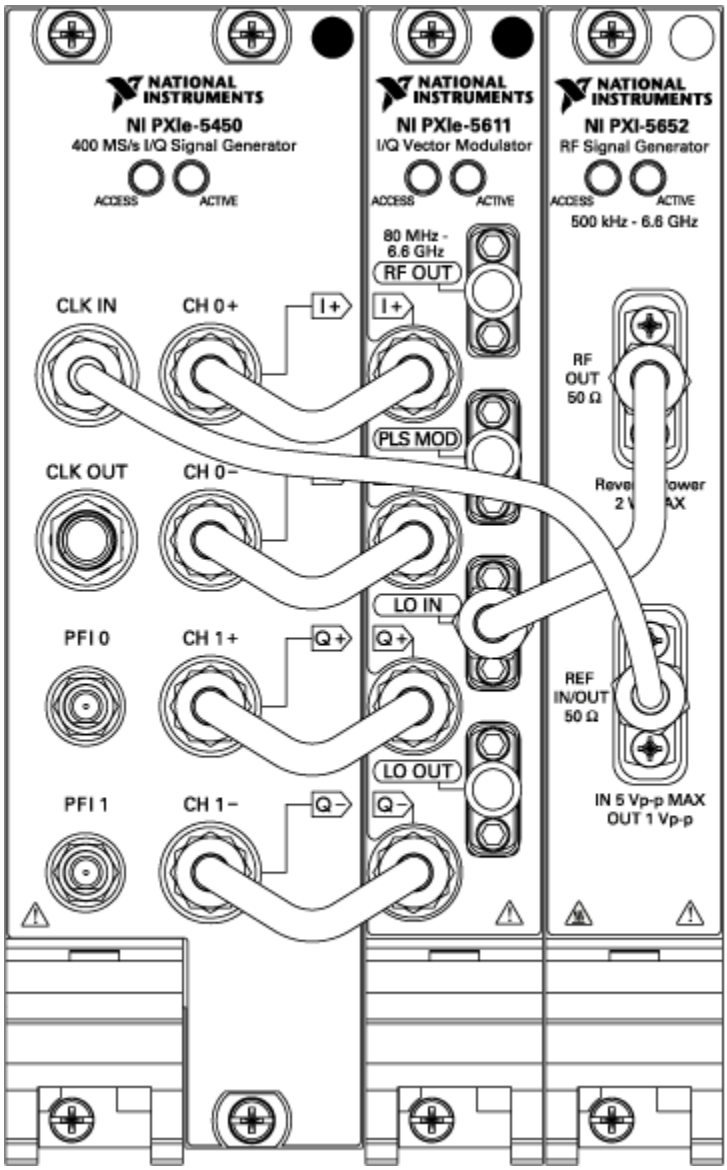
The timebases of the AWG module and the RF analog signal generator modules must be frequency-locked to a common 10 MHz Reference Clock. The following clock sources are available:

- Internal Reference Clock
- External Reference Clock
- PXI 10 MHz Backplane Clock

Configuring Internal Reference Clock Timing

The default configuration of the PXIe-5673 is for the PXI-5650/5651/5652 to export its internal Reference Clock to the PXIe-5450/5451 so that the PXIe-5450/5451 and the PXI-5650/5651/5652 devices are frequency-locked.

The default cable configuration is shown in the following figure.

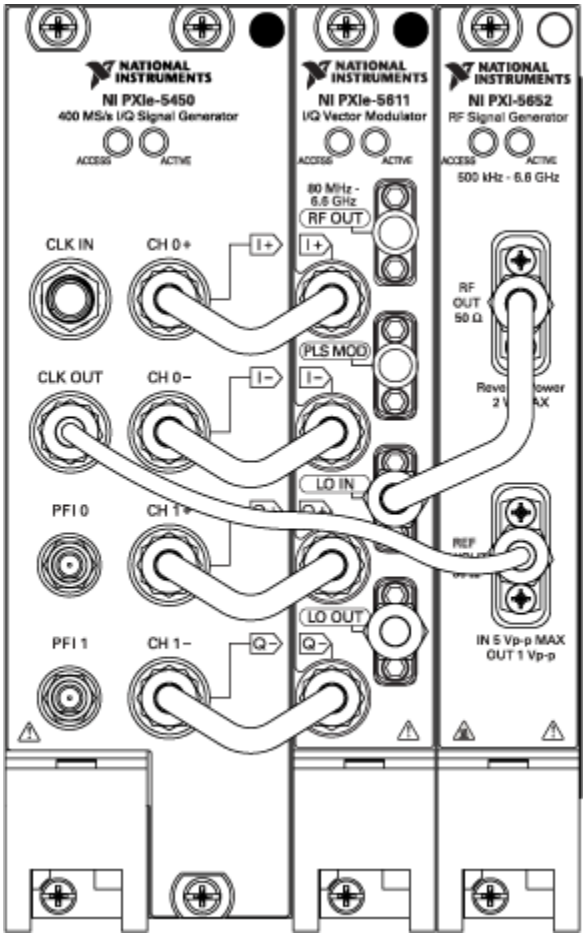


To configure the PXIe-5673 to use the internal clock, set the Reference Clock Source property to **OnBoardClock** or the `NIRFSG_ATTR_REF_CLOCK_SOURCE` attribute to `NIRFSG_VAL_ONBOARD_CLOCK_STR`.

Configuring External Reference Clock Timing

You can also configure the PXIe-5673 to lock to an external reference source.

The external Reference Clock timing cable configuration is shown in the following figure.



To configure the PXIe-5673 to use an external Reference Clock, set the Reference Clock Source property to **ClkIn** or the `NIRFSG_ATTR_REF_CLOCK_SOURCE` attribute to `NIRFSG_VAL_CLK_IN_STR`.

The phase noise of the system is also affected by external phase locking. Although the RF signal generator tries to minimize the effect of noisy references by using a very

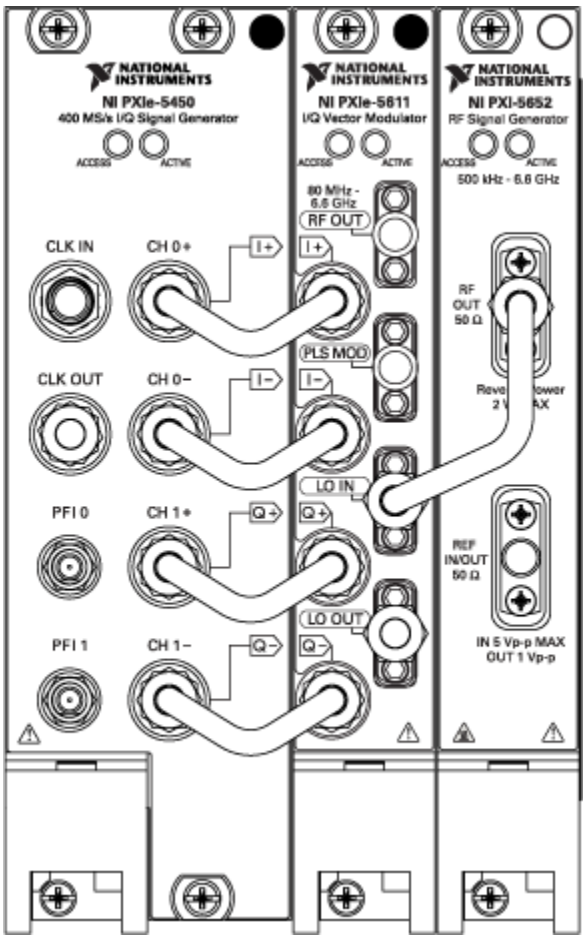
small phase-locked loop bandwidth, a considerable remnant may exist if the reference phase noise is 20 dB to 30 dB poorer than the upconverter module onboard OCXO. Some rubidium sources on the market have more phase noise than the upconverter module onboard reference but exhibit high long-term stability.

The external reference signal power level must be greater than -10 dBm or 0.2 V_{pk-pk} into 50 Ω.

Configuring PXI 10 MHz Backplane Clock Timing

You can also configure the PXIe-5673 to lock to the PXI 10 MHz backplane clock.

The configuration shown in the following figure locks the PXIe-5650/5651/5652 and PXIe-5450 to the PXI 10 MHz reference. Locking to the PXI 10 MHz reference does not require a cable, but this configuration does not provide the same frequency and phase noise performance as the PXI-5650/5651/5652 internal Reference Clock.



To configure the PXIe-5673 to use the PXI 10 MHz backplane clock, set the Reference Clock Source property to **PXI_CLK** or the `NIRFSG_ATTR_REF_CLOCK_SOURCE` attribute to `NIRFSG_VAL_PXI_CLK_STR`.

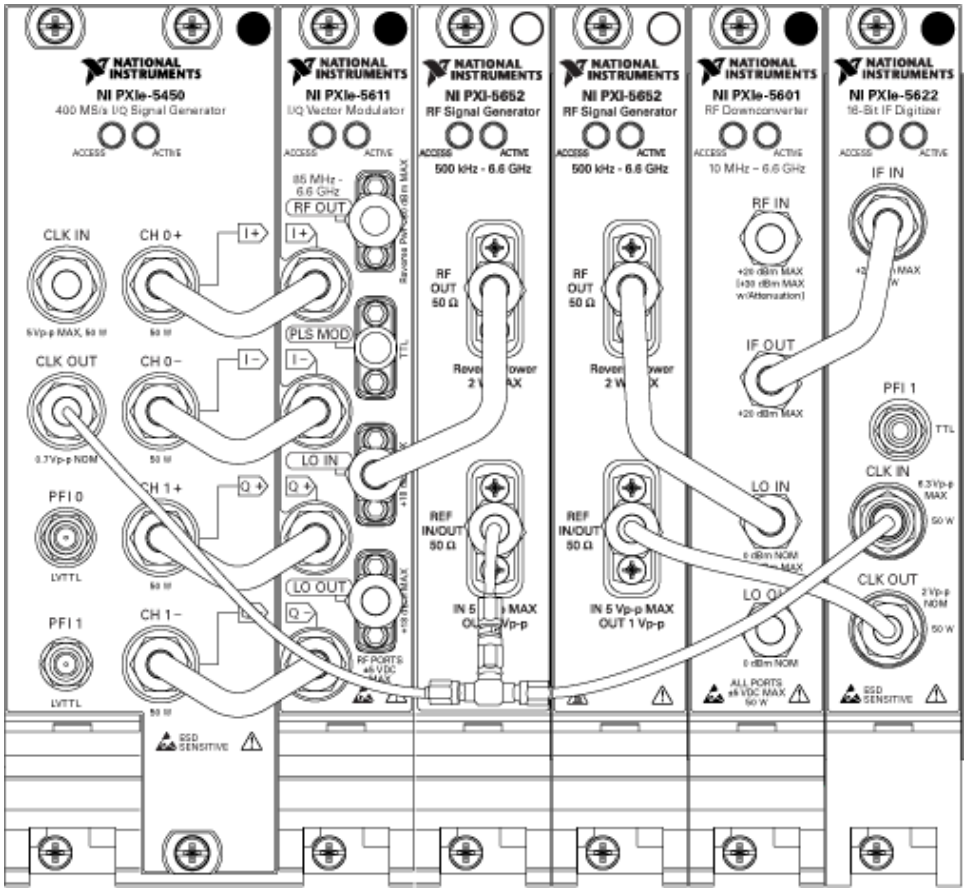
Connecting the PXIe-5673 to the PXIe-5663

You can use the PXIe-5673 Vector Signal Generator with the PXIe-5663 Vector Signal Analyzer to utilize generation and analysis of communications signals from DC to 6.6 GHz. You can configure the PXIe-5673 and PXIe-5663 devices to use either an external or internal Reference Clock.

Note Using an internal clock results in a low phase noise degrading below 1 kHz offset. This impacts communication signals with symbol captures long than 1 ms. For best device performance, NI recommends using an external Reference Clock.

Using an External Reference Clock for the PXIe-5673 and PXIe-5663

The following figure shows a properly interconnected PXIe-5673 and PXIe-5663 device using an external clock.



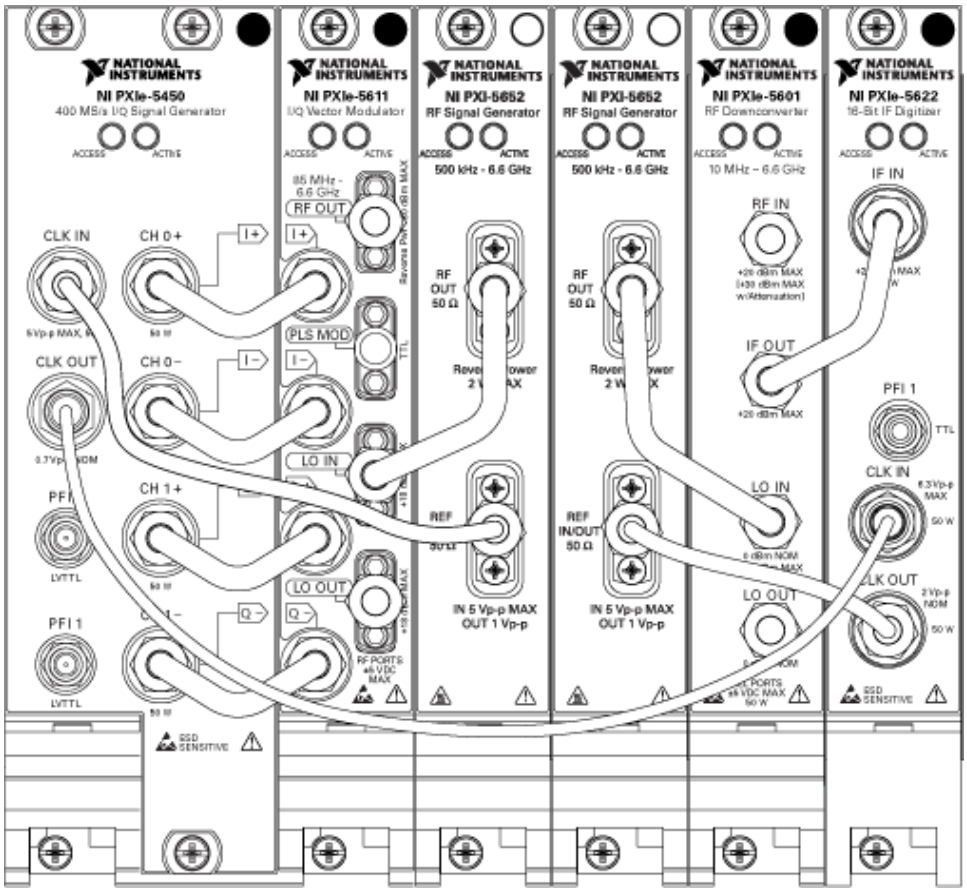
Complete the following steps to connect the PXIe-5673 and PXIe-5663 to use an external clock:

1. Install the PXI-5652 RF Analog Signal Generator that shipped with the PXIe-5663 immediately next to the PXI-5650/5651/5652 device already installed for the PXIe-5673.
2. Install the PXIe-5601 RF Signal Downconverter module that shipped with the PXIe-5663 immediately next to the PXI-5652 device installed in step 1.
3. Install the PXIe-5622 IF Digitizer that shipped with the PXIe-5663 immediately next to the PXIe-5601.
4. Use a flexible cable to connect the external clock of your choice to the CLK IN connector on the PXIe-5450/5451 Waveform Generator.
5. Use Cable C to connect the RF OUT connector on the PXIe-5652 installed in step 2 to the LO IN connector on the PXIe-5601.
6. Use Cable D to connect the IF OUT connector on the PXIe-5601 to the IF IN connector on the PXIe-5622.
7. Use a flexible cable to connect the REF IN/OUT connector on the PXI-5652 installed in step 1 to the CLK OUT connector on the PXIe-5622.

8. Use a flexible cable to connect the CLK OUT connector on the PXIe-5450/5451 to an open connector on a three-way splitter[2].
9. Use a flexible cable to connect the REF IN/OUT connector on the PXI-5650/5651/5652 device already installed for the PXIe-5673 to an open connector on a 3-way splitter.
10. Use a flexible cable to connect the CLK In connector on the PXIe-5622 to an open connector on a three-way splitter.
11. Connect a 50 Ω terminator to the LO OUT connector on the PXIe-5611 I/Q Modulator and the LO OUT connector on the PXIe-5601.

Using an Internal Reference Clock for the PXIe-5673 and PXIe-5663

The following figure shows a properly interconnected PXIe-5673 and PXIe-5663 device using an internal clock.



Complete the following steps to connect the PXIe-5673 and PXIe-5663 to use an internal clock:

2. The three-way splitter is not shipped with the PXIe-5663 or the PXIe-5673.

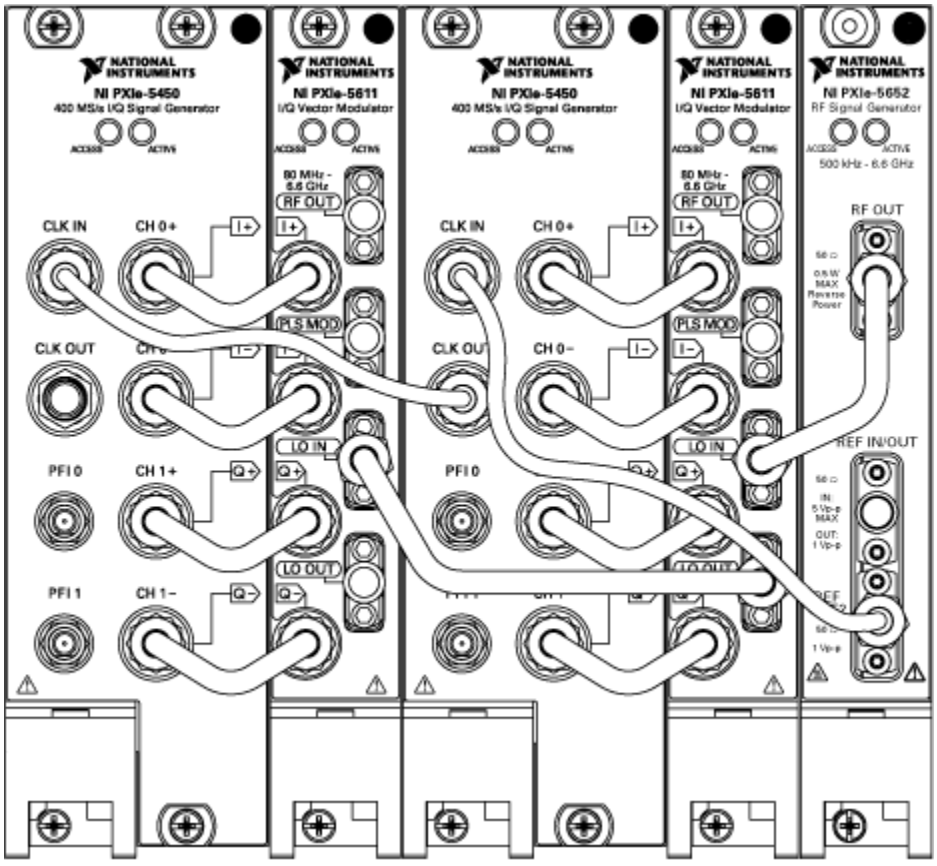
1. Use a flexible cable to connect the CLK IN connector on the PXIe-5450/5451 to the REF IN/OUT connector on the PXI-5650/5651/5652.
2. Install the PXI-5652 device that shipped with the PXIe-5663 immediately next to the PXI-5650/5651/5652 device already installed for the PXIe-5673.
3. Install the PXIe-5601 device that shipped with the PXIe-5663 immediately next to the PXI-5650/5651/5652 device installed in step 1.
4. Install the PXIe-5622 device that shipped with the PXIe-5663 immediately next to the PXIe-5601.
5. Use Cable C to connect the RF OUT connector on the PXI-5650/5651/5652 installed in step 2 to the LO IN connector on the PXIe-5601.
6. Use Cable D to connect the IF OUT connector on the PXIe-5601 to the IF IN connector on the PXIe-5622.
7. Use a flexible cable to connect the REF IN/OUT connector on the PXI-5650/5651/5652 installed in step 2 to the CLK OUT connector on the PXIe-5622.
8. Use a flexible cable to connect the CLK OUT connector on the PXIe-5450/5451 to the CLK IN connector on the PXIe-5622.
9. Connect a 50 Ω terminator to the LO OUT connector on the PXIe-5611 and the LO OUT connector on the PXIe-5601.

Advanced PXIe-5673E Configuration

Interconnecting Multiple PXIe-5673E Modules

The NI PXIe-5673E Getting Started Guide explains how to set up one PXIe-5673E Vector Signal Generator. NI-RFSG supports connecting multiple PXIe-5673E devices such as two PXIe-5611 I/Q Modulators and two PXIe-5450/5451 Waveform Generators, as shown in the following figure.

Note You must install one PXIe-5673E before installing multiple modules. Refer to ***PXIe-5673E Getting Started*** for more information about installing one PXIe-5673E.



Complete the following steps to interconnect multiple PXIe-5673E modules:

1. Install an additional PXIe-5611 immediately to the left of thepreviously installed PXIe-5450/5451.
2. Install an additional PXIe-5450/5451 immediately to the left of the PXIe-5611 installed in step 1.
3. Use Cable A to connect the CH 1-/Q- connector on the PXIe-5450/5451 installed in step 2 to the Q- connector on the PXIe-5611 installed in step 1.
4. Use Cable A to connect the CH 1+/Q+ connector on the PXIe-5450/5451 installed in step 2 to the Q+ connector on the PXIe-5611 installed in step 1.
5. Use Cable A to connect the CH 0-/I- connector on the PXIe-5450/5451 installed in step 2 to the I- connector on the PXIe-5611 installed in step 1.
6. Use Cable A to connect the CH 0+/I+ connector on the PXIe-5450/5451 installed in step 2 to the I+ connector on the PXIe-5611 installed in step 1.
7. Use a flexible cable to connect the CLK OUT connector on the first PXIe-5450/5451 to the CLK IN connector on the PXIe-5450/5451 installed in step 2.
8. Use Cable G to connect the LO OUT connector on the first PXIe-5611 to the LO IN connector on the PXIe-5611 installed in step 1.
9. Connect the 50 Ω terminator to the LO OUT connector on the PXIe-5611 installed in step 1.

After interconnecting multiple PXIe-5673E modules, configure the additional PXIe-5673E to use an External LO. Configure the PXIe-5673E that has an LO to export its Reference Clock by setting the Reference Clock Export Output Terminal property to **ClkOut** or the `NIRFSG_ATTR_EXPORTED_REF_CLOCK_OUTPUT_TERMINAL` attribute to `NIRFSG_VAL_CLK_OUT_STR`.

Related concepts:

- External LO

Related information:

- PXIe-5673E Getting Started

Timing Configurations for PXIe-5673E Modules

The timebases of the AWG module and the RF analog signal generator modules must be frequency-locked to a common 10 MHz Reference Clock. The following clock

sources are available:

- Internal Reference Clock
- External Reference Clock
- PXI Express 10 MHz Backplane Clock

Note The following timing configurations are for PXIe-5673E hardware modules that include the PXIe-5650/5651/5652 with three front panel connectors.

Configuring Internal Reference Clock Timing

The default configuration of the PXIe-5673E is for the PXIe-5650/5651/5652 to export its internal Reference Clock to the PXIe-5450/5451 so that the PXIe-5450/5451 and the PXIe-5650/5651/5652 devices are frequency-locked.

To configure the PXIe-5673E to use the internal clock, set the Reference Clock Source property to **OnBoardClock** or the `NIRFSG_ATTR_REF_CLOCK_SOURCE` attribute to `NIRFSG_VAL_ONBOARD_CLOCK_STR`.

Configuring External Reference Clock Timing

You can also configure the PXIe-5673E to lock to an external reference source.

To configure the PXIe-5673E to use an external Reference Clock, set the Reference Clock Source property to **ClkIn** or the `NIRFSG_ATTR_REF_CLOCK_SOURCE` attribute to `NIRFSG_VAL_CLK_IN_STR`.

The phase noise of the system is also affected by external phase locking. Although the RF signal generator tries to minimize the effect of noisy references by using a very small phase-locked loop bandwidth, a considerable remnant may exist if the reference phase noise is 20 dB to 30 dB worse than the upconverter module onboard OCXO. Some rubidium sources on the market have more phase noise than the upconverter module onboard reference but exhibit high long-term stability.

The external reference signal power level must be greater than –10 dBm or 0.2 $V_{pk\text{-}pk}$ into 50 Ω.

Configuring PXI Express 10 MHz Backplane Clock Timing

You can also configure the PXIe-5673E to lock to the PXI Express 10 MHz backplane clock.

Locking to the PXI Express 10 MHz reference does not provide the same frequency and phase noise performance as the PXIe-5650/5651/5652 internal Reference Clock.

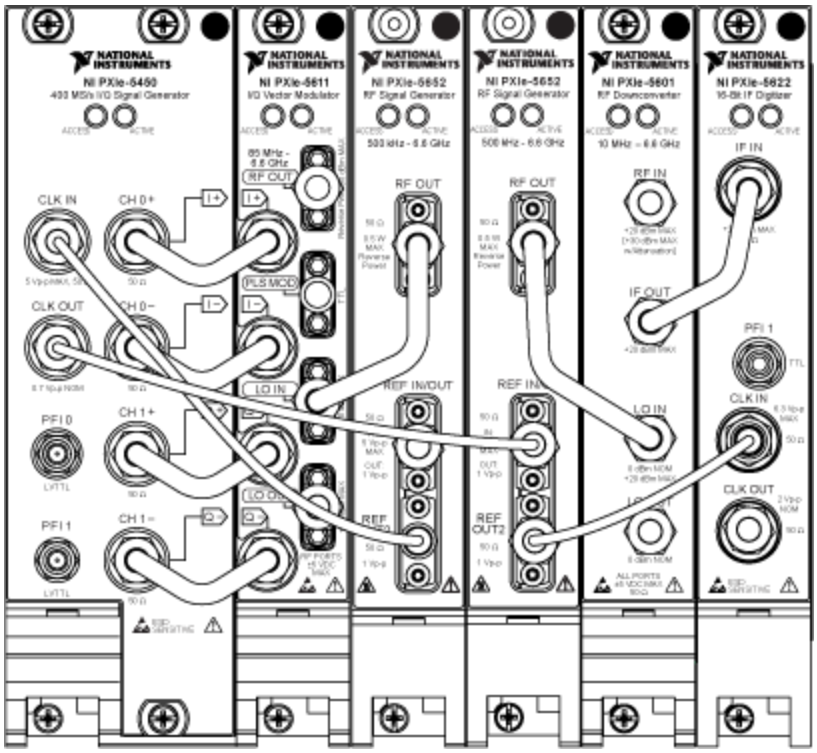
To configure the PXIe-5673E to use the PXI Express 10 MHz backplane clock, set the Reference Clock Source property to **PXI_CLK** or the `NIRFSG_ATTR_REF_CLOCK_SOURCE` attribute to `NIRFSG_VAL_PXI_CLK_STR`.

Connecting the PXIe-5673E to the PXIe-5663E

You can use the PXIe-5673E Vector Signal Generator with the PXIe-5663E Vector Signal Analyzer to utilize generation and analysis of communications signals from DC to 6.6 GHz. You can configure the PXIe-5673E and PXIe-5663E devices to use either an external or internal Reference Clock.

Note Using an internal clock results in a low phase noise degrading below 1 kHz offset. This impacts communication signals with symbol captures longer than 1 ms. For best device performance, NI recommends using an external Reference Clock.

Complete the following steps to use an internal or external clock with the PXIe-5673E and PXIe-5663E. The connections are identical, with the exception of step 8, which is not needed if you are using an internal clock.



Complete the following steps to connect the PXIe-5673E and PXIe-5663E to use an external clock:

1. Install the PXIe-5652 device that shipped with your PXIe-5663E immediately next to the PXIe-5650/5651/5652 device already installed for the PXIe-5673E.
2. Install the PXIe-5601 device that shipped with your PXIe-5663E immediately next to the PXIe-5652 device installed in step 1.
3. Install the PXIe-5622 device that shipped with your PXIe-5663E immediately next to the PXIe-5601.
4. Use Cable C to connect the RF OUT connector on the PXIe-5652 installed in step 1 to the LO IN connector on the PXIe-5601.
5. Use Cable D to connect the IF OUT connector on the PXIe-5601 to the IF IN connector on the PXIe-5622.
6. Use Cable D to connect the REF OUT2 connector on the PXIe-5652 installed in step 1 to the CLK IN connector on the PXIe-5622.
7. Use a flexible cable to connect the REF IN/OUT connector on the PXIe-5652 installed in step 1 to the CLK OUT connector on the PXIe-5450/5451.
8. **External clock users:** Using a flexible coaxial cable, connect the external clock of your choice to the REF IN/OUT connector on the PXIe-5650/5651/5652 already installed with your PXIe-5673E.
9. Connect a 50 Ω terminator to the LO OUT connector on the PXIe-5611 and the LO

OUT connector on the PXIe-5601.

Configuring an External Reference Clock

After interconnecting the PXIe-5673E and PXIe-5663E devices, complete the following steps to allow both devices to share an external Reference Clock source.

1. When programming the PXIe-5673E, set the **output terminal** parameter of the niRFSG Export Signal VI to **CLK OUT** or set the **outputTerminal** parameter of the `niRFSG_ExportSignal` function to `NIRFSG_VAL_CLK_OUT_STR`.
2. When programming the PXIe-5663E, set the **clock source** parameter of the niRFSA Configure Ref Clock VI to **RefIn** or set the **clockSource** parameter of the `niRFSA_ConfigureRefClock` function to NIRFSA_VAL_REF_IN_STR.

External LO

External LO refers to an LO source used with the PXIe-5673/5673E Vector Signal Generator that is not the PXI/PXIe-5650/5651/5652 RF Analog Signal Generator.

By default, a single NI-RFSG session controls all devices in the PXIe-5673/5673E—the PXIe-5611 I/Q Modulator, the PXIe-5450/5451 Waveform Generator, and the PXI/PXIe-5650/5651/5652 LO source. In a PXIe-5673/5673E device configured to use an external LO, the NI-RFSG session controls the I/Q modulator and the AWG, but the LO source is not controlled by the NI-RFSG session. An external LO is useful if you have an LO with lower phase noise, lower harmonics, or faster tuning time than the PXI/PXIe-5650/5651/5652.

Configuring the PXIe-5673/5673E to Use an External LO

After interconnecting multiple PXIe-5673/5673E modules, you can configure the PXIe-5673/5673E to use an external LO in MAX by completing the following steps:

1. Launch MAX by navigating to **Start**»**All Programs**»**NationalInstruments**»**NI MAX** or by clicking the NI MAXdesktop icon.
2. In the configuration tree, double-click **Devices and Interfaces** to seethe list of installed devices.
3. Expand your chassis tree item. You will see a list of installeddevices that includes the PXIe-5611 module, the PXIe-5450/5451 module, and thePXI/PXIe-5650/5651/5652 module.
4. Select the PXIe-PXIe-5611.
5. In the Associated Devices section, use the drop-down LO listbox and select **External**.

You can also configure the PXIe-5673/5673E to use an external LO through the option string input of the niRFSG Initialize With Options VI or `niRFSG_InitWithOptions` function.

Controlling the PXIe-5673/5673E with an External LO

Complete the following steps to control the PXIe-5673/5673E with an external LO by setting the appropriate frequency and power level:

1. Specify the LO frequency to the NI-RFSG session using the Frequency property or `NIRFSG_ATTR_FREQUENCY` attribute.
2. Specify the LO power using the LO In Power property or `NIRFSG_ATTR_LO_IN_POWER` attribute.

Shared LO

Shared LO is a special case of external LO where one PXI/PXIe-5650/5651/5652 RF Analog Signal Generator drives multiple PXIe-5673/5673E daisy-chained modules such as two I/Q modulators and two AWG modules. Sharing an LO signal allows the RF signals to be phase coherent, as phase coherency is important in beamforming applications.

Note RF list mode is not supported when sharing an LO signal.

Configuring the PXIe-5673/5673E to Use a Shared LO

After interconnecting multiple PXIe-5673/5673E modules, you can configure the PXIe-5673/5673E to use a shared LO in MAX by completing the following steps:

1. Launch MAX by navigating to **Start»All Programs»NationalInstruments»NI MAX** or by clicking the NI MAX desktop icon.
2. In the configuration tree, double-click **Devices and Interfaces** to see the list of installed devices.
3. Expand your chassis tree item. You will see a list of installed devices that includes the PXIe-5611 module, the PXIe-5450/5451 module, and thePXI/PXIe-5650/5651/5652 module.
4. In the Associated Devices section, use the drop-down LO listbox to specify the PXI/PXIe-5650/5651/5652 module that is connected to the PXIe-5611 by front panel coaxial cables.
5. For all subsequent PXIe-5611 daisy-chained devices, in the Associated Devices

section,use the drop-down LO listbox and select **External**.

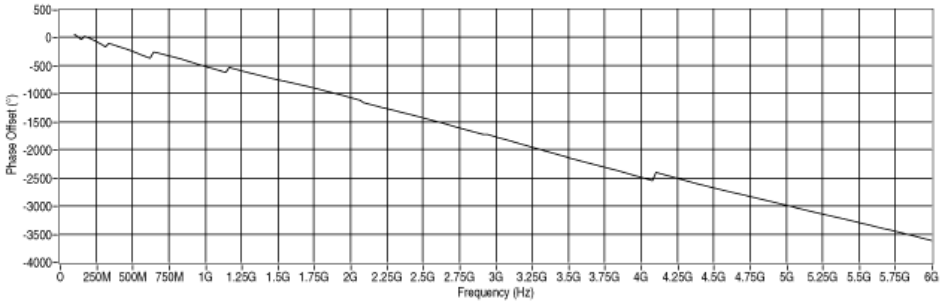
Phase Synchronization and Phase Coherency

Sharing an LO has implications on the PXIe-5673/5673E Vector Signal Generator phase synchronization and phase coherency.

Phase synchronization, or phase lock, guarantees that two or more devices are locked at the same frequency and phase. Phase coherency, or frequency lock, guarantees that two devices are locked to the same frequency with a constant phase offset between them. Phase offset is the difference between the phases of two or more signals.

You can achieve phase coherency on the PXIe-5673/5673E by using a shared LO. Phase coherency is guaranteed because a single LO is shared between each PXIe-5673/5673E module in the daisy chain.

The following plot shows the relationship between the LO IN phase to LO OUT phase when two PXIe-5673/5673E devices are daisy-chained, and the minimum power level is measured to find out where the devices were 180° out-of-phase from each other.



Configuring Phase Synchronization

You can achieve phase synchronization between daisy-chained PXIe-5673/5673E modules by applying a phase offset using the Phase Offset property or `NIRFSG_ATTR_PHASE_OFFSET` attribute. Phase offset between the subsequent devices has to be measured.

Note Use this property or attribute only on the subsequent devices in the daisy-chain.

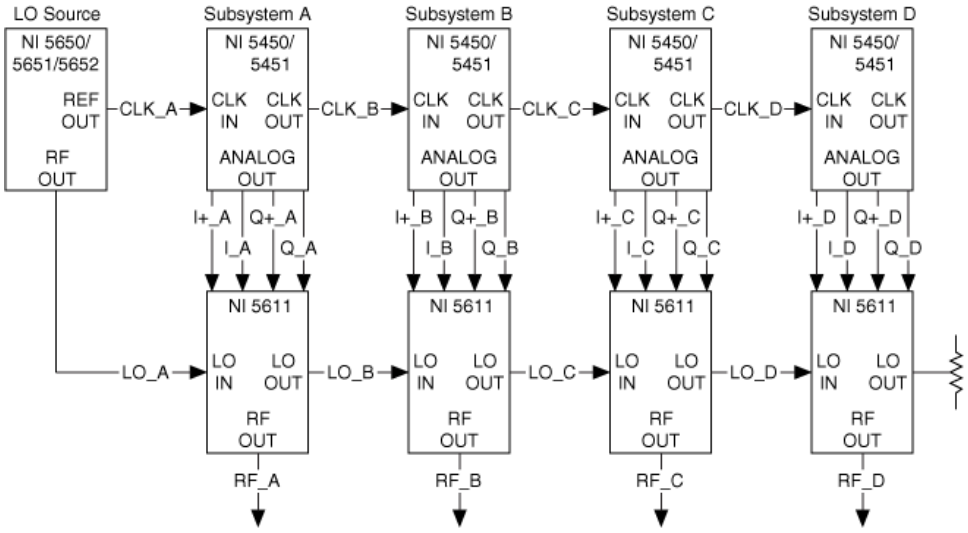
MIMO Systems

Multiple-input, multiple-output (MIMO) systems, such as when you share an LO, improve the overall bit error rate in the presence of multipath performance and increase throughput, but there are some implications on dynamic range.

When sharing an LO, the broadband noise of the LO signal increases slightly as it passes through each PXIe-5611 I/Q Modulator. An increase in noise results in a minimally degraded noise floor for each subsequent subsystem in the daisy chain.

The LO power level variation also increases as it passes through each PXIe-5611 module. An increase in LO power variation results in a slightly wider variation of carrier and image suppression for each subsequent subsystem in the daisy chain.

The following diagram shows the path of a shared LO signal through a MIMO system.



RF Power Level Adjustment

The PXIe-5673/5673E Vector Signal Generator RF output signal power level results from a combination of gain settings in the PXIe-5611 I/Q Modulator and output power level adjustments in the PXIe-5450/5451 Waveform Generator. Step changes in RF output signal power are achieved through attenuator settings in the coarse RF power conditioning section of the PXIe-5611. Vernier adjustments within those steps are realized by variation of onboard signal processing coefficients in the PXIe-5450/5451. NI-RFSG transparently adjusts all hardware modules to achieve the requested RF output power level. Hardware settings are selected by NI-RFSG to optimize linearity and noise floor performance. Refer to your device specifications document for guaranteed output power ranges.

Note The PXIe-5673/5673E allows you to request the maximum output power beyond the specified range. The amplifiers are compressed, and linearity and accuracy are compromised when the maximum possible output power is requested.

Adjustment Components

The PXIe-5611 I/Q Modulator adjusts the vector signal generator output signal power level using up to 124 dB of onboard RF attenuation. Absolute maximum power is a function of frequency and is unit-dependant.

The AWG module provides fine signal power adjustment by scaling the digital waveform. NI-RFSG automatically selects the scaling factor based on signal power requirements. NI-RFSG modifies the digital waveform such that it does not occupy the full-scale output voltage of the DAC. At the lowest requested power levels, the PXIe-5611 uses all of its available attenuation, and the remaining power is removed from the AWG module. Scaling the digital waveform in this manner potentially decreases the dynamic range and thus the signal-to-noise ratio. NI-RFSG performs scaling on both sine waves and arbitrary waveforms as required.

If the frequency output is varied while keeping power output levels constant, NI-RFSG

may automatically adjust the attenuator settings and the AWG power levels to maintain constant power output.

Attenuator Hold

The attenuator hold feature allows you to adjust the output level without switching the internal attenuators on the RF vector signal generator. To achieve this, NI-RFSG sets the PXI-5610 RF Signal Upconverter and PXIe-5611 I/Q Modulator to the attenuation corresponding to the highest desired power level in a sweep (refer to the Power Sweep example) and then adjusts output signal amplitude by scaling the digital waveform such that the digital waveform does not use the full scale of the DAC. Scaling the digital waveform potentially decreases the dynamic range and thus the signal-to-noise ratio.

Use attenuator hold when you need to keep the power monotonically changing while preserving the same power error at the specified frequency setting.

Configuring Attenuator Hold

1. Open a session to the instrument.
2. Configure the Attenuator Hold Max Power property or the `NIRFSG_ATTR_ATTENUATOR_HOLD_MAX_POWER` attribute. This setting specifies the highest power level on your sweep.
3. Specify the power level of the output signal (P).
4. Enable attenuator hold mode using the Attenuator Hold Enabled property or the `NIRFSG_ATTR_ATTENUATOR_HOLD_ENABLED` attribute. The attenuators are set at the Committed stage.
5. Initiate signal generation.

Note Generation starts at the specified power level P, but the attenuators are set in such a way that the requested maximum power can be achieved by incrementing the digital waveform.

Understanding PXIe-5673/5673E Specifications and Performance

This section contains information for the user who wants to optimize performance of the PXIe-5673/5673E Vector Signal Generator by better understanding the common specification characteristics of the device. Refer to the specifications document specific to your device for detailed device specifications.

Spurious Performance

In addition to the desired signal, the PXIe-5611 I/Q Modulator RF OUT front panel connector also contains signal-related spurs. This topic briefly describes the sources of the most common spurs and how to reduce their magnitude or effect when possible. Spurious performance is divided into two categories, depending on where the spurs are generated. The first category is RF-related and includes harmonics, subharmonics, intermodulation distortion (IMD), carrier suppression, and RF image. The second category is baseband-related and includes baseband feedthrough and baseband negative third harmonic.

RF-Related Spurious Performance

Harmonics

The PXIe-5673/5673E Vector Signal Generator filters the modulated and upconverted signal before passing it to the PXIe-5611 RF OUT front panel connector. This filtering process reduces the harmonic content of the RF OUT output, but some harmonics still appear at the output. The second and third harmonics are the most prominent. If the harmonic levels as described in the device specifications are higher than what your application allows, consider external filtering, and confirm that the external filter is designed for a 50 Ω environment.

Subharmonics

The PXI/PXIe-5650/5651/5652 RF Analog Signal Generator is used as the LO source for the PXIe-5673/5673E. The PXI/PXIe-5650/5651/5652 RF OUT front panel connector contains subharmonics when the generated frequency is greater than 3.3 GHz. The PXIe-5611 filters its LO signal before using it. Filtering significantly improves the subharmonic performance of the PXIe-5673/5673E, but because the filters are non-ideal, some subharmonic content is still expected at the PXI/PXIe-5650/5651/5652 RF OUT front panel connector for carriers over 3.3 GHz. External filtering can be useful in further lowering the subharmonic content in demanding applications. Make sure that the external filter is designed for a 50 Ω environment.

IMD

IMD products are due to nonlinearities, and IMD products appear when more than one tone is generated. Intermixing occurs among the generated tones to produce spurs. The most prevalent type of IMD seen at the output of the PXIe-5673/5673E is the third order IMD (IMD3). For example, in the case of two tones generating at frequencies f_1 and f_2, the IMD3 products are spurs at frequencies $2f_1 - f_2$ or $2f_2 - f_1$.

The adjacent channel power ratio (ACPR) performance is largely dependent on the IMD performance, but ACPR and IMD are not equal.The PXIe-5673/5673E sets the IMD performance at relatively higher output levels such around 0 dBm or greater. At lower power levels such as –30 dBm or lower, the IMD performance of the PXIe-5673/5673E is dominated by the onboard modulators. Reducing the power level on the onboard modulators (the baseband power) can also reduce the IMD products appearing at the PXIe-5611 RF OUT front panel connector.

Reducing IMD Products

You can reduce IMD products for relatively low output power levels by completing the following steps:

1. Set the Power Level Type property to **Peak Power** or the `NIRFSG_ATTR_POWER_LEVEL_TYPE` attribute to `NIRFSG_VAL_PEAK_POWER`.
2. Set the Software Scaling Factor property or

NIRFSG_ATTR_ARB_WAVEFORM_SOFTWARE_SCALING_FACTOR attribute to less than 1.

Reducing the baseband power by 1 dB in peak power mode reduces the desired signal power at the PXIe-5611 RF OUT front panel connector by 1 dB and that of the IMD products by 3 dB (for a total of 2 dBc improvement, assuming the output power is low enough so that the modulators dominate the IMD performance of the PXIe-5673/5673E).

Carrier Suppression

The PXIe-5673/5673E achieves very good carrier suppression after impairments are applied. The amount of carrier suppression when generating at low power levels might not stay at the same ratio to the desired signal compared to when generating at high power level.

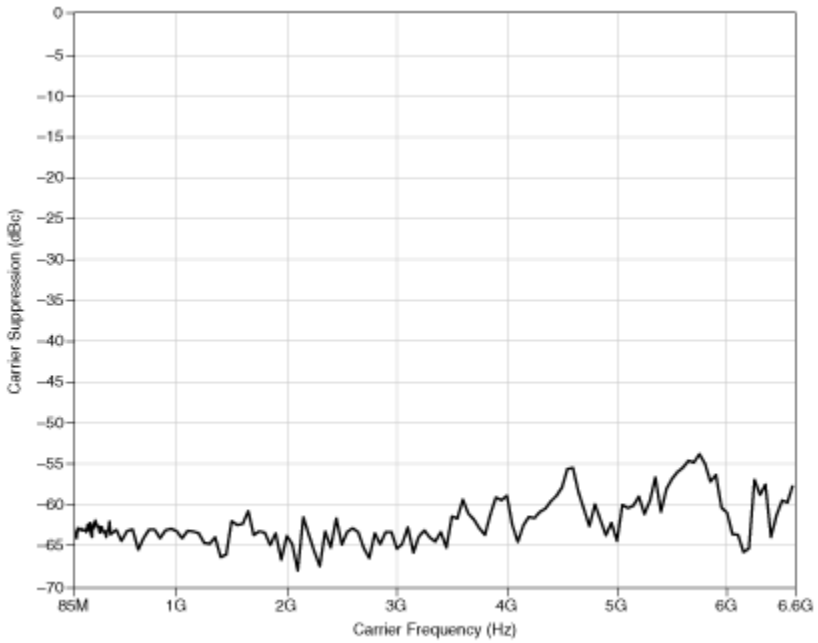
Generating a modulated signal with a relatively high crest factor causes the digital gain on the arbitrary waveform generator to be backed off when the Power Level Type property is set to **Average Power** or the NIRFSG_ATTR_POWER_LEVEL_TYPE attribute is set to NIRFSG_VAL_AVERAGE_POWER. Although the average power appearing at RF OUT lowers when a higher crest factor is being generated compared to when a lower crest factor signal is being generated, the carrier power is the same with lower and higher crest factors. Subsequently, the ratio of the carrier appearing with the higher crest factor signal to the signal itself is higher than that of a signal with a lower crest factor. If the amount of carrier suppression appearing in the output is too low for the application, complete the steps in the Impairment Calibration topic to lower the undesired signal.

A very similar effect to carrier suppression occurs when the Power Level Type property is set to **Peak Power** or the NIRFSG_ATTR_POWER_LEVEL_TYPE attribute is set to NIRFSG_VAL_PEAK_POWER and the Software Scaling Factor property or the NIRFSG_ATTR_ARB_WAVEFORM_SOFTWARE_SCALING_FACTOR attribute is lowered significantly. Software scaling should be used with caution.

The power in the signal is distributed across the signal bandwidth when generating a broadband signal. For example, assuming a similar crest factor as a sine wave, a 0 dBm signal with a bandwidth of 4 MHz plateaus at -66 dBm/Hz as compared to a single sine wave at the same power level appearing at 0 dBm. If the carrier suppression is -50 dBc

as compared to the sine wave, then depending on the resolution bandwidth of the spectrum analyzer analyzing the signal, the carrier may deviate from the signal plateau at the carrier frequency. (-50 dBc is a value used as an example. Refer to your device specifications document for information about expected performance.) In this example, the integrated signal power is still 50 dB higher than the carrier. Perform impairment calibration to achieve better results.

The following plot shows a possible broadband modulated signal with digital gain reduced by 35 dB.



RF Image

RF image occurs mostly due to phase skew and/or gain imbalance in the I and Q paths at baseband frequency. RF image degrades over baseband frequency. Manually calibrating the PXIe-5673/5673E in addition to calibration performed at NI can reduce RF image.

Baseband-Related Spurious Performance

Baseband Feedthrough

The baseband signal applied at the I+, I–, Q+, and Q– PXIe-5611 front panel leaks in to the PXIe-5611 RF OUT front panel connector depending on the frequency and the

carrier frequency. For example, a single-sideband +10 MHz signal generated at a carrier of 1 GHz produces a desired signal at the RF OUT connector at 1,010 MHz. A baseband feedthrough signal also appears at the RF OUT connector at 10 MHz. The following table summarizes the typically expected value of this feedthrough relative to the desired signal in dBc for different carrier frequencies (f_C) and baseband frequencies.

Baseband Frequency (MHz)	f_C < 250 MHz	250 ≤ f_C < 1200 MHz	1200 ≤ f_C < 2500 MHz	f_C ≥ 2500 MHz
1	< –75 dBc	< –75 dBc	< –75 dBc	< –75 dBc
10	–52 dBc	–58 dBc	–68 dBc	< –75 dBc
20	–44 dBc	–50 dBc	–52 dBc	< –75 dBc
30	–40 dBc	–46 dBc	–48 dBc	< –75 dBc
40	–38 dBc	–44 dBc	–44 dBc	< –75 dBc
50	–36 dBc	–42 dBc	–40 dBc	< –75 dBc

Baseband Negative Third Harmonic

Before being upconverted in frequency to the carrier frequency, the baseband signal undergoes a cubic order distortion that is also 180° off-relative to the baseband. A 180° phase-shift in the baseband third harmonic makes the baseband third harmonic appear at a negative frequency relative to the baseband signal at the RF frequency. For example, if you are generating a single-sideband continuous waveform at 1 MHz, write the following equation to the I and Q channels:

$$I\ Channel = a\ \cos(2\pi \cdot 1\ MHz \cdot t)$$

$$Q\ Channel = \sin(2\pi \cdot 1\ MHz \cdot t)$$

where t represents time

If the carrier is at 1.000 GHz, then the desired signal is at 1.001 GHz, and the baseband negative third harmonic is at 0.997 GHz.

Reducing the Spur Level

You can reduce the level of the spur by completing the following steps:

1. Set the Power Level Type property to **Peak Power** or the `NIRFSG_ATTR_POWER_LEVEL_TYPE` attribute to `NIRFSG_VAL_PEAK_POWER`.
2. Set the Software Scaling Factor property or `NIRFSG_ATTR_ARB_WAVEFORM_SOFTWARE_SCALING_FACTOR` attribute to less than 1.

Reducing the baseband power by 1 dB in the peak power mode reduces the desired signal power at the PXIe-5611 RF OUT front panel connector by 1 dB and that of the baseband negative third harmonic by 3 dB for a total of 2 dBc improvement.

Effects of Non-Ideal Reflection Coefficients on Delivered Power

The PXIe-5611 I/Q Modulator front panel connectors are designed to work in a 50 Ω environment. However, the connector impedances are not ideal because they are not exactly equal to 50 Ω. Deviation from ideal impedance can be evaluated as the reflection coefficient (Γ). Refer to the specifications document for your device for more information about voltage standing wave ratio (VSWR).

Reflection coefficient can be derived from VSWR with the following formula:

$$Reflection\ Coefficient = \frac{VSWR - 1}{VSWR + 1}$$

During characterization of the PXIe-5611 RF OUT and LO OUT front panel connectors for power accuracy calibration, the measurement device, a power meter, is connected to the RF OUT and LO OUT front panel connectors through an attenuator to improve the measurement device's reflection coefficient. Subsequently, the measurement device will look like an almost ideal (50 Ω) load. The output power level accuracy numbers in the specifications document for your device mention the accuracy under these conditions, while taking into account any deviations of the measurement

device's impedance as seen by the PXIe-5611 RF OUT or LO OUT front panel connectors from an ideal 50 Ω.

When an external load is connected to either the PXIe-5611 RF OUT or LO OUT front panel connector, the accuracy of the power delivered to the external load depends on the external load's LO OUT and RF OUT reflection coefficient(Γ_S can represent either the LO OUT or RF OUT reflection coefficient). Γ_L and Γ_S assume a reference of 50 Ω. The delivered power to the external load is bounded by the following equation:

$$P_{del} = P_{expected} \times \frac{(1 - |\Gamma_L|^2)}{|1 - \Gamma_S\Gamma_L|^2} \times 10^{\frac{\pm accuracy\ specification}{20}}$$

where P_{del} represents the delivered power, in mW

$P_{expected}$ represents the expected power passed out of the front panel connectors, in mW

Γ_L represents the load or device under test connected to the PXIe-5611

Γ_S represents the RF OUT or LO OUT reflection coefficient

accuracy power represents output power level accuracy for the power and temperature range you are returning, in dB, according to your device specifications.

If $P_{expected}$ is given in dBm, then the formula $10^{\frac{P_{expected\ in\ dBm}{10}}}$ converts dBm power into mW power. Γ_L and Γ_S are in non-dB and linear format, where 50 Ω results in $\Gamma = 0$ and $|\Gamma| = 1$ for a short or an open. Use the formula $10Log_{10}(P_{del})$ to convert the delivered power to the load from mW to dBm. The output power level accuracy specification is what your device specifications identifies as the power accuracy for the power and temperature range you are trying to return. Computing the delivered power depends on the sign of the reflection coefficients. Compute the delivered power to the external load twice with the following denominators and account for the different results in your error budget:

$$(1 + |\Gamma_S||\Gamma_L|)^2$$

and

$(1 - |\Gamma_S||\Gamma_L|)^2$

Example

SS

$$P_{del} = P_{expected} \times \frac{(1 - 0.1995^2)}{|(1 - 0.1585) \times 0.1995|^2} \times 10^{\frac{\pm 0.5}{20}}$$

$$P_{del} = P_{expected} \times \frac{(1 - 0.1995^2)}{|(1 + 0.1585) \times 0.1995|^2} \times 10^{\frac{\pm 0.5}{20}}$$

Adding an in-line external attenuator (a pad) at the PXIe-5611 RF OUT and LO OUT front panel connectors improves the reflection coefficient by double the attenuation amount in dB. For example, connecting a 3 dB pad at the PXIe-5611 RF OUT front panel connector reduces the output power by 3 dB (approximately half of the power) and reduces the magnitude of the reflection coefficient by 6 dB (approximately half of the magnitude).

Note In the preceding example, $P'_{expected} \approx \frac{P_{expected}}{2}$ and $|\Gamma'_S| = 0.07943$.

Settling Times

Note This topic applies only to the PXIe-5611 I/Q Modulator, module revision F and later.

When the carrier frequency and/or the output power level changes on the PXIe-5611 RF OUT front panel connector, NI-RFSG checks the amount of gain the PXIe-5611 must provide to meet the desired power level at the set carrier frequency, given a fixed output power from the PXIe-5450/5451 Waveform Generator. This situation applies in the default operation mode. A similar situation occurs when you program NI-RFSG to correct for any possible gain drift due to temperature change.

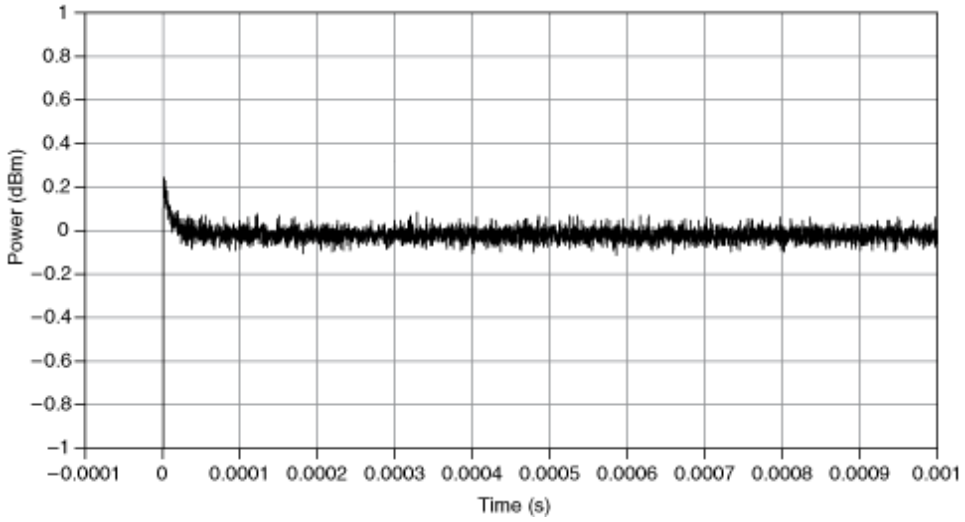
To allow for maximum user flexibility, NI-RFSG does not account for the amount of time required to settle to the final power level. NI-RFSG does not impose wait times at

the expense of power accuracy. However, when power accuracy is critical, deliberate wait periods should be added following any change in the amplitude or frequency of the PXIe-5673/5673E Vector Signal Generator.

Optimal Settling Times

Consider the following device functions for optimal settling times.

First, to maintain a constant output power level at different carrier frequencies or to meet a newly-set power level and the same carrier frequency, the PXIe-5673/5673E switches attenuators in its signal path. The following plot shows a typical residual settling that occurs when an attenuator is engaged to generate 0 dBm.



To avoid waiting for the attenuators to settle, especially when running power sweeps, enable attenuator hold. Enabling attenuator hold sets the gain level of the PXIe-5673 signal path to accommodate the maximum power to be generated and sweeps power by rescaling the digital data. The tradeoff is reduced signal-to-noise ratio.

Enable attenuator hold by setting the Attenuator Hold Enabled property to **TRUE** or the `NIRFSG_ATTR_ATTENUATOR_HOLD_ENABLED` attribute to `VI_TRUE`.

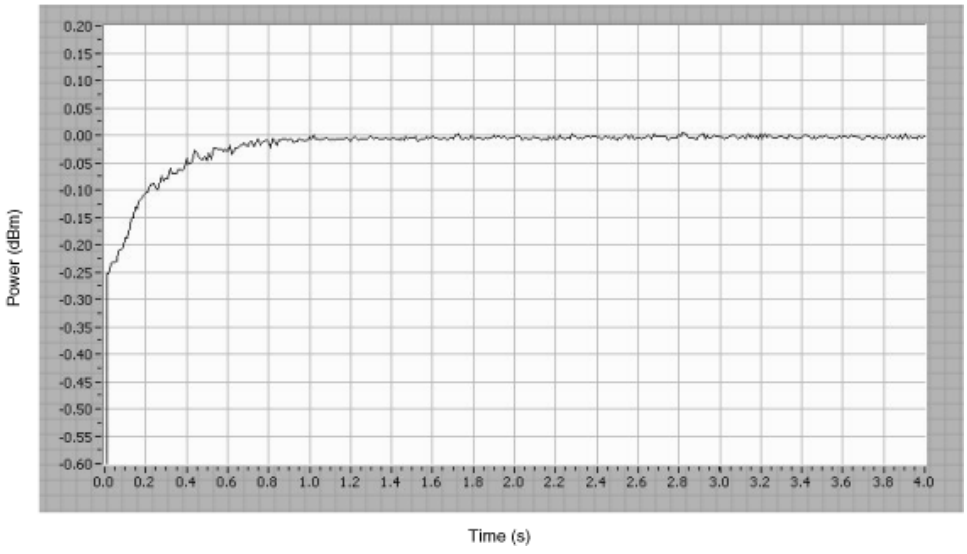
Second, the PXIe-5673/5673E uses several signal paths to cover its frequency range. Each signal path has an RF filter to remove some of the spurs that might affect the spurious performance of the device. The NI-RFSG instrument driver waits 1 ms or less when a path exchange occurs, which allows the output power to settle within approximately 0.5 dBm from its final value. In applications where the frequency is

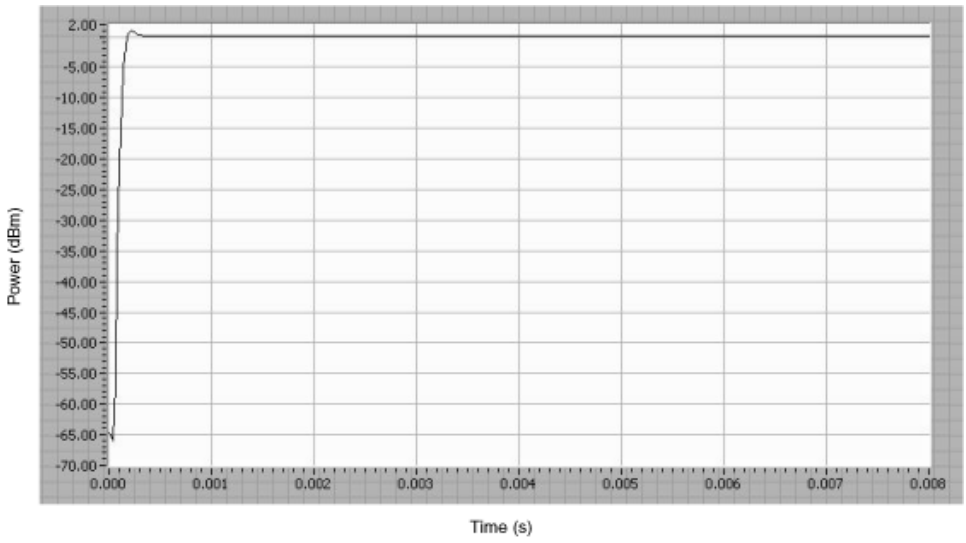
swept and power accuracy is priority, further wait times should be added when the PXIe-5673/5673E carrier frequency encounters an RF filter change.

The appropriate signal path is selected according to the coerced carrier frequency and the selected signal path cannot be overridden. Refer to the specifications document specific to your device for more information about frequency resolution. The following table summarizes the LO signal paths on the PXIe-5673/5673E.

LO Signal Path	Lowest Carrier Frequency (MHz)	Highest Carrier Frequency (MHz)
1	85.0	175.7
2	175.7	250.0
3	250.0	392.2
4	392.0	659.0
5	659.0	1170.7
6	1170.7	2450.0
7	2450.0	3500.0
8	3500.0	6600.0

The following plots demonstrate typical switching between one LO signal path and another. The final desired power level is 0 dBm.





Settling Times for Previous Modules

Note This topic applies only to the PXIe-5611 I/Q Modulator, revision A through E.

When the carrier frequency and/or the output power level changes on the PXIe-5611 RF OUT front panel connector, NI-RFSG checks the amount of gain the PXIe-5611 must provide to meet the desired power level at the set carrier frequency, given a fixed output power from the PXIe-5450 Waveform Generator. This situation applies in the default operation mode. A similar situation occurs when you program NI-RFSG to correct for any possible gain drift due to temperature change.

To allow for maximum user flexibility, NI-RFSG does not account for the amount of time required to settle within 0.5 dBm from the final power level. If speed is more important than power accuracy for your application, NI-RFSG does not impose long wait times. However, when power accuracy is critical, deliberate wait periods should be added following any change in setting the amplitude or frequency of the PXIe-5673 Vector Signal Generator.

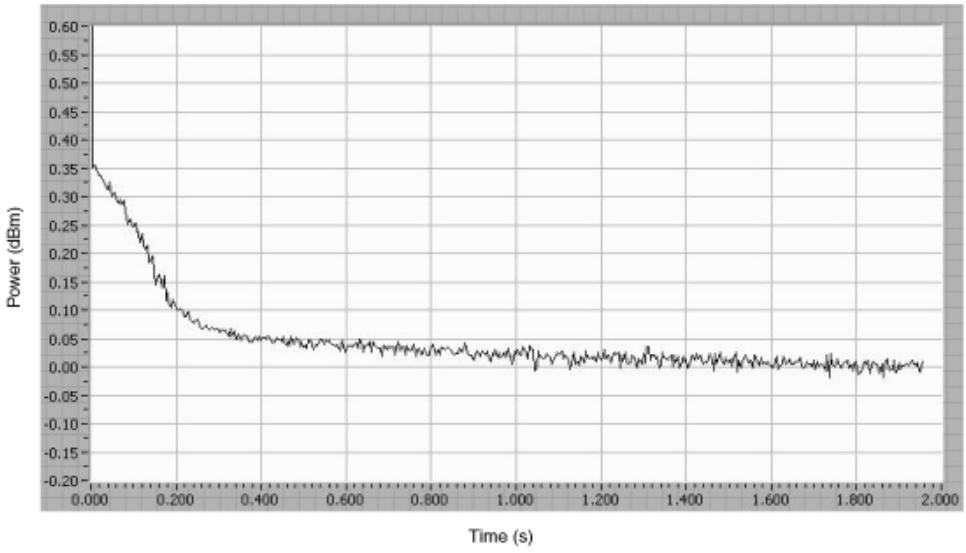
Optimal Settling Times

Consider the following device functions for optimal settling times.

First, to maintain a constant output power level at different carrier frequencies or to

meet a newly-set power level and the same carrier frequency, the PXIe-5673 switches attenuators in its signal path.

The PXIe-5673 uses high-performance gallium arsenide (GaAs) attenuators that allow the device to achieve good performance, but GaAs attenuators require relatively long times to settle. Although it takes 1 ms or less to settle within 0.5 dBm of final output power—for which NI-RFSG accounts—the amount of time it takes for the output power to settle closer to the final value can be in the hundreds of milliseconds range. The following plot shows a typical residual settling that occurs when an attenuator is engaged to generate 0 dBm.



To avoid waiting for the attenuators to settle, especially when running power sweeps, enable attenuator hold. Enabling attenuator hold sets the gain level of the PXIe-5673 signal path to accommodate the maximum power to be generated and sweeps power by rescaling the digital data. The tradeoff is reduced signal-to-noise ratio.

To enable attenuator hold, set the Attenuator Hold Enabled property to **TRUE** or the `NIRFSG_ATTR_ATTENUATOR_HOLD_ENABLED` attribute to `VI_TRUE`.

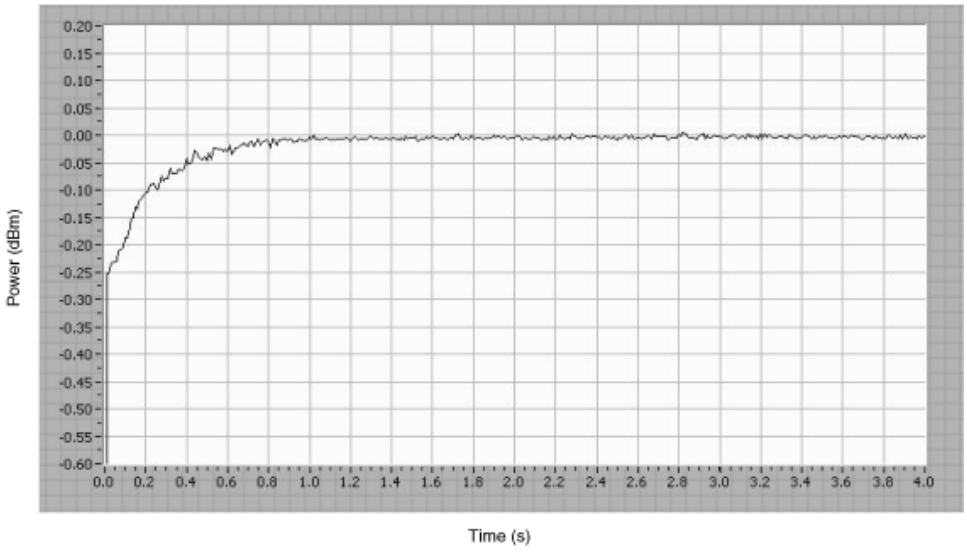
Second, the PXIe-5673 uses several signal paths to cover its frequency range. Each signal path has an RF filter to remove some of the spurs that might affect the spurious performance of the device. Similar to the case with the GaAs attenuators, the NI-RFSG waits 1 ms or less when a path exchange occurs, which allows the output power to settle within approximately 0.5 dBm from its final value. In applications where the frequency is swept and where power accuracy is priority, further wait times should be

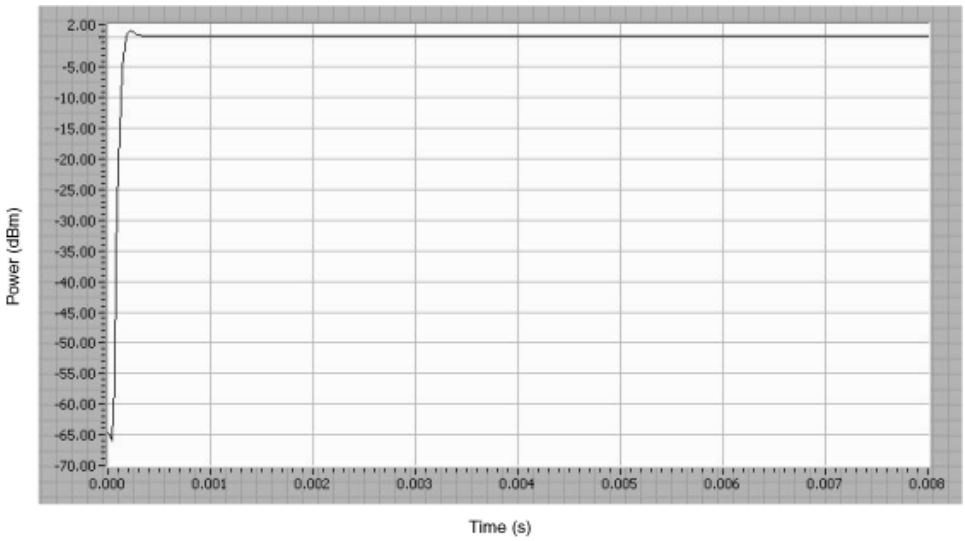
added when the PXIe-5673 carrier frequency encounters an RF filter change.

The appropriate signal path is selected according to the coerced carrier frequency and the selected signal path cannot be overridden. Refer to the specifications document specific to your device for more information about frequency resolution. The following table summarizes the LO signal paths on the PXIe-5673.

LO Signal Path	Lowest Carrier Frequency (MHz)	Highest Carrier Frequency (MHz)
1	85.0	175.7
2	175.7	250.0
3	250.0	392.2
4	392.0	659.0
5	659.0	1170.7
6	1170.7	2450.0
7	2450.0	3500.0
8	3500.0	6600.0

The following plots demonstrate typical switching between one LO signal path and another. The final desired power level is 0 dBm.





Identifying Module Revision

PXIe-5611 specifications and features may vary according to the revision letter of the module.

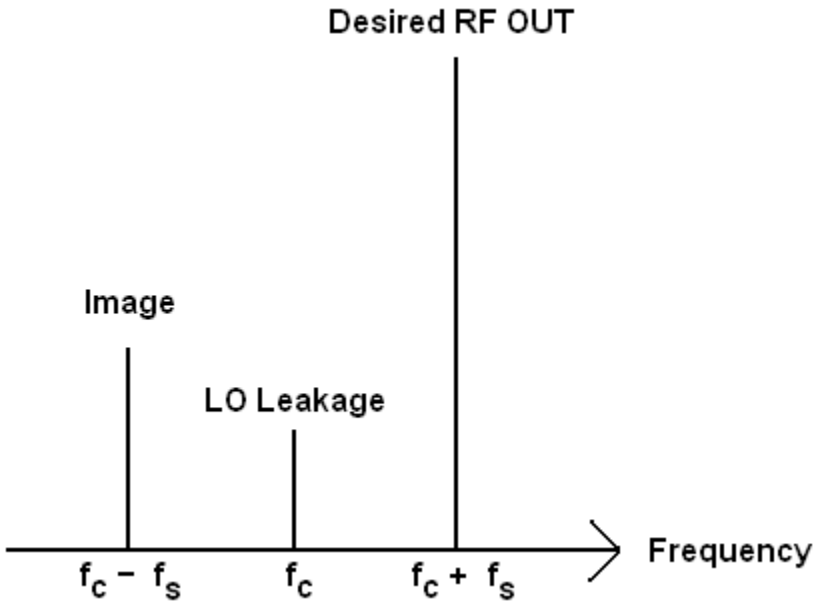
To determine the revision letter of your PXIe-5611, query the Module Revision property or the `NIRFSG_ATTR_MODULE_REVISION` attribute. You can also find the module revision by referring to the module part number, which is printed on your module and consists of six digits and one letter followed by an additional two digits.

Corresponding part numbers and module revision letters are shown in the following table.

PXIe-5611 Part Number	Revision
196385A-01	A
196385B-01	B
196385C-01	C
196385D-01	D
196385E-01	E
196385F-01	F
196385G-01	G

Impairment Calibration

I/Q impairments, such as I offset, Q offset, I/Q gain imbalance and I/Q phase skew, degrade the spurious performance of the I/Q modulator. The offsets contribute to carrier suppression. Gain imbalance and phase skew contribute to the creation of an image for the single-sideband RF signal output that is mirrored across the carrier.For a continuous waveform at a frequency $+f_S$ as the baseband signal generated at a carrier frequency of f_C, the expected LO leakage and the image is shown in the following plot.



The image power relative to the desired RF output (ISR), in dBc, is given by the following formula:

$$ISR \approx 10Log_{10}\left(\frac{\varepsilon^2 + \varphi^2}{4}\right)$$

where ε represents I/Q gain imbalance

ϕ represents I/Q skew in radians

The carrier to desired output (CSR), in dBc, is given by the following formula when the output power is 0 dBm:

$$CSR = 10Log_{10}\left(10(\alpha^2 + \beta^2)\right)$$

where α represents volts offset on the I channel

β represents volts offset on the Q channel

Correcting for Temperature Drift

To correct for temperature drift without having to re-initialize a session, call the niRFSG Perform Thermal Correction VI or the `niRFSG_PerformThermalCorrection` function.

Applying Additional Impairment Correction

You can also apply additional impairment correction with the following properties or attributes:

Property	Attribute
I Offset	`NIRFSG_ATTR_IQ_I_OFFSET`
Q Offset	`NIRFSG_ATTR_IQ_Q_OFFSET`
Gain Imbalance	`NIRFSG_ATTR_IQ_GAIN_IMBALANCE`
IQ Skew (Degrees)	`NIRFSG_ATTR_IQ_SKEW`

Improving Carrier and Image Rejection Performance

Further improvement in carrier and image rejection performance is possible by completing the following steps:

1. Connect the RF OUT front panel connector to an RF vector signal analyzer.
2. Generate a continuous waveform or a multi-tone signal with the PXIe-5673/5673E at a specified carrier frequency.
3. Observe the resulting spectrum and identify the generated signal along with its image and LO leakage.
4. Adjust the impairments using the appropriate properties or attributes to reduce their effects. For example, reduce the LO leakage and the image of the PXIe-5673/

5673E at a 1 GHz carrier frequency by completing the following steps:

a. Generate a single-sideband continuous waveform at 1 MHz.

> **Note** Generate at 1 MHz by writing cos(2π·1 MHz·t) to the I channel and sin(2π·1 MHz·t) to the Q channel, where t represents time.

b. Set the carrier frequency with the niRFSG Configure RF VI or the `niRFSG_ConfigureRF` function to 1 GHz and the output RF power to 0 dBm.
c. Set the RF vector signal analyzer to read the spectrum centered at 1 GHz with a 5 MHz span.
d. Set the reference level appropriately so that the incoming signal does not saturate the device.
e. Set the resolution bandwidth as small as possible while still obtaining updated spectra fast enough so that you can see the effect(s) of changing an impairment.
f. With the RF vector signal analyzer, locate the generated signal at exactly 1.001 GHz (if the device is locked in frequency with the PXIe-5673/5673E), the leaked LO at 1 GHz and the image at 0.999 GHz. Make sure the image and the leaked LO are at least 20 dB or 30 dB above the displayed noise floor. If not, reduce RF vector signal analyzer attenuation and/or resolution bandwidth to obtain such results.
g. Adjust I/Q skew in steps of 0.1 degrees from 0.0 while observing the image level. If setting the skew equal to 0.1 degrees reduces the amplitude of the image, then continue to increase the skew until the image reverses its course and starts increasing. If the image level increases by changing the skew from 0 to 0.1, then change the skew to –0.1, –0.2 and so on. The skew value that yields the minimum image is the value to save and use in the next step.
h. Adjust gain imbalance in steps of 0.001, starting from 1.000. Continue to increase the gain imbalance until the image is at its minimum.
i. For further reduction in image power, adjust I/Q skew in steps of 0.01 degrees until minimum image is achieved. The gain imbalance then can be readjusted with steps of 0.0001. Iterate as needed while reducing the step size by a decade going from one iteration to the next.

Manual offset calibration is performed using the preceding steps. While observing the amount of LO leakage recorded by the RF vector signal analyzer, adjust I offset in steps

of 0.001 V until minimum LO leakage is achieved. Adjust Q offset in similar steps until minimum LO leakage is achieved. If needed, iterate with steps of 0.0001 V and so on.

For example, to achieve -65 dBc image-to-signal and carrier-to-signal levels, the residual (following calibration) I/Q gain imbalance should be less than 0.000795 (or 0.0795%), the I-Q phase skew should be less than 0.000795 radians (or 0.045°), and the residual equivalent offsets should be kept less than 0.125 mV each.

Modulation Bandwidth Performance

The PXIe-5673/5673E Vector Signal Generator achieves good image rejection after applying impairments found during the impairment calibration process. Impairment calibration is performed at an offset of 1 MHz from the carrier. As the modulation bandwidth increases, the image performance degrades.

At ±10 MHz baseband bandwidth, the image at the RF OUT connector of the PXIe-5673/5673E is still within a few dB from its specified performance at ±1 MHz offset. Refer to the device specifications for information about expected performance. The image for a ±60 MHz modulation signal typically degrades to -40 dBc at the edges of the band at room temperature.

Baseband Interpolation

The AWG module implements baseband interpolation in order to reduce the power of aliased images. Interpolation is a process that effectively turns a lower sample rate into a higher sample rate. Because images are not interpolated, they become a part of the rejection band of the filter at the higher sample rate. The images are then moved into the rejection band of the filter. NI-RFSG selects the largest interpolation factor to give the maximum possible DAC sample rate.

Note For optimum performance, National Instruments recommends maintaining the sample rate between 270 MS/s and 400 MS/s due to the characteristics of the image rejection filter.

Interpolation Settings

To determine the total interpolation, divide 400 MS/s by your sample rate and round down to the nearest integer (or the nearest "step," as noted in the Interpolation table for your total interpolation value). Then, consult the following table for settings that will allow you to achieve your desired interpolated sample rate.

Example: At a sample rate of 4.5 MS/s, the total interpolation is determined by the following calculations:

400 MS/s / 4.45 MS/s = 89.88x total interpolation.

A total interpolation rate of 89.88x falls in the 24 to 8,192 range in the following table. As this range is measured in steps of 8, you must round down to the nearest multiple of 8, yielding a total interpolation rate of 88x. This value corresponds to a worst case image at or below -82 dB.

Desired Sample Rate (S/s)	I/Q Bandwidth (Hz)1 Sample/ symbol	Total Interpolation	Interpolated Sample Rate* (MS/s)	Theoretical Worst Case Image Feedthrough (dB),20 MS/s Bandwidth Signal	Theoretical Worst Case Image Feedthrough (dB), Maximum I/Q Bandwidth
12 k—24 k	4.8 k—9.6 k	16,384—32,768 in steps of 32	370—400	N/A	<-100
24 k—48 k	9.6 k—19.2 k	8,192—16,384 in steps of 16	370—400	N/A	<-100
48 k—16.66 M	19.2 k—6.664 M	24—8,192 in steps of 8	310—400	N/A	-100
16.66 M—33.33 M	6.664 M—13.332 M	12—24 in steps of 4	300—400	N/A	-88
33.33 M—50 M	13.332 M—20 M	8	267—400	N/A	-61
50 M—67.5 M	20 M—27 M	4	200—270	-31	-23
67.5 M—100 M	27 M—40 M	4	270—400	-62	-45

Desired Sample Rate (S/s)	I/Q Bandwidth (Hz)1 Sample/ symbol	Total Interpolation	Interpolated Sample Rate* (MS/s)	Theoretical Worst Case Image Feedthrough (dB),20 MS/s Bandwidth Signal	Theoretical Worst Case Image Feedthrough (dB), Maximum I/Q Bandwidth
100 M—135 M	40 M—54 M	2	200—270	-31	-31
135 M—200 M	54 M—80 M	2	270—400	-62	-28
200 M	108 M—160 M	2	400	-82	-28

Assumptions: Internal Sample Clock, High Resolution clock mode. I/Q ranges do not include the first point (for example, 50 M has 8x total interpolation).

* If your interpolated sample rate falls within an undesirable band, you can use the Modulation Toolkit to provide fractional resampling that will adjust the sample rate to achieve better image rejection.

Note With OSP enabled, Sample Rate = Symbol Rate x Samples/Symbol

Compression

Compression describes the higher output power region of an amplifier where the amplifier's gain becomes non-linear. The PXIe-5673/5673E Vector Signal Generator begins to enter its compression region as output power levels increase above 0 dBm. The effects of this compression can be observed as a decreased TOI point and increased intermodulation and harmonic tones. The PXIe-5673/5673E uses multiple amplifiers in stages, and any, all, or none of these stages may be in compression at high output powers. The power levels in these stages are automatically balanced to achieve the optimal response for linearity and noise.

Optimizing for Low Power Generation

When you set the Power Level Type property to **Average Power** or the

NIRFSG_ATTR_POWER_LEVEL_TYPE attribute to NIRFSG_VAL_AVERAGE_POWER, reducing the power level at the RF OUT front panel connector, for example, from 1 dBm to 0 dBm reduces the carrier suppression by 1 dB. Subsequently, the carrier suppression to the desired RF output power ratio is mostly maintained, in dBc. This carrier suppression is mostly due to DC offset appearing at baseband. Other factors cause some of the LO power to leak into the RF OUT front panel connector and dominates the carrier suppression if the output power drops significantly. For example, generating a -90 dBm signal causes a significant level of LO to appear at the RF OUT front panel connector. Refer to the specifications document specific to your device for information about expected performance.

Note If your application requires low power levels and is sensitive to carrier suppression at power levels specified in the device specifications, consider using external attenuators instead of the onboard attenuators. For example, if the level of carrier suppression that appears along with a -90 dBm output is not ideal, generate -60 dBm and connect a 30 dB in-line SMA attenuator. This yields -60 dBm performance in terms of carrier suppression while still delivering -90 dBm.

Hardware Integration and Maintenance

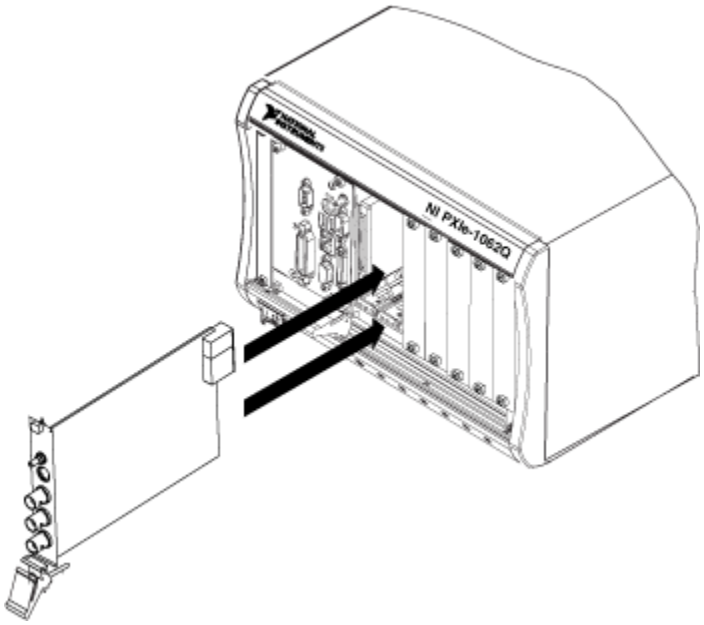
This section contains information about integrating and maintaining NI-RFSG devices into a PXI- or PXI Express-based measurement system.

The PXI architecture has built-in timing and triggering features that can synchronize multiple devices over a backplane timing bus. Multiple devices in a modular instrumentation system can share a common Reference Clock and synchronize to triggers that are distributed over controlled signal paths that ensure matched propagation. Internal routing of these timing signals in PXI eliminate complicated external wiring. Standardized timing protocols eliminate incompatibilities, giving you the best performance when synchronizing any kind of analog, digital, or timing measurements.

PXI Express Modules

The PXI Express Specification integrates PCI Express signaling into the PXI standard, which increases backplane bandwidth and enhances PXI timing and synchronization features by incorporating a 100 MHz differential Reference Clock and differential triggers. The PXI Express Specification adds these features to PXI while maintaining backward compatibility.

Figure 10. PXI Express Module Installation



Chassis Guidelines

You can install NI PXI Express modules in the following PXI Express chassis slots:

- **PXI hybrid slots**—Accepts either PXI modules that are hybrid slot-compatible or PXI Express modules
- **PXI Express slots**—Accepts PXI Express modules
- **PXI Express system timing slots**—Accepts PXI Express modules

Note Refer to the getting started guide for your PXI Express device and chassis documentation for more information about installing and configuring PXI Express modules.

Maintaining PXI Systems

Clean the fan filters on the chassis regularly to prevent fan blockage and ensure efficient air circulation.

Cleaning frequency depends on the amount of use and the operating environment. For specific information about cleaning procedures and other recommended maintenance, refer to the module specifications and the chassis user documentation.

Uninstalling the Hardware

Hot Surface If the module has been in use, it may exceed safe handling temperatures and cause burns. Allow the module to cool before removing it from the chassis.

Notice Disconnect or disable any external RF, clock, or digital connections to the device front panel. Applying external signals while the device is powered off may cause damage.

Complete the following steps to uninstall your hardware.

1. Power off the chassis.
2. Ground yourself with a grounding strap or touch a grounded metal surface.
3. Disconnect any cables from the module front panel connectors.
4. Unlatch the module by pushing down on the ejector handle.
5. Pull the ejector handle and hold the module by the edges to remove it from the chassis.

Store the module in the original antistatic packaging when not in use to avoid damage.