myRIO Device Reference and Procedures

2024-04-26

Contents

myRIO Device Reference and Procedures

Use this book as a reference for information about using myRIO devices with NI CompactRIO Device Drivers in LabVIEW.

Refer to the myRIO Toolkit Help for more detailed information about using the LabVIEW myRIO Toolkit to create applications for myRIO devices.

To view related topics, click the **Locate** button, shown at left, in the toolbar at the top of this window. The **LabVIEW Help** highlights this topic in the **Contents** tab so you can navigate the related topics.

myRIO-1900

Portable Reconfigurable I/O (AI, AO, DIO)

10 AI channels, 6 AO channels, 40 DIO channels, Xilinx Z-7010 FPGA

Software Reference (?)

FPGA Interface

Hardware Documentation (?)

The **NI myRIO-1900 User Guide and Specifications** ship with the LabVIEW myRIO Toolkit.

myRIO-1900 Pin Assignments

Connector A

Show/Hide Pinout

Connector B

Show/Hide Pinout

Connector C

▸ Show/Hide Pinout

Related Topics

Configuring a Project with Connected Hardware
Configuring a Project with Offline Hardware

myRIO-1900 (FPGA Interface)

Portable Reconfigurable I/O (AI, AO, DIO)

10 AI channels, 6 AO channels, 40 DIO channels, Xilinx Z-7010 FPGA

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
Audio**x**	AudioIn/Left, AudioIn/Right, AudioOut/Left, AudioOut/Right
ConnectorA/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector A has AI channels 0 to 3.
ConnectorA/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector A has AO channels 0 to 1.
ConnectorA/DIO**y**	Digital input/output channel **y** on Connector A, where **y** is the number of the channel. Connector A has channels 0 to 15. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorA/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.

ConnectorA/DIO15:8	Digital port consisting of channels 8 to 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
ConnectorB/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector B has AI channels 0 to 3.
ConnectorB/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector B has AO channels 0 to 1.
ConnectorB/DIO**y**	Digital input/output channel **y** on Connector B, where **y** is the number of the channel. Connector B has channels 0 to 15. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorB/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorB/DIO15:8	Digital port consisting of channels 8 to 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
ConnectorC/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector C has AI channels 0 to 1.
ConnectorC/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector C has AO channels 0 to 1.
ConnectorC/DIO**y**	Digital input/output channel **y** on Connector C, where **y** is the number of the channel. Connector C has channels 0 to 7. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
Onboard I/O	AccelerationX, AccelerationY, and AccelerationZ. Use the FPGA I/O Node to access these channels.
Onboard I/O	Button0, LED0, LED1, LED2, and LED3. Use the FPGA I/O Node to access these channels.

Arbitration

You can configure the arbitration settings for the DIO channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node topic for a description of this method.

Module Methods

This device does not support any module methods.

Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop for digital I/O only. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

myRIO-1950

Portable Reconfigurable I/O (AI, AO, DIO)

10 AI channels, 6 AO channels, 40 DIO channels, Xilinx Z-7010 FPGA

Software Reference (?)

FPGA Interface

Hardware Documentation (?)

The **NI myRIO-1950 User Guide and Specifications** ship with the LabVIEW myRIO Toolkit.

myRIO-1950 Pin Assignments

Connector A

Show/Hide Pinout

Connector B

Show/Hide Pinout

Connector C

Show/Hide Pinout

Related Topics

Configuring a Project with Connected Hardware
Configuring a Project with Offline Hardware

myRIO-1950 (FPGA Interface)

Portable Reconfigurable I/O (AI, AO, DIO)

10 AI channels, 6 AO channels, 40 DIO channels, Xilinx Z-7010 FPGA

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description

ConnectorA/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector A has AI channels 0 to 3.
ConnectorA/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector A has AO channels 0 to 1.
ConnectorA/DIO**y**	Digital input/output channel **y** on Connector A, where **y** is the number of the channel. Connector A has channels 0 to 15. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorA/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorA/DIO15:8	Digital port consisting of channels 8 to 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
ConnectorB/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector B has AI channels 0 to 3.
ConnectorB/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector B has AO channels 0 to 1.
ConnectorB/DIO**y**	Digital input/output channel **y** on Connector B, where **y** is the number of the channel. Connector B has channels 0 to 15. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorB/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorB/DIO15:8	Digital port consisting of channels 8 to 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
Onboard I/O	AccelerationX, AccelerationY, and AccelerationZ. Use the FPGA I/O Node to access these channels.
Onboard I/O	Button0, LED0, LED1, LED2, and LED3. Use the FPGA I/O Node to access these channels.

Arbitration

You can configure the arbitration settings for the DIO channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node topic for a description of this method.

Module Methods

This device does not support any module methods.

Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop for digital I/O only. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

NI ELVIS RIO Control Module

Portable Reconfigurable I/O (AI, AO, DIO)

8 AI channels, 4 AO channels, 32 DIO channels, Xilinx Z-7010 FPGA

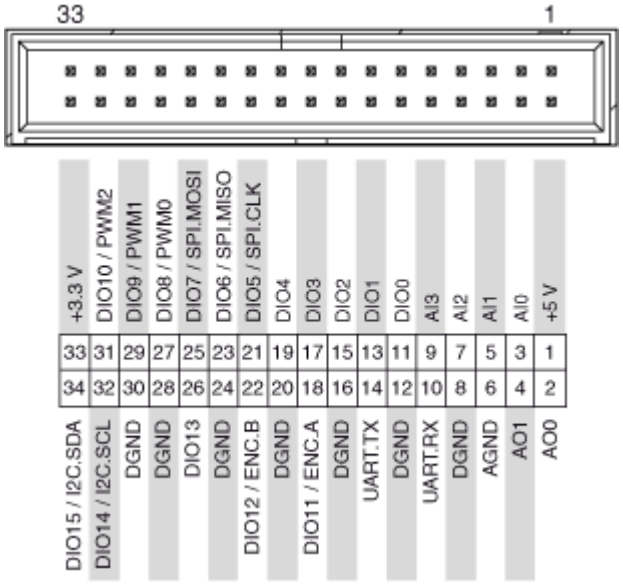
Software Reference (?)

FPGA Interface

Hardware Documentation (?)

NI ELVIS RIO CM hardware documentation on ni.com/manuals

NI ELVIS RIO CM Pin Assignments



Related Topics

Configuring a Project with Connected Hardware
Configuring a Project with Offline Hardware

NI ELVIS RIO Control Module (FPGA Interface)

Portable Reconfigurable I/O (AI, AO, DIO)

8 AI channels, 4 AO channels, 32 DIO channels, Xilinx Z-7010 FPGA

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
ConnectorA/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector A has AI channels 0 to 3.
ConnectorA/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector A has AO channels 0 to 1.
ConnectorA/DIO**y**	Digital input/output channel **y** on Connector A, where **y** is the number of the channel. Connector A has channels 0 to 15. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorA/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorA/DIO15:8	Digital port consisting of channels 0 to 7. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
ConnectorB/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector B has AI channels 0 to 3.
ConnectorB/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector B has AO channels 0 to 1.
ConnectorB/DIO**y**	Digital input/output channel **y** on Connector B, where **y** is the number of the channel. Connector B has channels 0 to 15. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorB/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorB/DIO15:8	Digital port consisting of channels 0 to 7. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
Onboard I/O	Button0, LED0, LED1, LED2, and LED3. Use the FPGA I/O Node to access these channels.

Arbitration

You can configure the arbitration settings for the DIO channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node topic for a description of this method.

Module Methods

This device does not support any module methods.

Properties

This device does not support any properties.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop for digital I/O only. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

NI ELVIS III

Reconfigurable I/O (AI, AO, DIO)

16 AI channels, 4 AO channels, 40 DIO channels, Xilinx Z-7020 FPGA

Software Reference (?)

FPGA Interface

Hardware Documentation (?)

NI ELVIS III 2018 Manual on ni.com

NI ELVIS III Pin Assignments

Supply (+15 V_{out})	1	63	Supply (-15 V_{out})
Supply (+15 V_{out})	2	64	Supply (-15 V_{out})
Supply (+5 V_{out})	3	65	DGND
Supply (+5 V_{out})	4	66	DGND
Supply (+5 V_{out})	5	67	DGND
DGND	6	68	DGND
B/DIO0	7	69	B/DIO1
B/DIO2	8	70	B/DIO3
B/DIO4	9	71	B/DIO5
B/DIO6	10	72	B/DIO7
DGND	11	73	DGND
USB D+	12	74	USB_VBUS
USB D-	13	75	DGND
B/DIO8	14	76	B/DIO9
B/DIO10	15	77	B/DIO11
B/DIO12	16	78	B/DIO13
B/DIO14	17	79	B/DIO15
DGND	18	80	DGND
RSVD	19	81	RSVD
RSVD	20	82	RSVD
RSVD	21	83	RSVD
RSVD	22	84	RSVD
DGND	23	85	DGND
Supply (+3.3 V_{out})	24	86	B/DIO17
B/DIO16	25	87	B/DIO19
B/DIO18	26	88	A/DIO19
A/DIO18	27	89	A/DIO17
A/DIO16	28	90	RSVD
A/DIO14	29	91	A/DIO15
A/DIO12	30	92	A/DIO13
A/DIO10	31	93	A/DIO11
A/DIO8	32	94	A/DIO9
A/DIO6	33	95	A/DIO7
A/DIO4	34	96	A/DIO5
A/DIO2	35	97	A/DIO3
A/DIO0	36	98	A/DIO1
DGND	37	99	DGND
RSVD	38	100	RSVD
AGND	39	101	AGND
B/AI0	40	102	B/AI4
B/AI1	41	103	B/AI5
B/AI2	42	104	B/AI6
B/AI3	43	105	B/AI7
AGND	44	106	AGND
A/AI3	45	107	A/AI7
A/AI2	46	108	A/AI6
A/AI1	47	109	A/AI5
A/AI0	48	110	A/AI4
RSVD	49	111	RSVD
RSVD	52	114	RSVD
RSVD	53	115	RSVD
B/AO0	54	116	RSVD
AGND	55	117	RSVD
RSVD	56	118	AGND
RSVD	57	119	B/AO1
RSVD	58	120	RSVD
AGND	59	121	AGND
A/AO0	60	122	A/AO1
RSVD	61	123	RSVD
RSVD	62	124	RSVD

Related Topics

Configuring a Project with Connected Hardware
Configuring a Project with Offline Hardware

NI ELVIS III (FPGA Interface)

Reconfigurable I/O (AI, AO, DIO)

16 AI channels, 4 AO channels, 40 DIO channels, Xilinx Z-7020 FPGA

FPGA I/O Node

You can use an FPGA I/O Node, configured for reading and writing, with this device.

Use the FPGA I/O Node to access the following terminals for this device.

Terminal	Description
ConnectorA/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector A has AI channels 0 to 7.
ConnectorA/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector A has AO channels 0 to 1.
ConnectorA/DIO**y**	Digital input/output channel **y** on Connector A, where **y** is the number of the channel. Connector A has channels 0 to 19. DIO 16 and DIO 17 are shared with the UART and Console Out application. When the UART or Console Out application is enabled, DIO 16 functions as the UART Rx line, and DIO 17 functions as the UART Tx line. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorA/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorA/DIO15:8	Digital port consisting of channels 8 to 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.

ConnectorB/AI**x**	Analog input channel **x**, where **x** is the number of the channel. Connector B has AI channels 0 to 7.
ConnectorB/AO**x**	Analog output channel **x**, where **x** is the number of the channel. Connector B has AO channels 0 to 1.
ConnectorB/DIO**y**	Digital input/output channel **y** on Connector B, where **y** is the number of the channel. Connector B has channels 0 to 19. DIO 16 and DIO 17 are shared with the UART and Console Out application. When the UART or Console Out application is enabled, DIO 16 functions as the UART Rx line, and DIO 17 functions as the UART Tx line. Use the FPGA I/O Node or the Set Data Output or Set Data Enable method to access this channel.
ConnectorB/DIO7:0	Digital port consisting of channels 0 to 7. Channel 7 is returned in the MSB, and channel 0 is returned in the LSB.
ConnectorB/DIO15:8	Digital port consisting of channels 8 to 15. Channel 15 is returned in the MSB, and channel 8 is returned in the LSB.
Onboard I/O	Button0, LED0, LED1, LED2, LED3, Inst Trig Out and Inst Trig In. Button0 returns the value of the onboard button status. LED0:3 controls the four onboard LEDs. Inst Trig Out sends the trigger signal to the instrumentation board. Inst Trig In receives the trigger signal from the instrumentation board. Use the FPGA I/O Node to access these channels.

Note When the application board is turned off, the digital outputs go into tristate and the analog outputs go to 0 V. When the power is turned on, the digital outputs and the analog outputs go to the value that was last set. For the digital outputs, this happen immediately. For the analog outputs, there is a delay for the values to go from 0 V to the last written value. If an analog output operation is invoked while this is happening, it gets held off and may potentially affect the loop timing.

Arbitration

You can configure the arbitration settings for the DIO channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. The default arbitration setting is Never Arbitrate.

I/O Methods

Use the FPGA I/O Method Node to access the following I/O methods for this device.

Method	Description
Set Output Data	Refer to the FPGA I/O Method Node topic for a description of this method.
Set Output Enable	Refer to the FPGA I/O Method Node topic for a description of this method.

Module Methods

Method	Description
IO Sample	Acquires a single sample from the module. The channel number, terminal mode, and voltage range are all configurable at run time. **Note** Do not configure the VI to run an IO Sample method and an AI IO Node in parallel when both are targeted to the same connector. This will cause incorrect reading from the IO Sample method. The AI IO Node still gives the correct reading, but will not be able to meet the specified data rate. The same thing applies to having two IO Sample methods run in parallel when both are targete

	d to the same connect or.

Properties

Property	Description
Conversion Time (ticks)	Sets the convert to convert period when scanni ng through a channel List. This property allows users to set a minimum convert to convert perio d of 1 us and a maximum of 1 ms. This property is in the unit of ticks, with a tick rate of 40MHz or a tick resolution of 25 ns. This property does not affect the conversion time of the IO Sample met hod.
UART Enable	Enables or disables the UART usage through DIO 16 and DIO 17 for both ConnectorA and Connect orB. UART is disabled by default.
Console Out Enable	Reads the Console Out settings. This property is applicable for ConnectorA only.
Terminal Mode	Refer to the NI sbRIO-9627 (FPGA Interface) topi c for a description of this property.
Voltage Range	Refer to the NI sbRIO-9627 (FPGA Interface) topi c for a description of this property.

Single-Cycle Timed Loop

This device supports the single-cycle Timed Loop for digital I/O only. Configure the number of output synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Properties dialog box. Configure the number of input synchronizing registers for the channels of this device in the Advanced Code Generation page of the FPGA I/O Node Properties dialog box.

IO Sample Method (FPGA Interface)

This module method acquires a single sample from the module. The channel number, terminal mode, and voltage range are all configurable at run time. You use this module method by selecting it in an FPGA I/O Method Node that is configured for the appropriate device and/or channel. Details

Note Do not configure the VI to run an IO Sample method and an AI IO Node in parallel when both are targeted to the same connector. This will cause incorrect reading from the IO Sample method. The AI IO Node still gives the correct reading, but will not be able to meet the specified data rate. The same thing applies to having two IO Sample methods run in parallel when both are targeted to the same connector.

Voltage Range [i+1] contains the voltage range setting that gets loaded into the module conversion pipeline. This setting affects the data to be sampled one iteration into the future. Refer to Conversion Timing topic for more information.

Terminal Mode [i+1] contains the terminal mode setting that gets loaded into the module conversion pipeline. This setting affects the data to be sampled one iteration into the future. Refer to Conversion Timing topic for more information.

Channel Number [i+1] contains the channel number that gets loaded into the module conversion pipeline. This setting affects the data to be sampled one iteration into the future. Refer to Conversion Timing topic for more information.

Data [i] Returns the data from the current sample.

error in describes error conditions that occur before this VI or function runs. The default is `no error`. If an error occurred before this VI or function runs, the VI or function passes the **error in** value to **error out**. This VI or function runs normally only if no error occurred before this VI or function runs. If an error occurs while

this VI or function runs, it runs normally and sets its own error status in **error out**. Use **error in** and **error out** to check errors and to specify execution order by wiring **error out** from one node to **error in** of the next node.

status is TRUE (X) if an error occurred before this VI or function ran or FALSE (checkmark) to indicate a warning or that no error occurred before this VI or function ran. The default is FALSE.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

error out contains error information. If **error in** indicates that an error occurred before this VI or function ran, **error out** contains the same error information. Otherwise, it describes the error status that this VI or function produces. Right-click the **error out** indicator on the front panel and select **Explain Error** from the shortcut menu for more information about the error.

status is TRUE (X) if an error occurred or FALSE (checkmark) to indicate a warning or that no error occurred.

code is the error code number identifying an error. The default is 0. If status is TRUE, code is a nonzero error code. If status is FALSE, code is 0 or a warning code.

source always contains an empty string because strings are not supported in LabVIEW FPGA.

Using This Method

The IO Sample method provides an efficient and flexible interface to the module. You can use this method to acquire a single sample from any of the channels on the module, at any range and with any available input mode.

When this method is executed, the module performs a single conversion on the next channel present in the conversion pipeline on the module. The data from this conversion is returned via the **Data** [i] method output. While the conversion data is read from the module, the new configuration information specified by the three method inputs (**Voltage Range** [i+1], **Terminal Mode** [i+1], and **Channel Number** [i+1]) is loaded into the configuration pipeline on the module. The pipeline is one sample deep. So, the configuration information specified on one execution of the IO Sample method determines which channel will be sampled by the IO Sample method one iteration into the future. Refer to the Conversion Timing topic for more details.

Conversion Timing for the NI ELVIS III (FPGA Interface)

The NI ELVIS III implements a one-element deep pipeline to access the AI channels per connector. This pipeline results in maximum sample rate, but may not result in the best resolution. To achieve better resolution, you will need to add your own loop delay and slow down the sampling rate. When using the FPGA I/O Node to sample channels, the pipeline is automatically managed by the FPGA I/O Node, and the channels within the FPGA I/O Node are sampled in numerical order regardless of the order they appear in the node.

If the first channel request in the FPGA I/O Node does not match the first channel request stored in the module pipeline, there will be a delay before the first sample occurs. This delay is caused by the input settling time, which is required for the input value to reach a steady level before starting conversion.

If the next channel request in the FPGA I/O Node matches the previous channel request, there will not be any delay incurred, because that channel would have already settled, unless there's a change in the Voltage Range and Terminal Mode setting, which then requires the FPGA I/O Node to wait for the settling delay.

You can reduce this settling delay using the Conversion Time Property Node, which allows a range from 40 ticks to 40000 ticks. One tick corresponds to 25 ns. By default, the convert to convert period is 75 ticks. Setting it to 40 ticks ensures that you are scanning through your channel list at 1 MS/s, but at a lower resolution. Setting it to 40000 ticks ensures that you are scanning through the channel list at 1kS/s, but at a higher resolution.

When using the IO Sample method, you must take steps to manage this pipeline in the VIs. To read one channel, that channel must be requested one cycle before the time it is to be sampled. The following diagram illustrates how the pipeline works within a sequence structure. A typical application would use a loop structure to iterate through a scan list, which is a predefined list of channels and settings, continuously. The sequence structure shows how data moves into the ELVIS III pipeline and then is converted.